LITE-ON SEMICONDUCTOR

# L12ESDL5V0C6-4

**ESD PROTECTION DEVICE**

STAND-OFF VOLTAGE - **5.0** Volts
POWER DISSIPATION - **120** WATTS

## GENERAL DESCRIPTION

The L12ESDL5V0C6-4 is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

## FEATURES

- Protects up to four I/O lines (Data lines) & power line (Vcc pin5)
- Low capacitance: 0.3pF typical (I/O to I/O)
- Low clamping voltage
- IEC 61000-4-2, level 4 ( ESD ), > ±15KV ( air ) ; > ±8KV ( contact ).

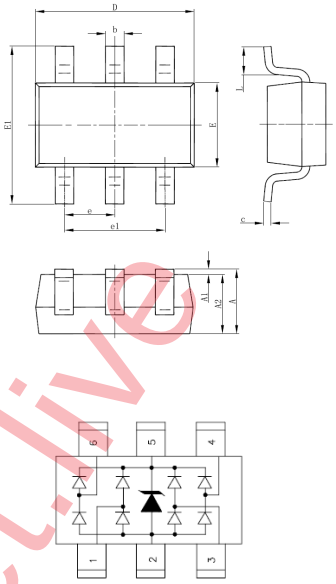
## APPLICATION

- High Definition Multimedia Interface (HDMI)
- Digital Visual Interface (DVI)
- Monitors and Flat Panel Displays
- USB 2.0
- USB OTG
- IEEE 1394 Firewire Port

## MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/E

## SOT23-6L



4 lines Protection

| SOT23-6L | | |
|---|---|---|
| DIM. | MIN. | MAX. |
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.30 | 0.50 |
| c | 0.08 | 0.22 |
| D | 2.45 | 3.00 |
| E | 1.50 | 1.75 |
| E1 | 2.80 typ. | |
| e | 0.95 typ. | |
| e1 | 1.90 typ. | |
| L | 0.30 | 0.60 |
| All Dimensions in millimeter | | |

| PIN ASSIGNMENT | |
|---|---|
| 1, 3, 4, 6 | I/O Lines |
| 5 | $V_{CC}$ |
| 2 | Ground |

## MAXIMUM RATINGS (Tj= 25℃ unless otherwise noticed)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Pulse Power (tp = 8/20us) | $P_{pk}$ | 120 | W |
| Peak Pulse Current (tp = 8/20us) | Ipp | 5 | A |
| Operating Junction Temperature Range | $T_J$ | -55 to + 125 | ℃ |
| Storage Temperature Range | Tstg | -55 to + 150 | ℃ |
| Soldering Temperature, t max = 10s | $T_L$ | 260 | ℃ |

## ELECTRICAL CHARACTERISTICS (Tj= 25℃ unless otherwise noticed)

| Parameter | Symbol | Conditions | Mln | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Reverse standoff voltage | $V_{RWM}$ | Any pin to ground | --- | --- | 5.0 | V |
| Breakdown voltage | VBR | IR = 1 mA | 6.0 | --- | --- | V |
| Reverse leakage current | IRM | $V_{DRM}$ = 5V | --- | --- | 1 | uA |
| Clamping Voltage | $V_C$ | $I_{PP}$ = 1A, tp = 8/20μs, Any I /O pin to ground | --- | --- | 15 | V |
| Clamping Voltage | $V_C$ | $I_{PP}$ = 5A, tp = 8/20μs, Any I/O pin to ground | --- | --- | 24 | V |
| Junction capacitance | $C_J$ | $V_R$ = 2.5V, f = 1MHz, Any I/O pin to ground | --- | --- | 0.8 | pF |
| Junction capacitance | $C_J$ | $V_R$ = 2.5V, f = 1MHz, Between I/O pins | --- | --- | 0.4 | pF |



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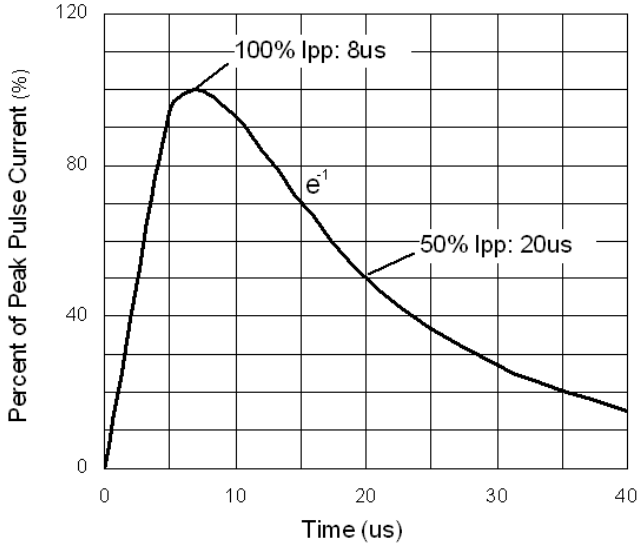



**Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5**

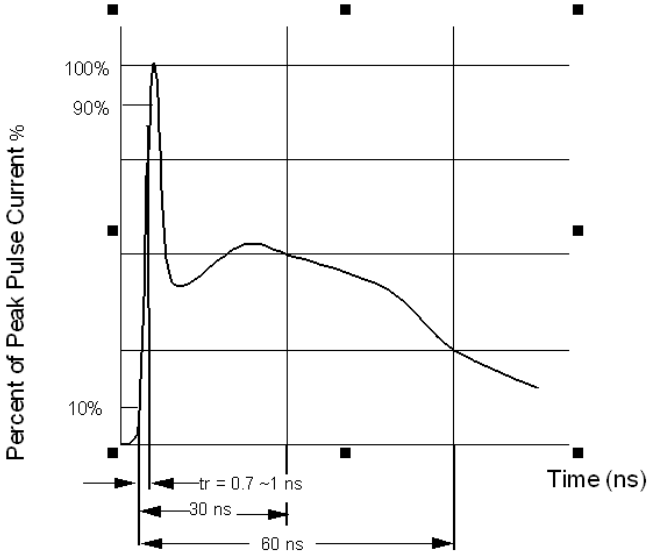



**Figure 2. ESD pulse waveform according to IEC 61000-4-2**

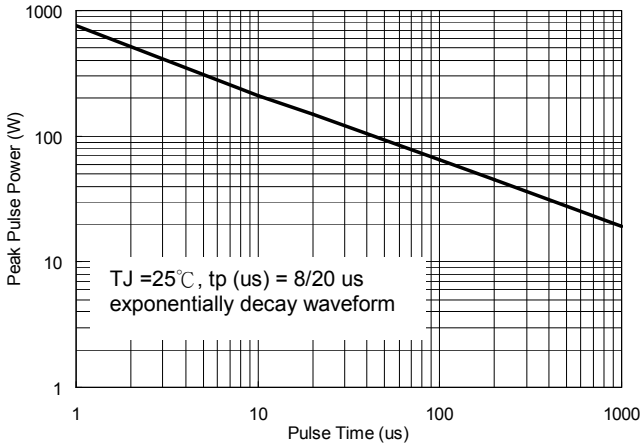



**Figure 3. Power Dissipation versus Pulse Time**

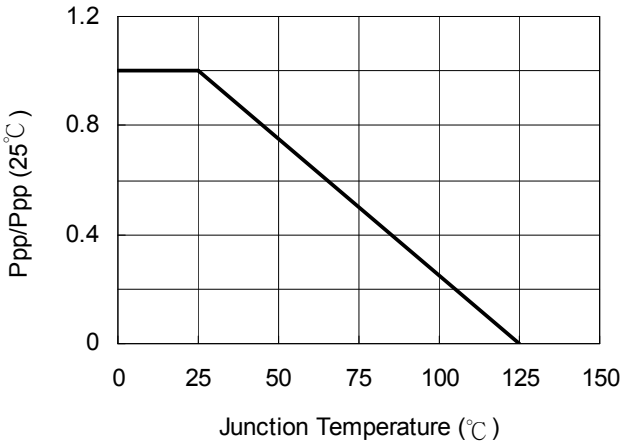



**Figure 4. Peak pulse power versus TJ**

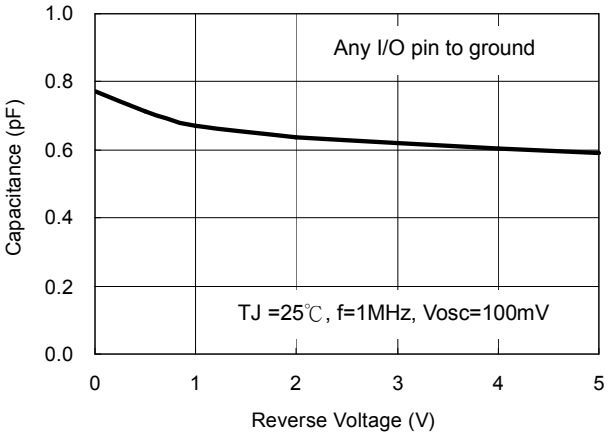



**Figure 5. Typical Junction Capacitance**

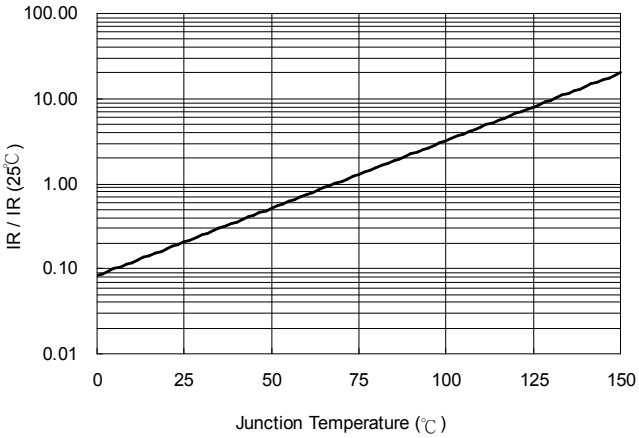



**Figure 6. Reverse Leakage Current versus TJ**

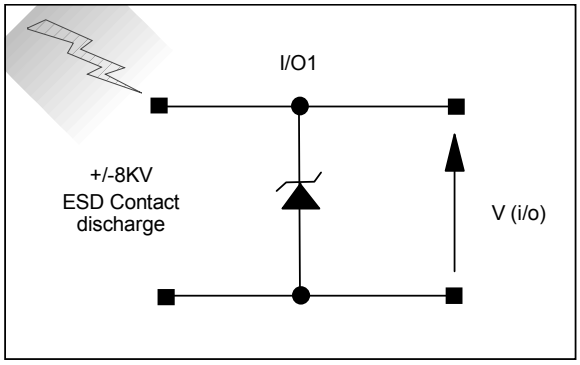



**Figure 7. ESD Test Configuration**

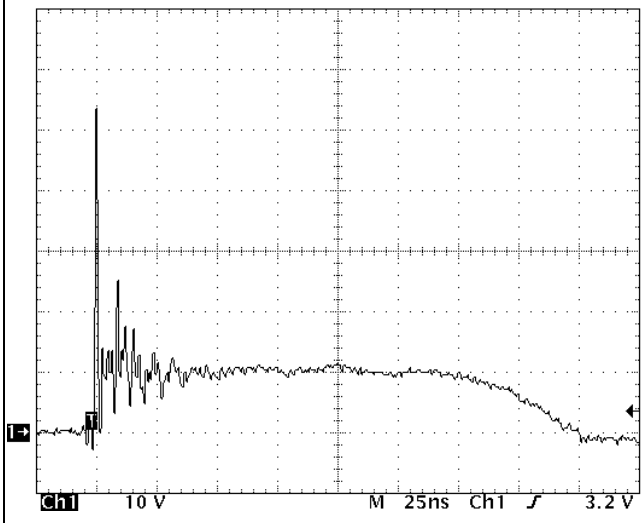



**Figure 8. Clamped +8 kV ESD voltage waveform**

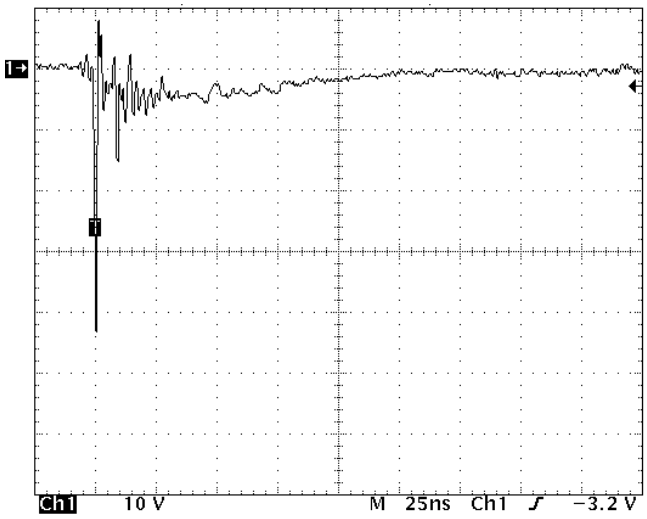
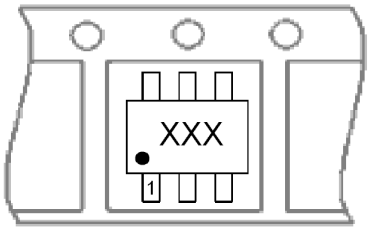



**Figure 9. Clamped -8 kV ESD voltage waveform**

## Marking & Orientation

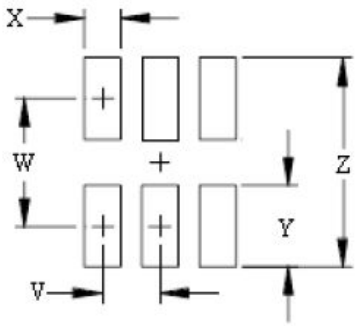



| DEVICE | Wire | Marking | Packing |
|---|---|---|---|
| L12ESDL5V0C6-4 | Au | LC5 | Taping / Reel |
| L12ESDL5V0C6-4C | Cu | LCV | Taping / Reel |

## Packaging Information

| DEVICE | Q'TY/REEL (PCS) | REEL DIA. (INCH) | Q'TY/BOX (PCS) | Q'TY/CARTON (PCS) |
|---|---|---|---|---|
| L12ESDL5V0C6-4<br>L12ESDL5V0C6-4C | 3000 | 7 | 45000 | 90K/180K |

## SOT23-6L Soldering Pad Layout




| Dim. | Millimeters | Inches |
|---|---|---|
| Z | 3.60 | 0.141 |
| X | 0.80 | 0.031 |
| W | 2.60 | 0.102 |
| Y | 1.00 | 0.039 |
| V | 0.95 | 0.037 |

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