NT7065B

40 COMMON / SEGMENT DRIVER FOR DOT MATRIX LCD

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LCD DRIVER

40-Channel Segment / Common Driver For Dot Matrix LCD

The NT7065B is a LCD driver LSI which is fabricated by low power CMOS technology. Bascially this LSI consists of 20 x 2 bit bi-directional shift register, 20 x 2 bit data latch and 20 x 2 bit driver. (refer to Fig 1) This LSI can be used a common or segment driver.

Function

- Dot matrix LCD driver with 40 channel output.
- Selectable function to use common/segment drivers simultaneously.
- Input / Output signal.

--- output; 20 x 2 channel waveform for LCD driving
--- Input ; - Serial display date and control pulse from the controller LSI.
- Bias voltage (V_1-V_6)

Features

- Display driving bias: static~1/5
- Power supply voltage: +5V ± 10%;+3V ± 10%
- LCD supply voltage:3~13V (V_{DD}-V_{EE})
- Interface : (Controller NT7066U)

- CMOS Process
- 64QFP and bare chip available

Block Diagram

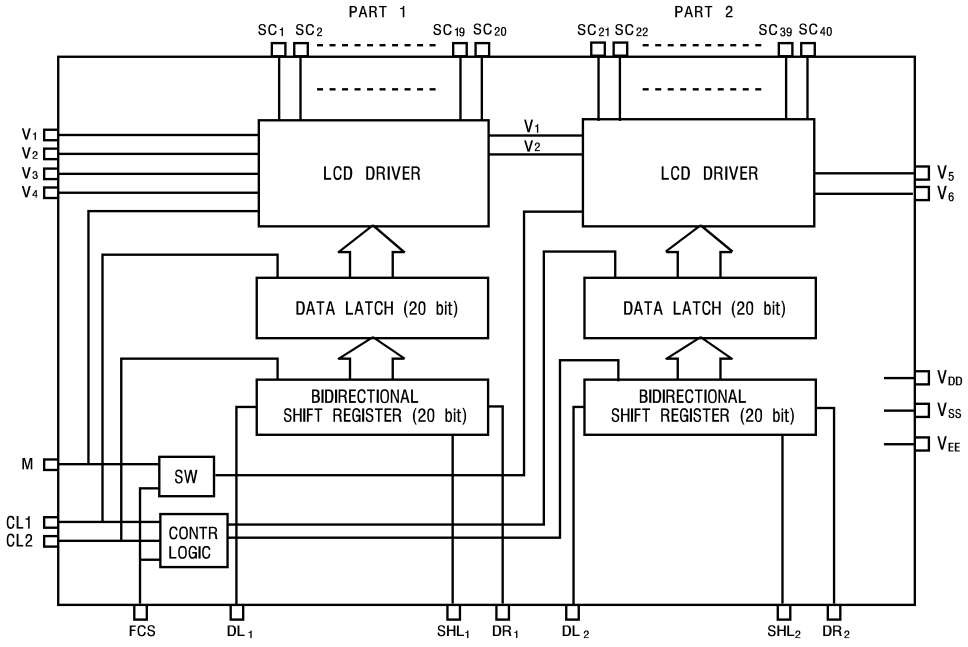


Fig. 1. NT7065B functional block diagram

PIN DESCRIPTION

<table>
<tr><th>PIN(NO.)</th><th>INPUT/ OUTPUT</th><th colspan="2">NAME</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>V_{DD}(24)</td><td rowspan="3">Power</td><td colspan="2" rowspan="2">Operating Voltage</td><td>For logical circuit (+5V ± 10%,+3V ±10%)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>GND(34)</td><td>0V(GND)</td></tr>
<tr><td>V_{EE}(31)</td><td colspan="2">Negative Supply Voltage</td><td>For LCD driver circuit (-5V)</td></tr>
<tr><td>V_1 V_2 (44,45)</td><td>Input</td><td colspan="2">Bias Voltage</td><td>Bias Voltage level for LCD drive (select level)</td><td>Power</td></tr>
<tr><td>SC_1~SC_{20}</td><td>Output</td><td rowspan="4">Part 1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>V_3 V_4 (46,47)</td><td>Input</td><td>Bias voltage</td><td>Bias voltage level for LCD drive (nonselect level)</td><td>Power</td></tr>
<tr><td>SHL1 (41)</td><td>Input</td><td rowspan="2">Data interface</td><td>Selection of the shift direction of Part 1 shift register
<table><tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL1, DR1 (35,36)</td><td>Input Output</td><td>Data input/output of Part 1 shift register</td><td>Controller or NT7065B</td></tr>
<tr><td>SC_{21}~SC_{40}</td><td>Output</td><td rowspan="4">Part 2</td><td>LCD driver</td><td>LCD driver output</td><td></td></tr>
<tr><td>V5 V6 (48,49)</td><td>Input</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (nonselect level)</td><td>Power</td></tr>
<tr><td>SHL2(42)</td><td>Input</td><td rowspan="2">Data interface</td><td>Selection of the shift direction of Part 2 shift register
<table><tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL2,DR2 (37,38)</td><td>Input Output</td><td>Data input/output of Part 2 shift register</td><td>Controller or NT7065B</td></tr>
<tr><td>M(40)</td><td>Input</td><td colspan="2">Alternated signal for LCD driver output</td><td rowspan="3"><table><tr><th>PART</th><th>FCS</th><th>CL1</th><th>CL2</th><th>M polarity</th></tr><tr><td rowspan="2">1</td><td>VSS</td><td rowspan="2">latch clock (↓)</td><td rowspan="2">shift clock (↓)</td><td rowspan="2">M</td></tr><tr><td>VDD</td></tr><tr><td rowspan="2">2</td><td>VSS</td><td rowspan="2">shift clock (↑)</td><td rowspan="2">latch clock (↑)</td><td rowspan="2">$\overline{M}$</td></tr><tr><td>VDD</td></tr></table>
Shift/latch clock of display data and polarity of M signal are changed by FCS signal.
By setting FCS to V_{DD} level, user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously</td><td rowspan="3">Controller</td></tr>
<tr><td>CL1,CL2 (32,33)</td><td>Input</td><td colspan="2">Data shift/latch clock</td></tr>
<tr><td>FCS(43)</td><td>Input</td><td colspan="2">Mode selection</td></tr>
<tr><td>NC(39)</td><td></td><td colspan="2"></td><td>No connection pin</td><td>N.C</td></tr>
</table>

Maximum Absolute Limit (Ta=25°C)

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	–0.3 ~ +7.0	V
Driver supply voltage	V_{LCD}	V_{DD}–13.5 ~ V_{DD}+0.3	V
Input voltage 1	$V_{IN\ 1}$	–0.3 ~ V_{DD}+0.3	V
Input Voltage 2 (V_1–V_6)	$V_{IN\ 2}$	V_{DD}+0.3 ~ V_{EE} –0.3	V
Operating temperature	T_{opr}	–30 ~ +85	°C
Storage temperature	T_{stg}	–55 ~ +125	°C

- Voltage greater than above may damage to the circuit
- V_{EE} connect a protection resistor (220Ω ±5%)

ELECTRICAL CHARACTERISTICS

DC characteristics (V_{DD}=2.7 ~ 5.5V, V_{DD}-V_{EE}=3 ~ 13V, V_{SS}=0V, Ta= -30~ +85°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current *	I_{DD}	f_{CL2}=400KHz	-	1	mA	-
Supply Current *	I_{EE}	F_{cl1}=1KHz	-	10	µA	
Input High Voltage	V_{IH}	-	0.7 V_{DD}	V_{DD}	V	CL1, CL2, DL1, DL2 DR1, DR2, SHL1, SHL2 M, FCS
Input Low Voltage	V_{IL}		0	0.3 V_{DD}		
Input Leakage Current	I_{LKG}	V_{IN}=0-V_{DD}	-5	5	µA	
Output High Voltage	V_{OH}	I_{OH}= -0.4mA	V_{DD}-0.4	-	V	DL1, DL2, DR1, DR2
Output Low Voltage	V_{OL}	I_{OL}= +0.4mA	-	0.4		
Voltage Descending	V_{D1}	I_{ON}=0.1mA for one of SC1-SC40	-	1.1		V(V_1-V_6)-SC(SC1-SC40)
	V_{D2}	I_{ON}=0.05mA for each SC1-SC40		1.5		
Leakage Current	I_V	V_{IN}=V_{DD}~V_{EE} (Output SC1~SC40 : floating)	-10	10	µA	V1-V6

*V_{DD}-V_{EE}=4V

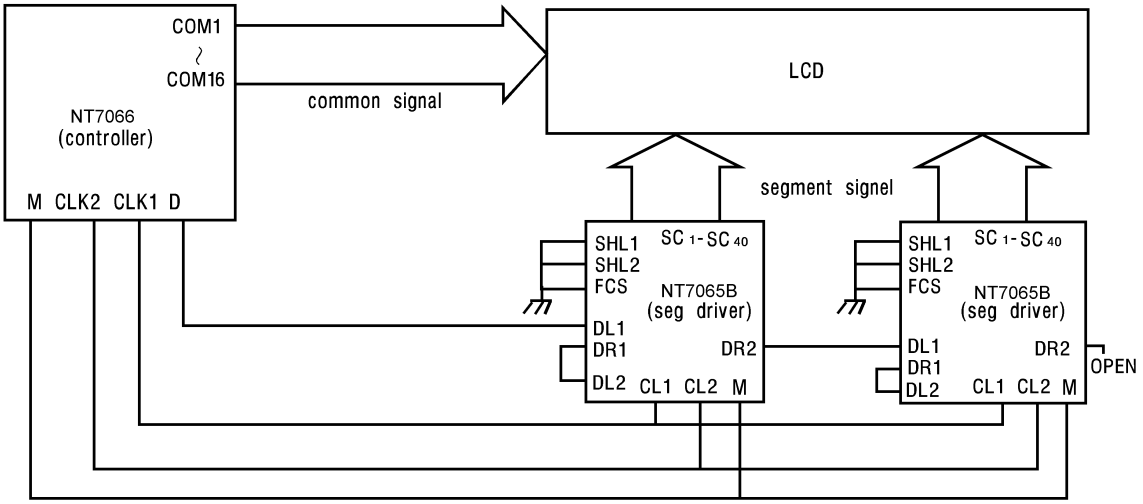
AC CHARACTERISTICS (V_{DD}=2.7~5.5V, V_{DD}-V_{EE}=3~13V, V_{SS}=0V, Ta= -30~ +85°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	f_{CL}	-	-	400	KHz	CL2
Clock High Level Width	t_{WCKH}	-	800	-	ns	CL1, CL2
Clock Low Level Width	t_{WCKL}	-	800	-		CL2
Clock Set-up Time	t_{SL}	from CL2 to CL1	500	-		CL1, CL2
	t_{LS}	from CL1 to CL2	500	-		
Clock Rise/Fall Time	t_R/t_F	-	-	200		
Data Set-up Time	t_{SU}	-	300	-		DL1, DL2, DR1, DR2, FLM
Data Hold Time	t_{DH}	-	300	-		
Data Delay Time	t_D	CL=15pF	-	500		DL1, DL2, DR1, DR2

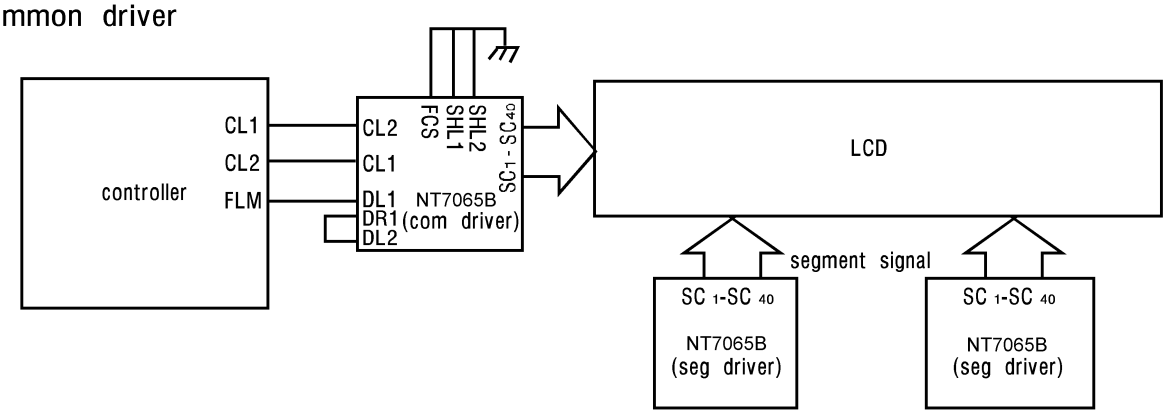
* Input/Output current is excluded; When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, To avoid this, input level must be fixed at “H” or “L”.

Application Circuit

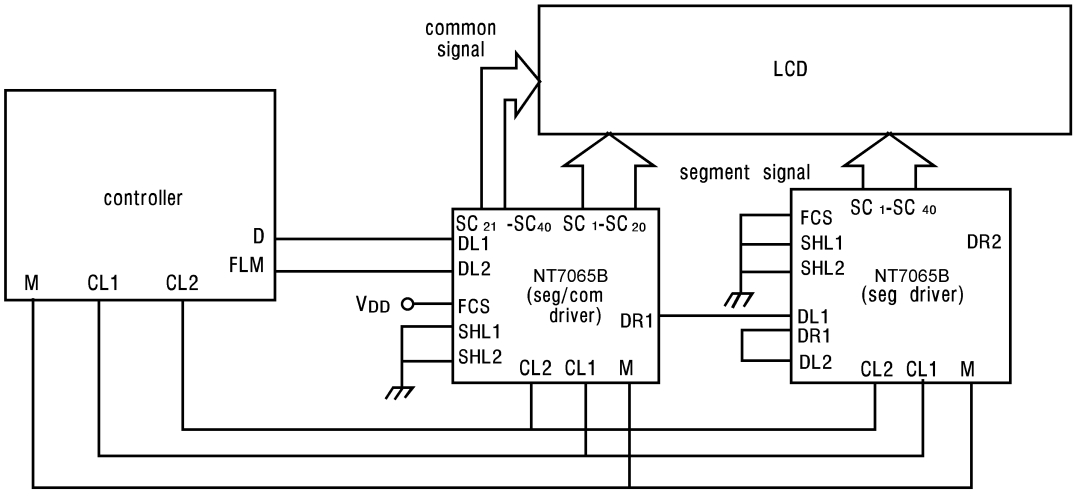
1) Segment driver



2) Common driver



3) Segment/common driver



2) To drive common type

When the FCS is connected to VDD, only part2 (SC21-SC40) of 0065 is operated as common driver (refer to Fig 5).

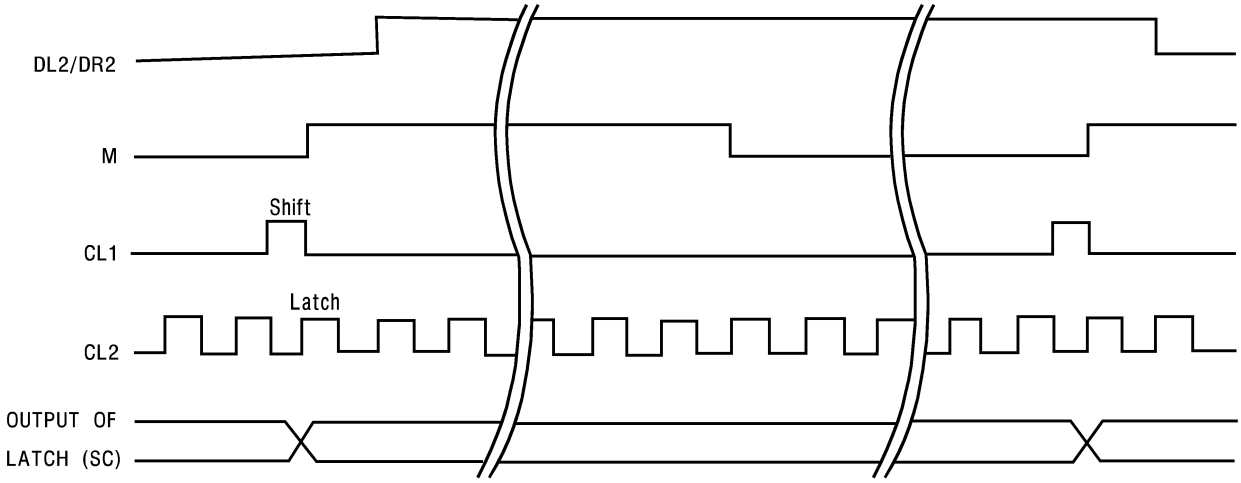


Fig . 5. Common Data Waveforms

LCD OUTPUT WAVEFORMS

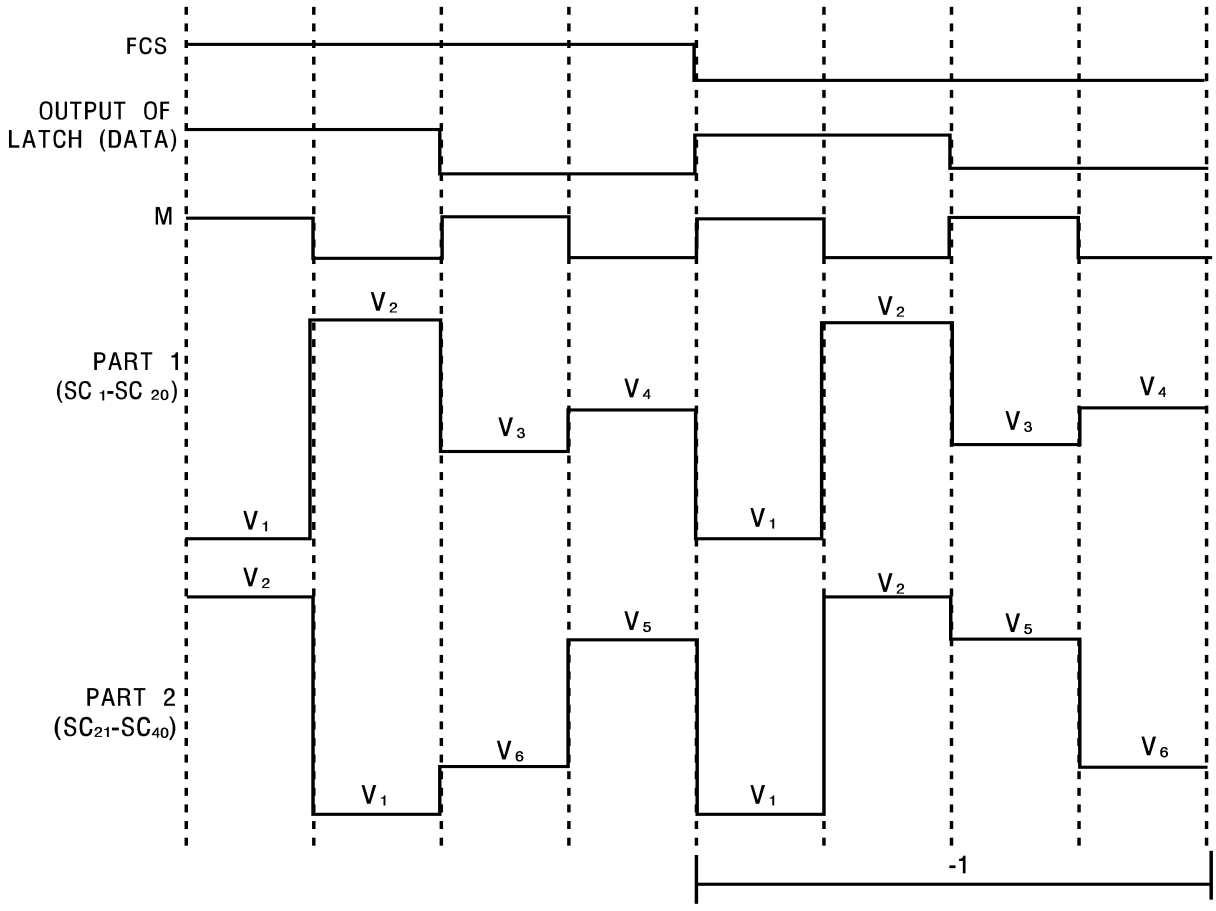


Fig. 6. Output waveform

*1: To usa for same function of part 1 and part 2, V3 and V5, V4 and V6 of power supply for LCD driver are short circuited respectively.

Timing Characteristics

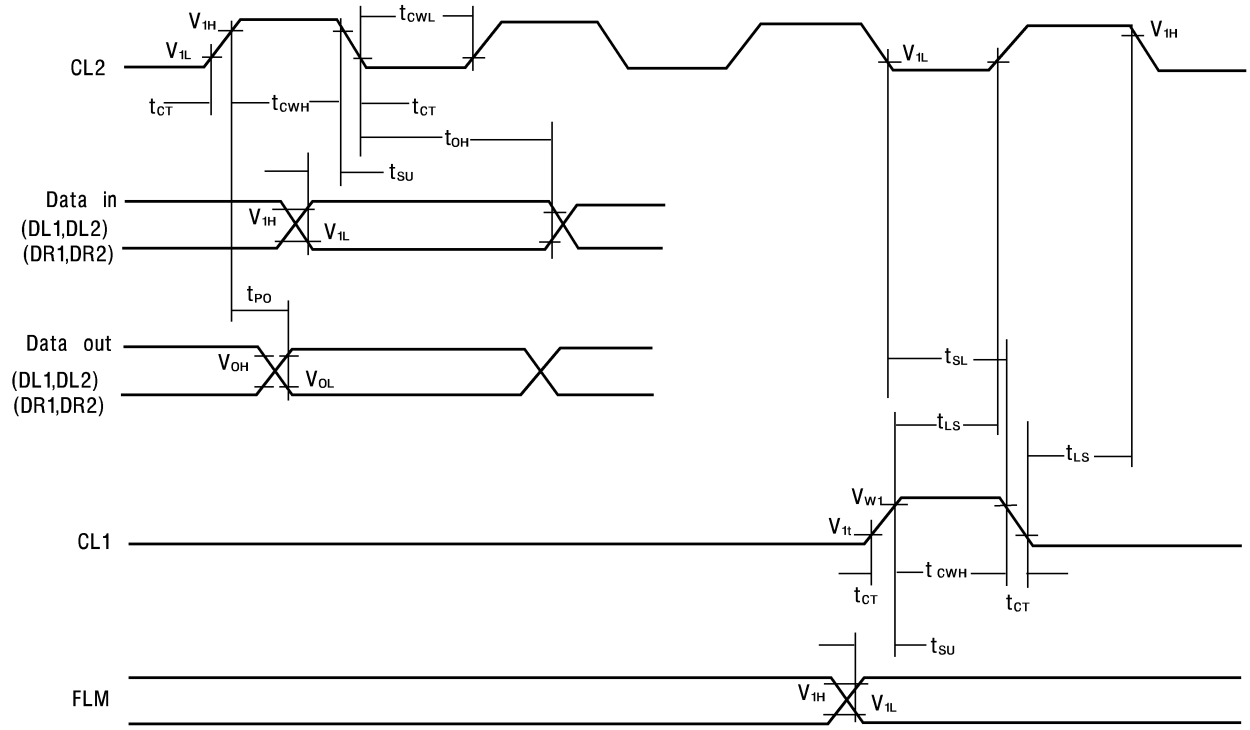


Fig . 3. AC characteristics

Functional Description

1) To drive segment type
When the FCS is connected to Vss, NT7065B (SC1-SC40) is operated as segment driver.(refer to fig 4)

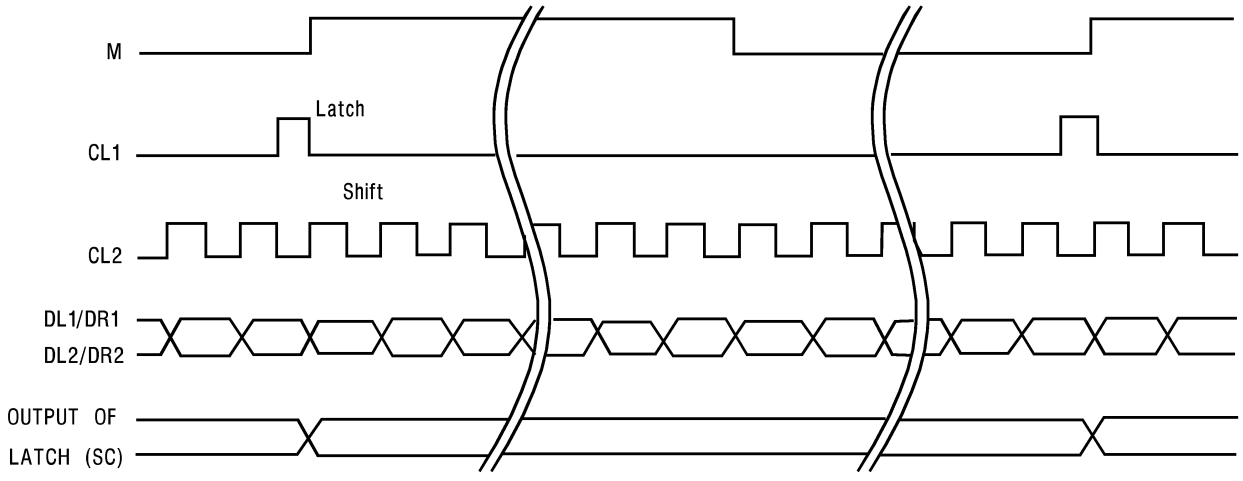


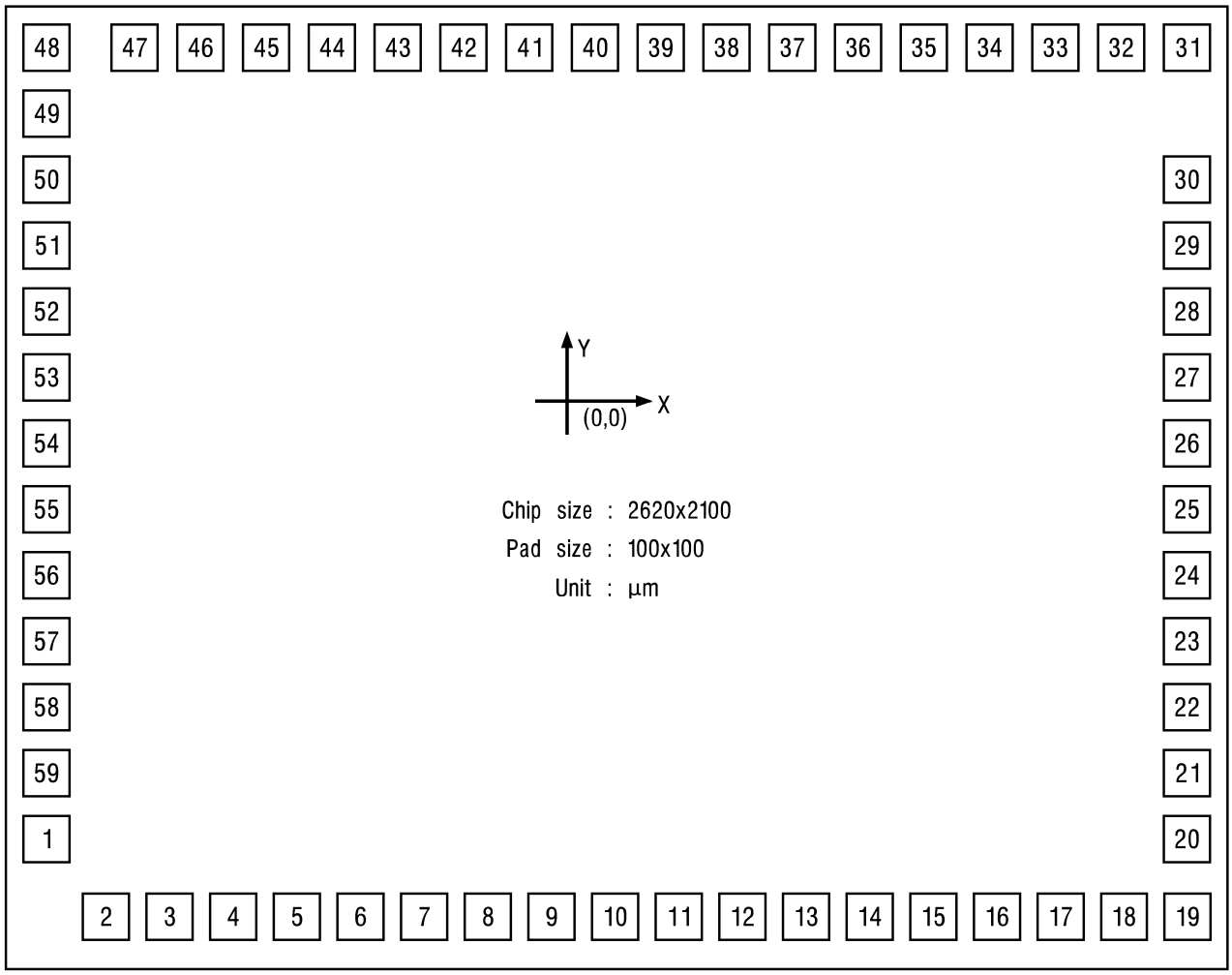
Fig. 4. Segment Data Waveforms

Pad Location

PAD No	PAD NAME	COORDINATE		PAD No	PAD NAME	COORDINATE	
		X	Y			X	Y
1	VEE	-1120,2	-642,5	31	SC28	1117,5	865,2
2	CL1	-1062,5	-865,2	32	SC27	992,5	865,2
3	CL2	-937,5	-865,2	33	SC26	867,5	865,2
4	VSS	-812,5	-865,2	34	SC25	742,5	865,2
5	DL1	-687,5	-865,2	35	SC24	617,5	865,2
6	DR1	-562,5	-865,2	36	SC23	492,5	865,2
7	DL2	-437,5	-865,2	37	SC22	367,5	865,2
8	DR2	-312,5	-865,2	38	SC21	242,5	865,2
9	M	-187,5	-865,2	39	SC20	117,5	865,2
10	SHL1	-62,5	-865,2	40	SC19	-7,5	865,2
11	SHL2	62,5	-865,2	41	SC18	-132,5	865,2
12	FCS	187,5	-865,2	42	SC17	-257,5	865,2
13	V1	332,5	-865,2	43	SC16	-382,5	865,2
14	V2	457,5	-865,2	44	SC15	-507,5	865,2
15	V3	582,5	-865,2	45	SC14	-632,5	865,2
16	V4	707,5	-865,2	46	SC13	-757,5	865,2
17	V5	832,5	-865,2	47	SC12	-882,5	865,2
18	V6	957,5	-865,2	48	SC9	-1120,2	-857,2
19	SC40	1082,5	-865,2	49	SC10	-1120,2	732,5
20	SC39	1120,2	-627,5	50	SC11	-1120,2	607,5
21	SC38	1120,2	-502,5	51	SC8	-1120,2	482,5
22	SC37	1120,2	-377,5	52	SC7	-1120,2	357,5
23	SC36	1120,2	-252,5	53	VDD	-1120,2	232,5
24	SC35	1120,2	-127,5	54	SC6	-1120,2	107,5
25	SC30	1120,2	-2,5	55	SC5	-1120,2	-17,5
26	SC31	1120,2	122,5	56	SC4	-1120,2	-142,5
27	SC32	1120,2	247,5	57	SC3	-1120,2	-267,5
28	SC33	1120,2	372,5	58	SC2	-1120,2	-392,5
29	SC34	1120,2	479,5	59	SC1	-1120,2	-517,5
30	SC29	1120,2	622,5				

Note:(0,0) is centre in the chip

Pad Diagram



The NT7065B substrate should be connected to Vdd in the PCB layout artwork.