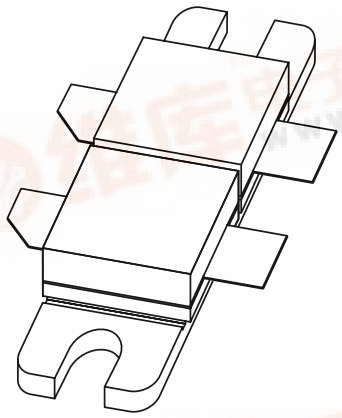
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DATA SHEET



BLV862
UHF linear push-pull power transistor

Product specification
Supersedes data of 1997 Oct 14

1999 Jun 25

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PHILIPS

UHF linear push-pull power transistor BLV862

FEATURES

- Double stage internal input and output matching networks for an optimum wideband capability and high gain
- Polysilicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Common emitter class-AB operation in output stages in bands 4 and 5 (470 to 860 MHz) television transmitter amplifiers (vision or sound).

DESCRIPTION

NPN silicon planar epitaxial transistor with two sections in push-pull configuration. The device is encapsulated in a SOT262B 4-lead rectangular flange package, with two ceramic caps.

PINNING

PIN	SYMBOL	DESCRIPTION
1	c1	collector 1; note 1
2	c2	collector 2; note 1
3	b1	base 1
4	b2	base 2
5	e	common emitter; note 2

Notes

1. Collectors 1 and 2 are connected together internally.
2. Common emitters are connected to the flange.

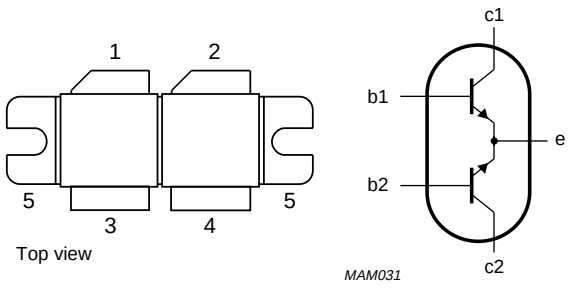


Fig.1 Simplified outline (SOT262B) and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	ΔG_p (dB)
CW class-AB	860	28	150	≥8 typ. 9	≥45 typ. 52	≤1

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

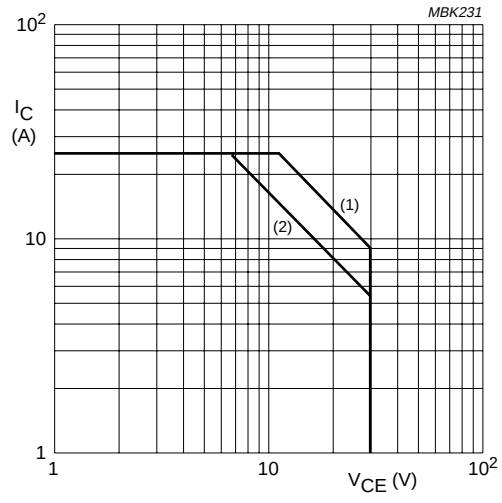
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	25	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	350	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 350 W; note 1	0.5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 1	0.15	K/W

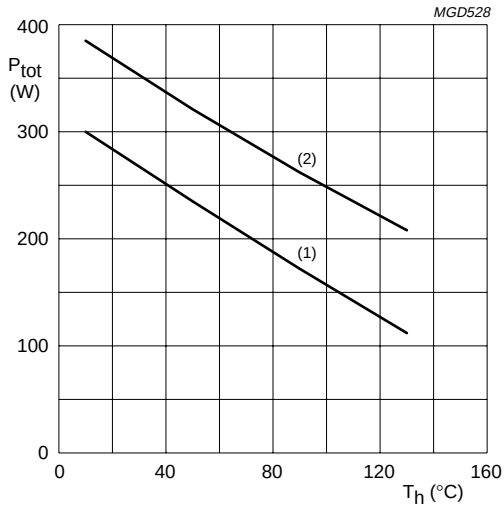
Note

1. Thermal resistance is determined under specified RF operating conditions.



Total device; both sections equally loaded.
(1) T_{mb} = 25 °C.
(2) T_h = 70 °C.

Fig.2 DC SOAR.



Total device; both sections equally loaded.
(1) Continuous operation.
(2) Short time operation during mismatch.

Fig.3 Power derating curves.

CHARACTERISTICS

Values apply to either transistor section; T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_E = 0; I_C = 60 mA	65	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_B = 0; I_C = 150 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_E = 3 mA; I_C = 0	3	–	–	V
I_{CBO}	collector-base leakage current	V_{CB} = 28 V	–	–	5	mA
h_{FE}	DC current gain	I_C = 4.5 A; V_{CE} = 10 V	30	–	140	–
Δh_{FE}	DC current gain ratio of both sections	I_C = 4.5 A; V_{CE} = 10 V	0.67	–	1.5	–
C_c	collector capacitance	$I_E = i_e$= 0; V_{CE} = 28 V; f = 1 MHz; note 1	–	75	–	pF

Note

1. The value of C_c is that of the die only, it is not measurable because of the internal matching network.

APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter push-pull class-AB test circuit; note 1.

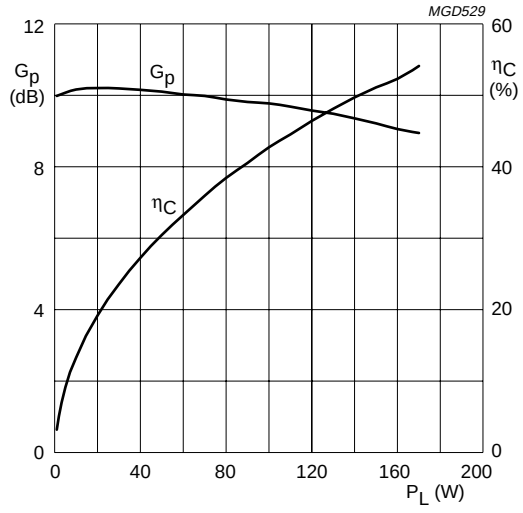
MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	P_L (W)	G_p (dB)	η_C (%)	ΔG_p (dB)
CW class-AB	860	28	0.8	150	≥8 typ. 9	≥45 typ. 52	≤1

Note

1. See application note *“AN98014 in handbook SC19b.*”

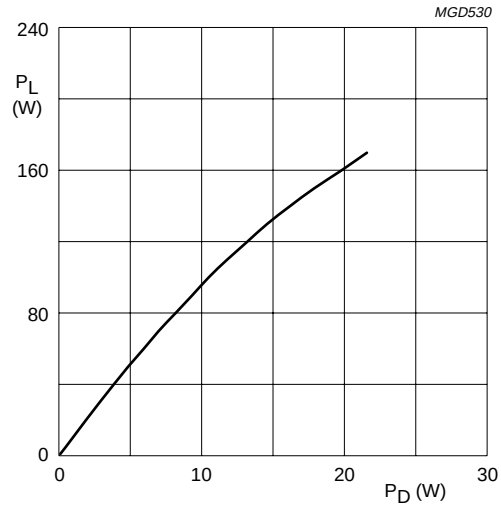
Ruggedness in class-AB operation

The BLV862 is capable of withstanding a load mismatch corresponding to VSWR = 2 : 1 through all phases under the conditions: T_h = 25 °C; f = 860 MHz; V_{CE} = 28 V; I_{CQ} = 0.8 A; P_L = 150 W; $R_{th\ mb\text{-}h}$ = 0.15 K/W.



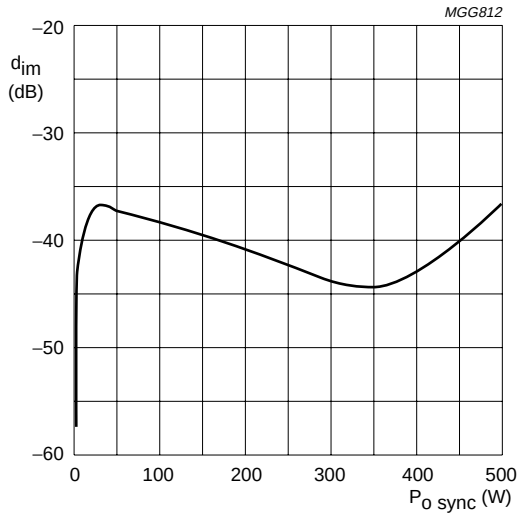
T_h = 25 °C; f = 860 MHz; V_{CE} = 28 V; I_{CQ} = 0.8 A.

Fig.4 Power gain and collector efficiency as functions of load power; typical values.



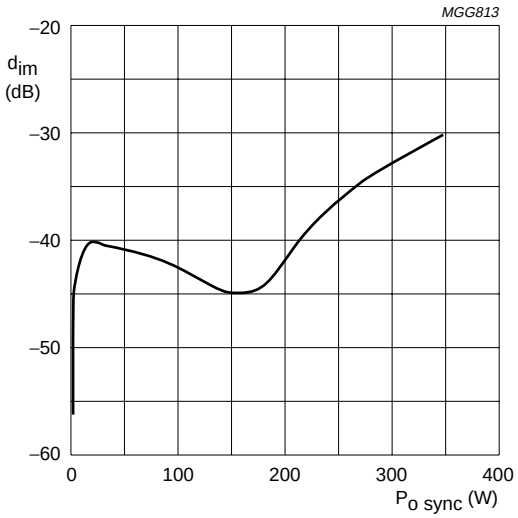
T_h = 25 °C; f = 860 MHz; V_{CE} = 28 V; I_{CQ} = 0.8 A.

Fig.5 Load power as a function of drive power; typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.8 A;
2-tone: f_{vision} = 855.25 MHz (-8 dB); $f_{sideband}$ = 859.68 MHz (-16 dB).

Fig.6 Intermodulation distortion as a function of output power; typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.8 A;
3-tone: f_{vision} = 855.25 MHz (-8 dB); $f_{sideband}$ = 859.68 MHz (-16 dB);
f_{sound} = 860.75 MHz (-10 dB).

Fig.7 Intermodulation distortion as a function of output power; typical values.

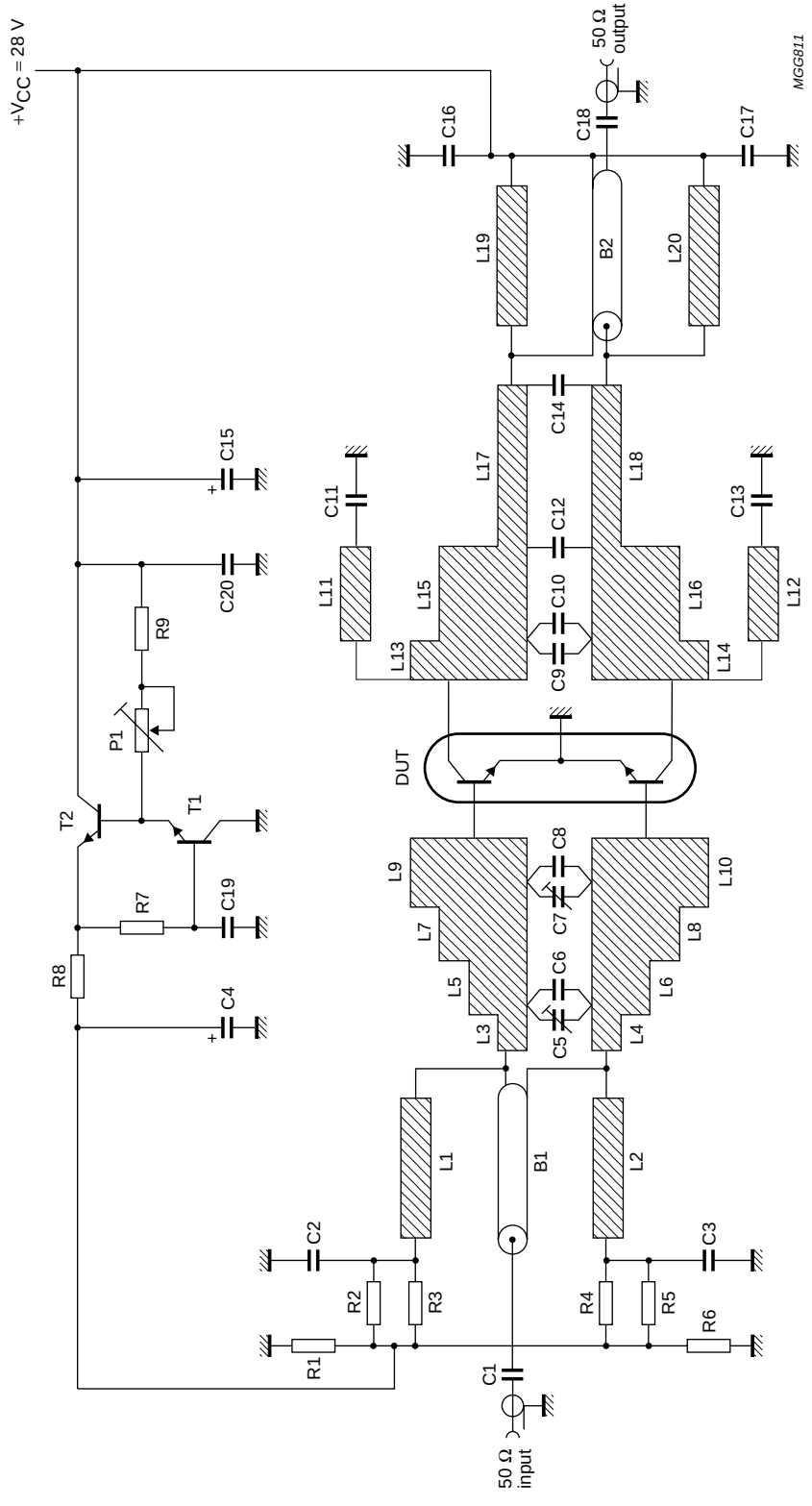
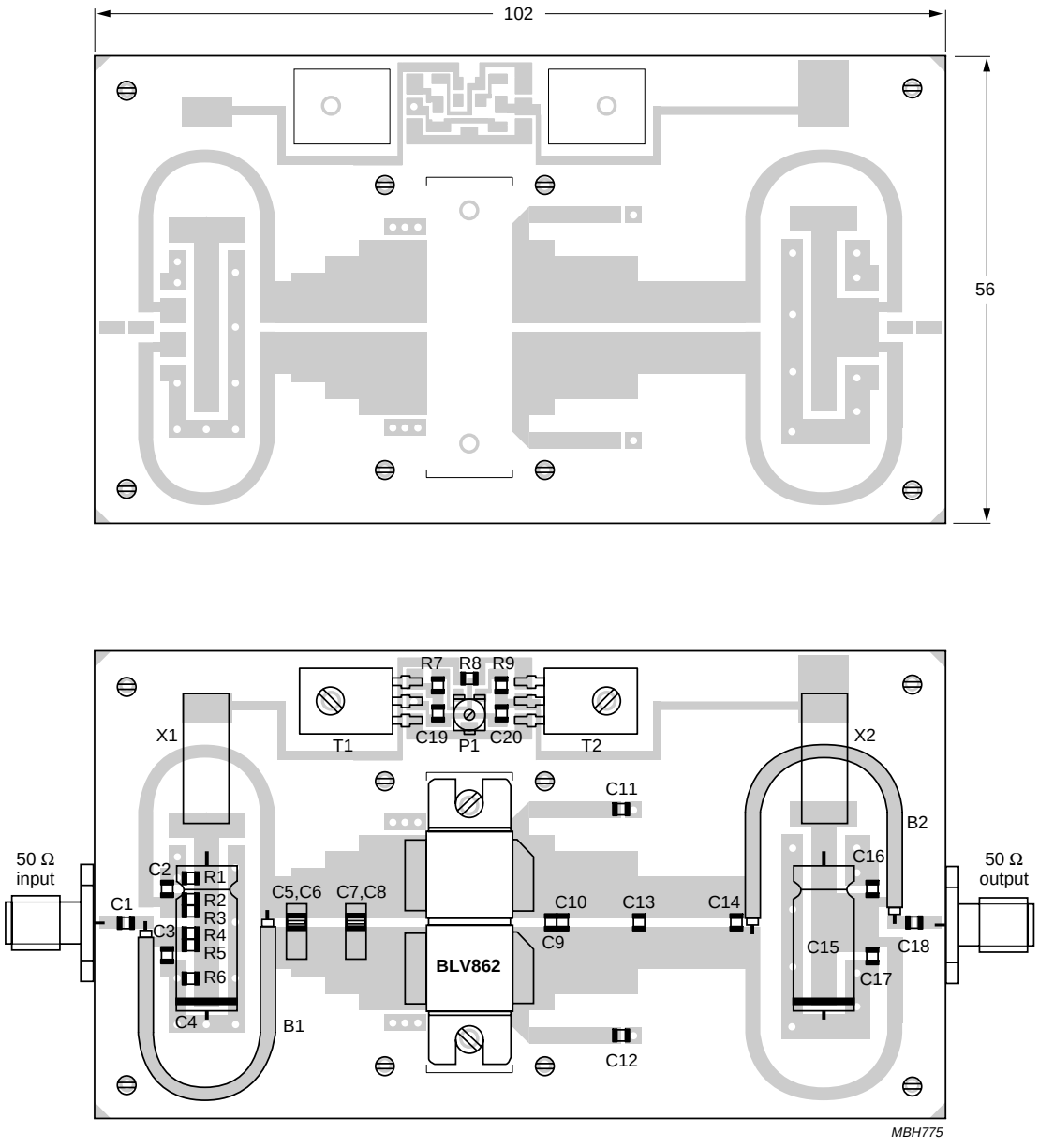


Fig.8 Class-AB test circuit at f = 860 MHz.



Dimensions in mm.

The components are situated on one side of the copper-clad PTFE-glass board (TLX8) from Taconic, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

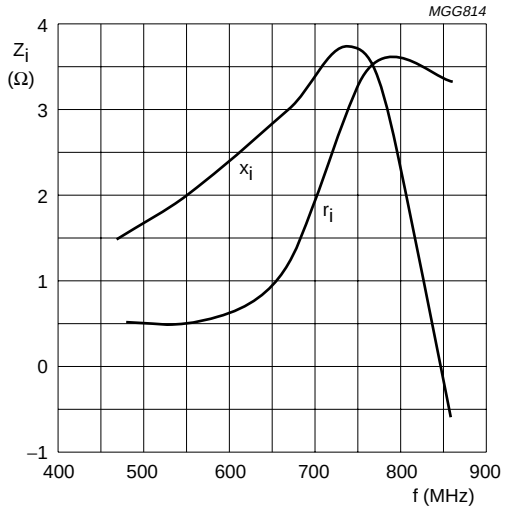
Fig.9 Printed-circuit board and component lay-out for the 860 MHz class-AB test circuit.

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1	multilayer ceramic chip capacitor; note 1	10 pF		
C2. C3	multilayer ceramic chip capacitor	1 nF		2222 852 47102
C4	solid aluminium capacitor	220 μF; 16 V		2222 031 35221
C5, C7	Tekelec trimmer	1 to 5 pF		
C6, C8	multilayer ceramic chip capacitor; note 2	6.8 pF		
C9, C10	multilayer ceramic chip capacitor; note 3	10 pF		
C11, C13	multilayer ceramic chip capacitor; note 1	100 pF		
C12	multilayer ceramic chip capacitor; note 1	8.2 pF		
C14	multilayer ceramic chip capacitor; note 2	3.9 pF		
C15	solid aluminium capacitor	100 μF; 40 V		2222 031 37101
C16, C17	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C18	multilayer ceramic chip capacitor; note 1	22 pF		
C19	multilayer ceramic chip capacitor; note 1	100 pF		
C20	multilayer ceramic chip capacitor	15 nF		2222 852 47153
L1, L2	stripline; note 4		47 × 1.8 mm	
L3, L4	stripline; note 4		2 × 5 mm	
L5, L6	stripline; note 4		4 × 6 mm	
L7, L8	stripline; note 4		4 × 8 mm	
L9, L10	stripline; note 4		8.1 × 10 mm	
L11, L12	stripline; note 4		15 × 2 mm	
L13, L14	stripline; note 4		5 × 10 mm	
L15, L16	stripline; note 4		10 × 8 mm	
L17, L18	stripline; note 4		12.9 × 5 mm	
L19, L20	stripline; note 4		48.7 × 1.8 mm	
B1	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	47 mm	
B2	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	48.7 mm	
R1, R6	SMD resistor	100 Ω	0805	2122 118 03881
R2, R3, R4, R5, R8	SMD resistor	1 Ω	0805	2122 118 04562
R7	SMD resistor	47 Ω	0805	2122 118 04598
R9	SMD resistor	1.2 kΩ	0805	2122 118 04579
P1	potentiometer	4.7 kΩ		
X1, X2	copper ribbon hairpin			
T1, T2	NPN transistor	BD139		9330 912 20112

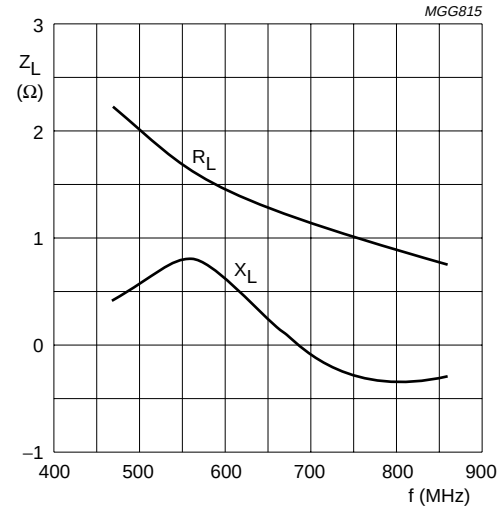
Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. American Technical Ceramics type 180R or capacitor of same quality.
4. The striplines are on a double copper-clad printed-circuit board: PTFE-glass material (TLX8) from Taconic (ε_r = 2.55); thickness 0.5 mm.



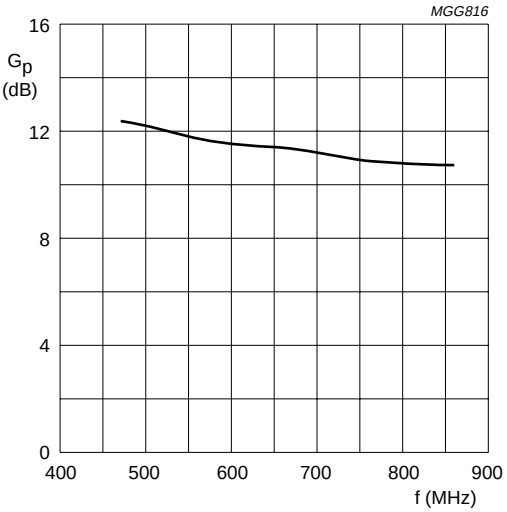
T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.8 A; P_L = 150 W (total device).

Fig.10 Input impedance (per section) as function of frequency (series components); typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.8 A; P_L = 150 W (total device).

Fig.11 Load impedance (per section) as function of frequency (series components); typical values.



T_h = 25 °C; V_{CE} = 28 V; I_{CQ} = 0.8 A; P_L = 150 W (total device).

Fig.12 Power gain as a function of frequency; typical values.

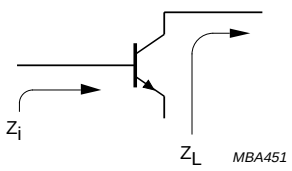
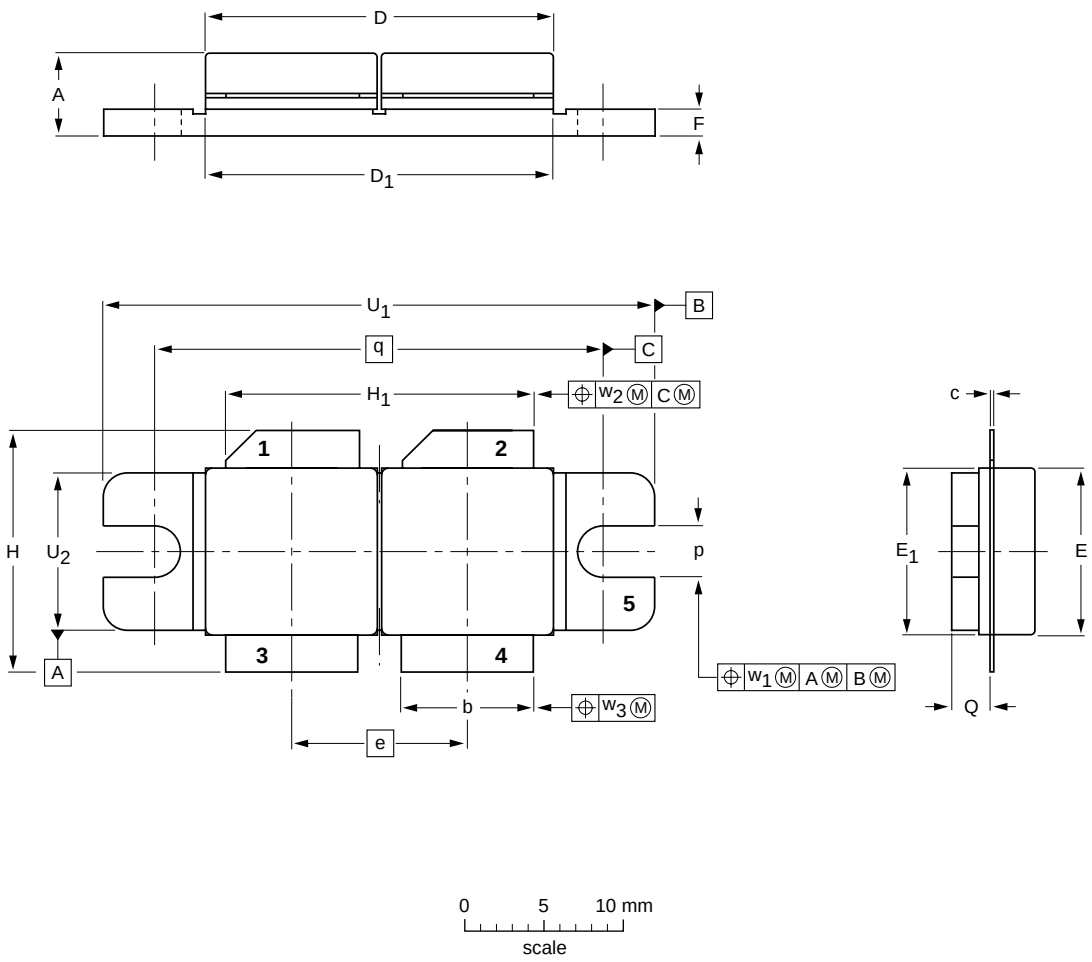


Fig.13 Definition of transistor impedance.

PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT262B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.39 4.62	8.51 8.25	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	15.49 14.99	19.69 19.17	3.28 3.02	2.47 2.20	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.212 0.182	0.335 0.325	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.61 0.59	0.775 0.755	0.129 0.119	0.097 0.087	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262B						99-03-29

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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