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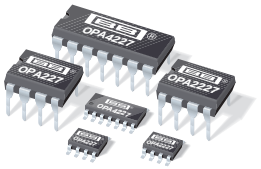
JAMECO® ELECTRONICS

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Jameco Part Number 1357327

Burr-Brown Products
from Texas Instruments



OPA227
OPA2227
OPA4227
OPA228
OPA2228
OPA4228

SBOS110A – MAY 1998 – REVISED JANUARY 2005

High Precision, Low Noise OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: 3nV/√Hz
- WIDE BANDWIDTH:
  OPA227: 8MHz, 2.3V/μs
  OPA228: 33MHz, 10V/μs
- SETTLING TIME: 5μs
  (significant improvement over OP-27)
- HIGH CMRR: 138dB
- HIGH OPEN-LOOP GAIN: 160dB
- LOW INPUT BIAS CURRENT: 10nA max
- LOW OFFSET VOLTAGE: 75μV max
- WIDE SUPPLY RANGE: ±2.5V to ±18V
- OPA227 REPLACES OP-27, LT1007, MAX427
- OPA228 REPLACES OP-37, LT1037, MAX437
- SINGLE, DUAL, AND QUAD VERSIONS

APPLICATIONS

- DATA ACQUISITION
- TELECOM EQUIPMENT
- GEOPHYSICAL ANALYSIS
- VIBRATION ANALYSIS
- SPECTRAL ANALYSIS
- PROFESSIONAL AUDIO EQUIPMENT
- ACTIVE FILTERS
- POWER SUPPLY CONTROL

SPICE model available for OPA227 at www.ti.com

DESCRIPTION

The OPA227 and OPA228 series op amps combine low noise and wide bandwidth with high precision to make them the ideal choice for applications requiring both ac and precision dc performance.

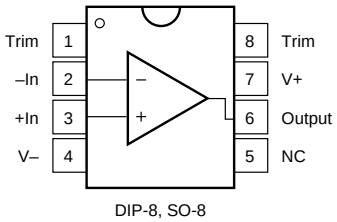
The OPA227 is unity-gain stable and features high slew rate (2.3V/μs) and wide bandwidth (8MHz). The OPA228 is optimized for closed-loop gains of 5 or greater, and offers higher speed with a slew rate of 10V/μs and a bandwidth of 33MHz.

The OPA227 and OPA228 series op amps are ideal for professional audio equipment. In addition, low quiescent current and low cost make them ideal for portable applications requiring high precision.

The OPA227 and OPA228 series op amps are pin-for-pin replacements for the industry standard OP-27 and OP-37 with substantial improvements across the board. The dual and quad versions are available for space savings and per-channel cost reduction.

The OPA227, OPA228, OPA2227, and OPA2228 are available in DIP-8 and SO-8 packages. The OPA4227 and OPA4228 are available in DIP-14 and SO-14 packages with standard pin configurations. Operation is specified from –40°C to +85°C.

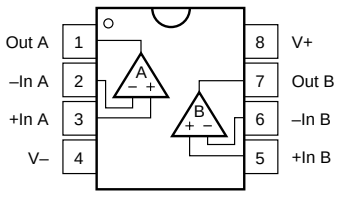
OPA227, OPA228



DIP-8, SO-8

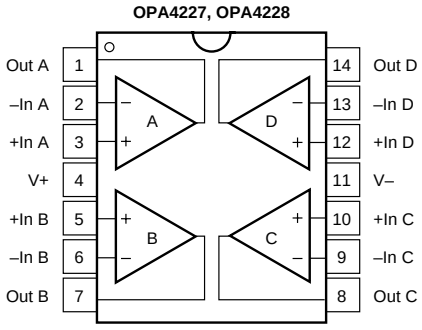
NC = Not Connected

OPA2227, OPA2228



DIP-8, SO-8

OPA4227, OPA4228



DIP-14, SO-14

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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SPECIFICATIONS: V_S = ±5V to ±15V

OPA227 Series

At T_A = +25°C, and R_L = 10kΩ, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

PARAMETER	CONDITION	OPA227P, U OPA2227P, U			OPA227PA, UA OPA2227PA, UA OPA4227PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage V_{OS}			±5	±75		±10	±200	µV
T_A = –40°C to +85°C				**±100**			**±200**	µV
vs Temperature dV_{OS}/dT			**±0.1**	**±0.6**		**±0.3**	**±2**	µV/°C
vs Power Supply PSRR	V_S = ±2.5V to ±18V		±0.5	±2		*	*	µV/V
T_A = –40°C to +85°C				**±2**			*	µV/V
vs Time			0.2			*		µV/mo
Channel Separation (dual, quad)	dc		0.2			*		µV/V
	f = 1kHz, R_L = 5kΩ		110			*		dB
INPUT BIAS CURRENT								
Input Bias Current I_B			±2.5	±10		*	*	nA
T_A = –40°C to +85°C				**±10**			*	nA
Input Offset Current I_{OS}			±2.5	±10		*	*	nA
T_A = –40°C to +85°C				**±10**			*	nA
NOISE								
Input Voltage Noise, f = 0.1Hz to 10Hz			90			*		nVp-p
			15			*		nVrms
Input Voltage Noise Density, f = 10Hz e_n			3.5			*		nV/√Hz
f = 100Hz			3			*		nV/√Hz
f = 1kHz			3			*		nV/√Hz
Current Noise Density, f = 1kHz i_n			0.4			*		pA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range V_{CM}		(V–)+2		(V+)–2	*		*	V
Common-Mode Rejection CMRR	V_{CM} = (V–)+2V to (V+)–2V	120	138		*	*		dB
T_A = –40°C to +85°C		**120**			*			dB
INPUT IMPEDANCE								
Differential			10^7 || 12			*		Ω || pF
Common-Mode	V_{CM} = (V–)+2V to (V+)–2V		10^9 || 3			*		Ω || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain A_{OL}	V_O = (V–)+2V to (V+)–2V, R_L = 10kΩ	132	160		*	*		dB
T_A = –40°C to +85°C		**132**			*			dB
	V_O = (V–)+3.5V to (V+)–3.5V, R_L = 600Ω	132	160		*	*		dB
T_A = –40°C to +85°C		**132**			*			dB
FREQUENCY RESPONSE								
Gain Bandwidth Product GBW			8			*		MHz
Slew Rate SR			2.3			*		V/µs
Settling Time: 0.1%	G = 1, 10V Step, C_L = 100pF		5			*		µs
0.01%	G = 1, 10V Step, C_L = 100pF		5.6			*		µs
Overload Recovery Time	V_{IN} • G = V_S		1.3			*		µs
Total Harmonic Distortion + Noise THD+N	f = 1kHz, G = 1, V_O = 3.5Vrms		0.00005			*		%
OUTPUT								
Voltage Output	R_L = 10kΩ	(V–)+2		(V+)–2	*		*	V
T_A = –40°C to +85°C	R_L = 10kΩ	**(V–)+2**		**(V+)–2**	*		*	V
	R_L = 600Ω	(V–)+3.5		(V+)–3.5	*		*	V
T_A = –40°C to +85°C	R_L = 600Ω	**(V–)+3.5**		**(V+)–3.5**	*		*	V
Short-Circuit Current I_{SC}			±45			*		mA
Capacitive Load Drive C_{LOAD}			See Typical Curve			*		
POWER SUPPLY								
Specified Voltage Range V_S		±5		±15	*		*	V
Operating Voltage Range		±2.5		±18	*		*	V
Quiescent Current (per amplifier) I_Q	I_O = 0		±3.7	±3.8		*	*	mA
T_A = –40°C to +85°C	I_O = 0			**±4.2**			*	mA
TEMPERATURE RANGE								
Specified Range		–40		+85	*		*	°C
Operating Range		–55		+125	*		*	°C
Storage Range		–65		+150	*		*	°C
Thermal Resistance θ_{JA}								
SO-8 Surface Mount			150			*		°C/W
DIP-8			100			*		°C/W
DIP-14			80			*		°C/W
SO-14 Surface Mount			100			*		°C/W

* Specifications same as OPA227P, U.

SPECIFICATIONS: V_S = ±5V to ±15V

OPA228 Series

At T_A = +25°C, and R_L = 10kΩ, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

PARAMETER	CONDITION	OPA228P, U OPA2228P, U			OPA228PA, UA OPA2228PA, UA OPA4228PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage V_{OS}			±5	±75		±10	±200	µV
T_A = –40°C to +85°C				**±100**			**±200**	µV
vs Temperature dV_{OS}/dT			**±0.1**	**±0.6**		**±0.3**	**±2**	µV/°C
vs Power Supply PSRR	V_S = ±2.5V to ±18V		±0.5	±2		*	*	µV/V
T_A = –40°C to +85°C				**±2**			*	µV/V
vs Time			0.2			*		µV/mo
Channel Separation (dual, quad)	dc		0.2			*		µV/V
	f = 1kHz, R_L = 5kΩ		110			*		dB
INPUT BIAS CURRENT								
Input Bias Current I_B			±2.5	±10		*	*	nA
T_A = –40°C to +85°C				**±10**			*	nA
Input Offset Current I_{OS}			±2.5	±10		*	*	nA
T_A = –40°C to +85°C				**±10**			*	nA
NOISE								
Input Voltage Noise, f = 0.1Hz to 10Hz			90			*		nVp-p
			15			*		nVrms
Input Voltage Noise Density, f = 10Hz e_n			3.5			*		nV/√Hz
f = 100Hz			3			*		nV/√Hz
f = 1kHz			3			*		nV/√Hz
Current Noise Density, f = 1kHz i_n			0.4			*		pA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range V_{CM}		(V–)+2		(V+)–2	*		*	V
Common-Mode Rejection CMRR	V_{CM} = (V–)+2V to (V+)–2V	120	138		*	*		dB
T_A = –40°C to +85°C		**120**			*			dB
INPUT IMPEDANCE								
Differential			10^7 || 12			*		Ω || pF
Common-Mode	V_{CM} = (V–)+2V to (V+)–2V		10^9 || 3			*		Ω || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain A_{OL}	V_O = (V–)+2V to (V+)–2V, R_L = 10kΩ	132	160		*	*		dB
T_A = –40°C to +85°C		**132**			*			dB
	V_O = (V–)+3.5V to (V+)–3.5V, R_L = 600Ω	132	160		*	*		dB
T_A = –40°C to +85°C		**132**			*			dB
FREQUENCY RESPONSE								
Minimum Closed-Loop Gain			5			*		V/V
Gain Bandwidth Product GBW			33			*		MHz
Slew Rate SR			11			*		V/µs
Settling Time: 0.1%	G = 5, 10V Step, C_L = 100pF, C_F =12pF		1.5			*		µs
0.01%	G = 5, 10V Step, C_L = 100pF, C_F =12pF		2			*		µs
Overload Recovery Time	V_{IN} • G = V_S		0.6			*		µs
Total Harmonic Distortion + Noise THD+N	f = 1kHz, G = 5, V_O = 3.5Vrms		0.00005			*		%
OUTPUT								
Voltage Output	R_L = 10kΩ	(V–)+2		(V+)–2	*		*	V
T_A = –40°C to +85°C	R_L = 10kΩ	**(V–)+2**		**(V+)–2**	*		*	V
	R_L = 600Ω	(V–)+3.5		(V+)–3.5	*		*	V
T_A = –40°C to +85°C	R_L = 600Ω	**(V–)+3.5**		**(V+)–3.5**	*		*	V
Short-Circuit Current I_{SC}			±45			*		mA
Capacitive Load Drive C_{LOAD}	See Typical Curve					*		
POWER SUPPLY								
Specified Voltage Range V_S		±5		±15	*		*	V
Operating Voltage Range		±2.5		±18	*		*	V
Quiescent Current (per amplifier) I_Q	I_O = 0		±3.7	±3.8		*	*	mA
T_A = –40°C to +85°C	I_O = 0			**±4.2**			*	mA
TEMPERATURE RANGE								
Specified Range		–40		+85	*		*	°C
Operating Range		–55		+125	*		*	°C
Storage Range		–65		+150	*		*	°C
Thermal Resistance θ_{JA}								
SO-8 Surface Mount			150			*		°C/W
DIP-8			100			*		°C/W
DIP-14			80			*		°C/W
SO-14 Surface Mount			100			*		°C/W

* Specifications same as OPA228P, U.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Signal Input Terminals, Voltage	(V–) –0.7V to (V+) +0.7V
Current	20mA
Output Short-Circuit[2]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet, or refer to our web site at www.ti.com.

ELECTROSTATIC DISCHARGE SENSITIVITY

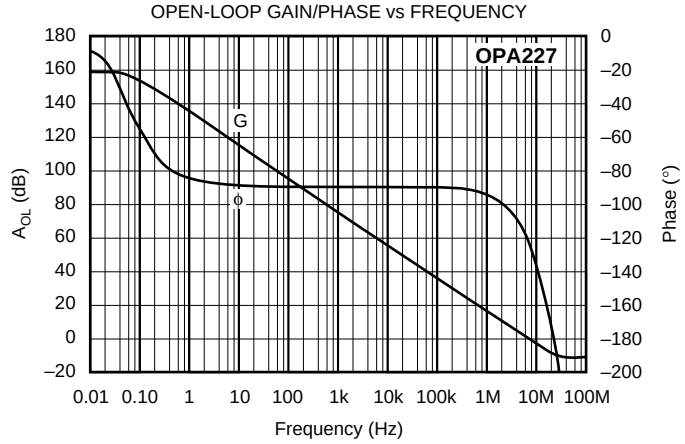
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

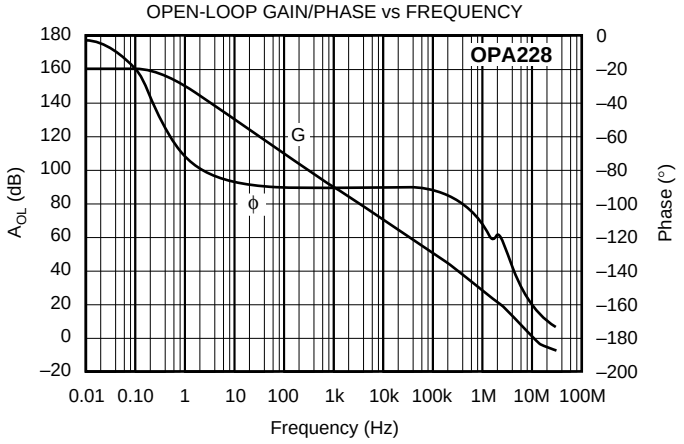
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, R_L = 10kΩ, and V_S = ±15V, unless otherwise noted.

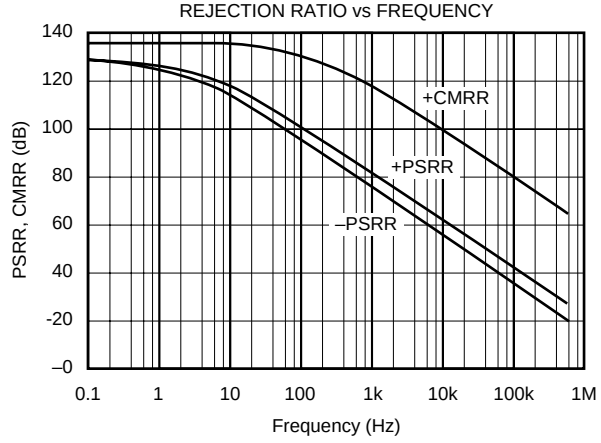
OPEN-LOOP GAIN/PHASE vs FREQUENCY



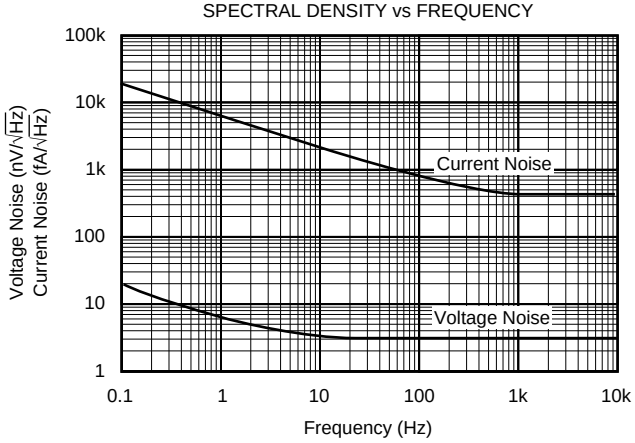
OPEN-LOOP GAIN/PHASE vs FREQUENCY



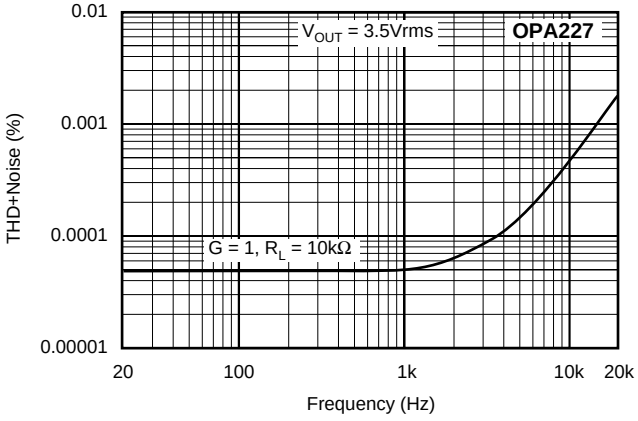
POWER SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY



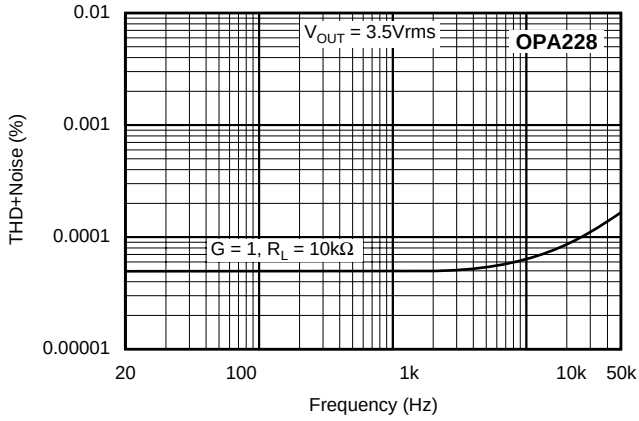
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



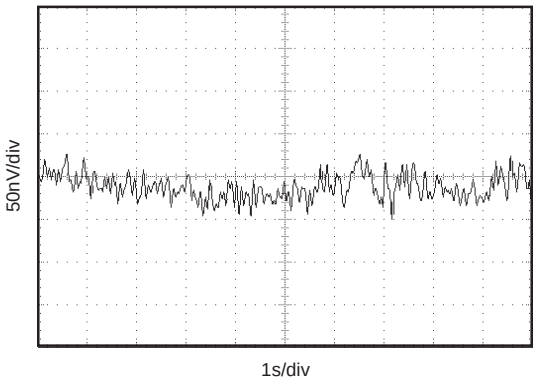
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



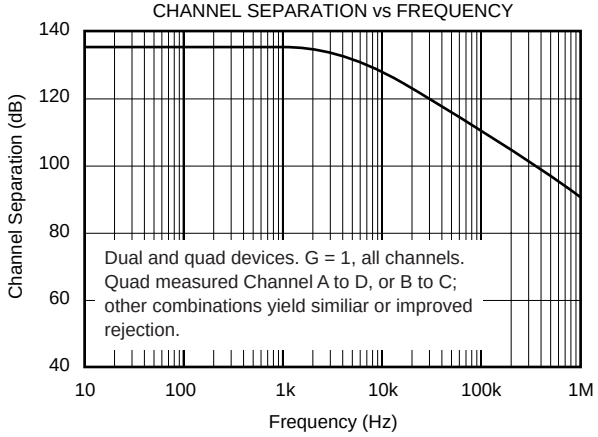
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, R_L =10kΩ, and V_S = ±15V, unless otherwise noted.

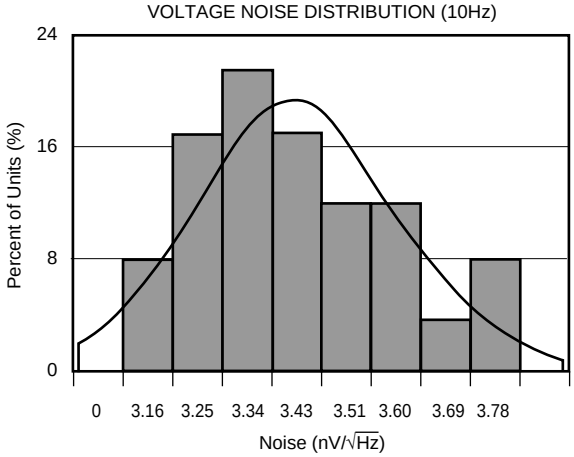
INPUT NOISE VOLTAGE vs TIME



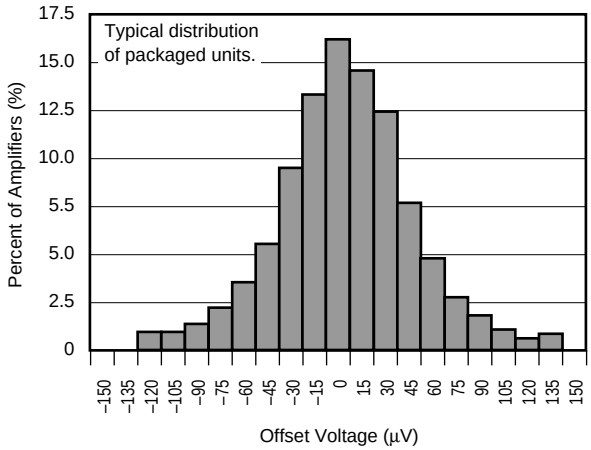
CHANNEL SEPARATION vs FREQUENCY



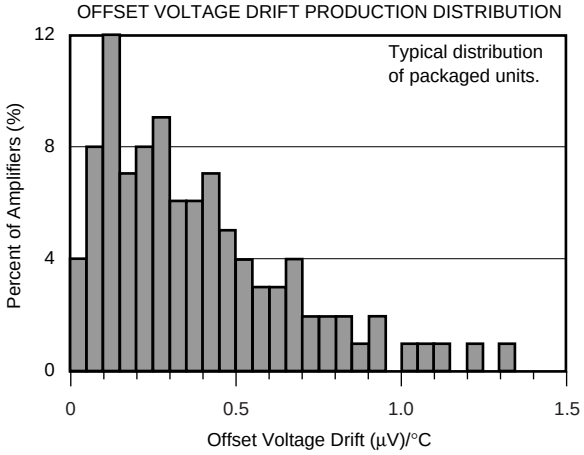
VOLTAGE NOISE DISTRIBUTION (10Hz)



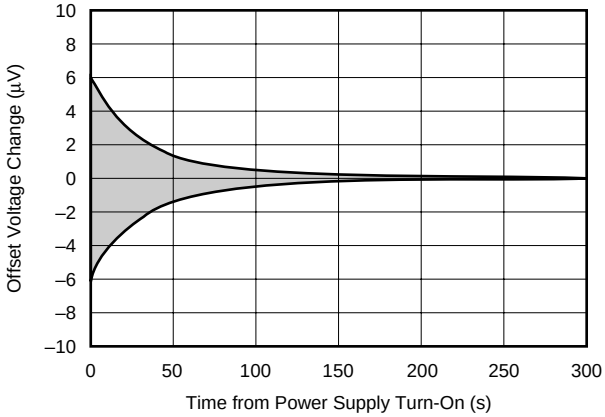
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



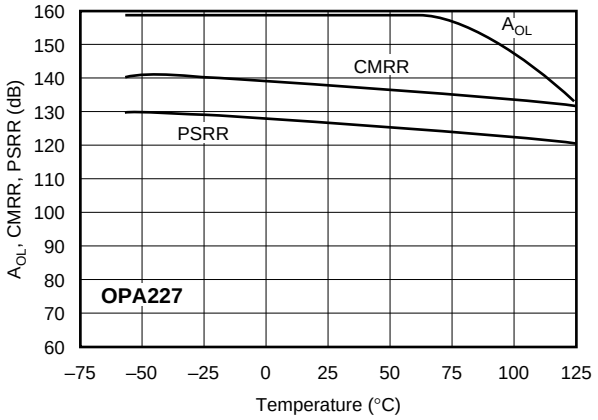
WARM-UP OFFSET VOLTAGE DRIFT



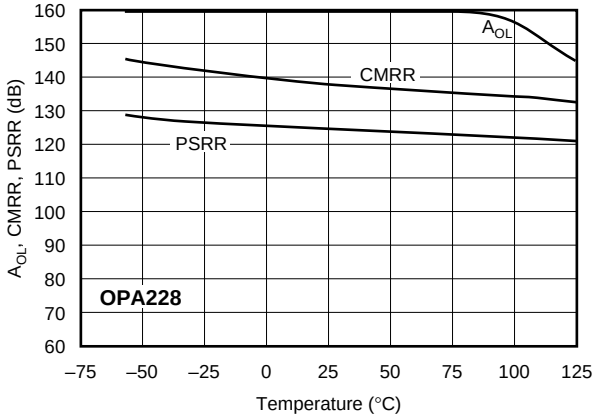
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, R_L = 10kΩ, and V_S = ±15V, unless otherwise noted.

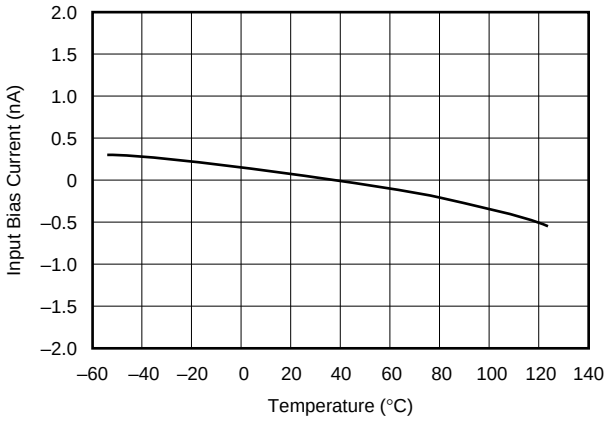
A_{OL}, CMRR, PSRR vs TEMPERATURE



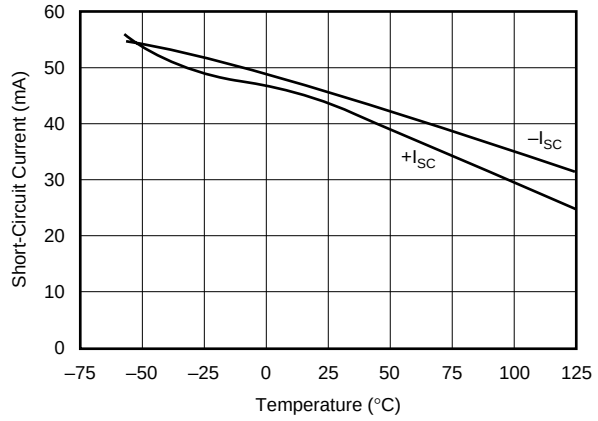
A_{OL}, CMRR, PSRR vs TEMPERATURE



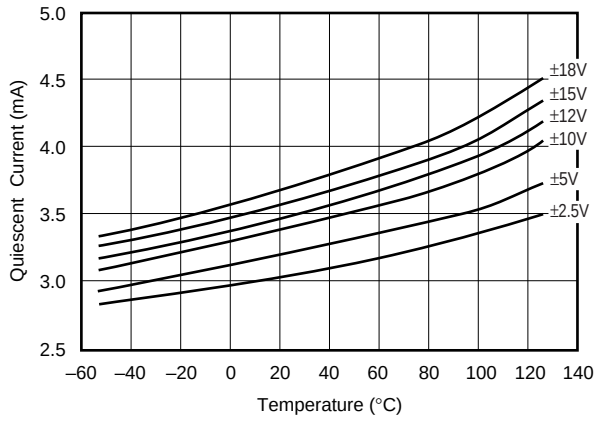
INPUT BIAS CURRENT vs TEMPERATURE



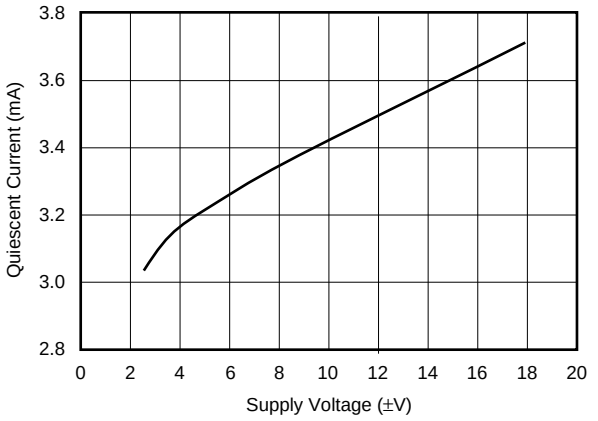
SHORT-CIRCUIT CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



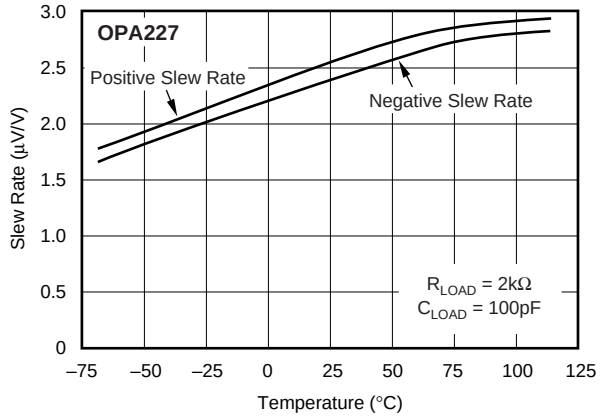
QUIESCENT CURRENT vs SUPPLY VOLTAGE



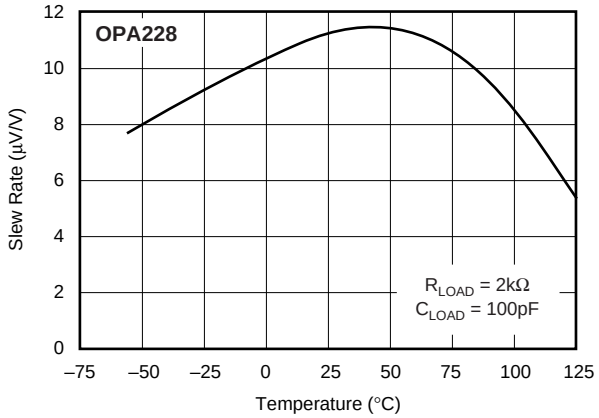
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, R_L = 10kΩ, and V_S = ±15V, unless otherwise noted.

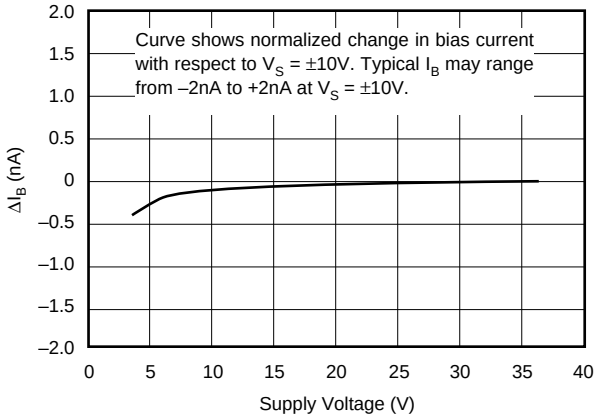
SLEW RATE vs TEMPERATURE



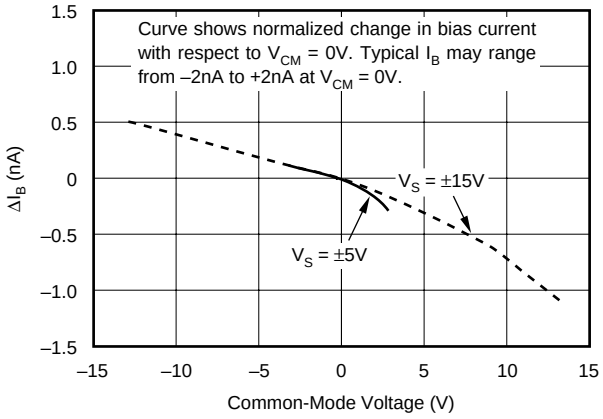
SLEW RATE vs TEMPERATURE



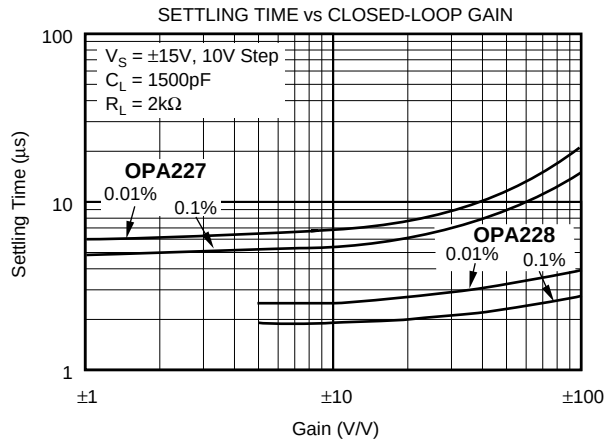
CHANGE IN INPUT BIAS CURRENT vs POWER SUPPLY VOLTAGE



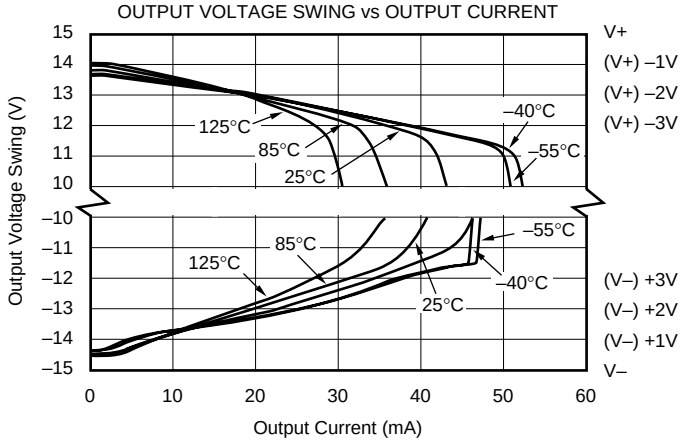
CHANGE IN INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



SETTLING TIME vs CLOSED-LOOP GAIN



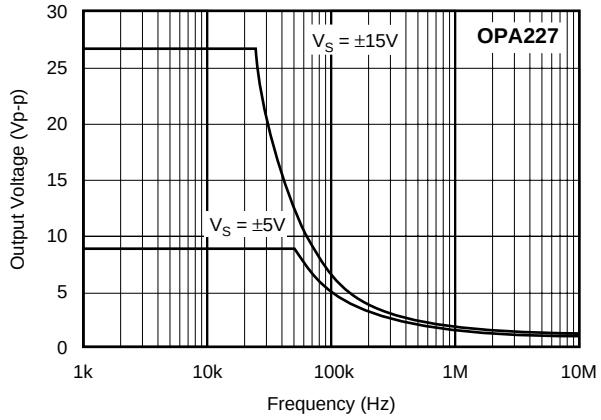
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



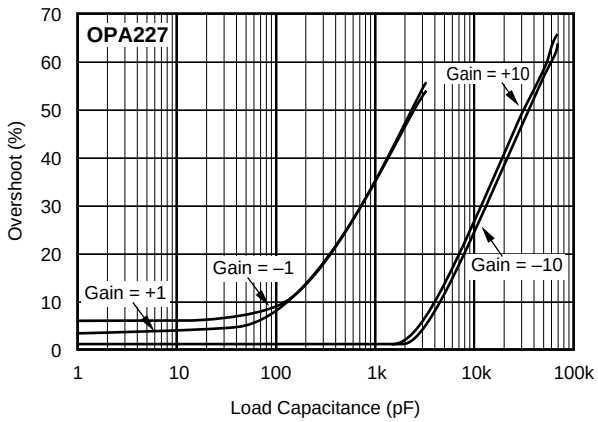
TYPICAL PERFORMANCE CURVES (CONT)

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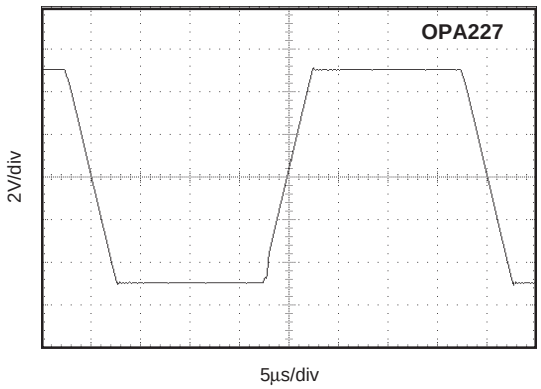
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



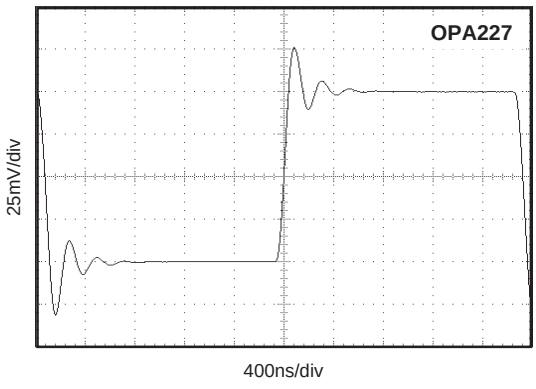
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



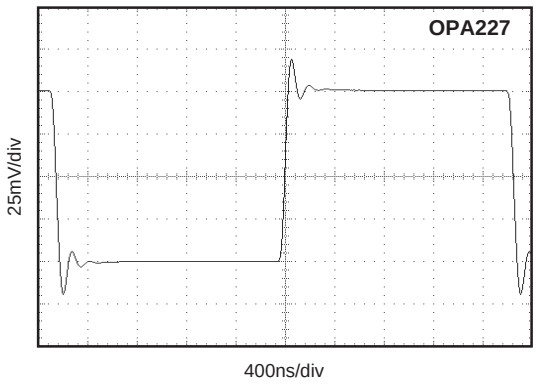
LARGE-SIGNAL STEP RESPONSE
G = –1, C_L = 1500pF



SMALL-SIGNAL STEP RESPONSE
G = +1, C_L = 1000pF



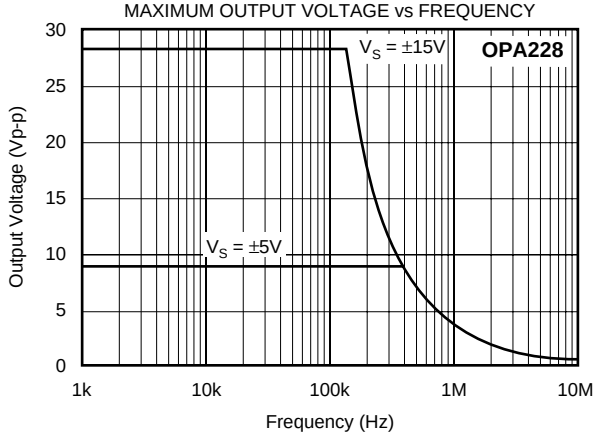
SMALL-SIGNAL STEP RESPONSE
G = +1, C_L = 5pF



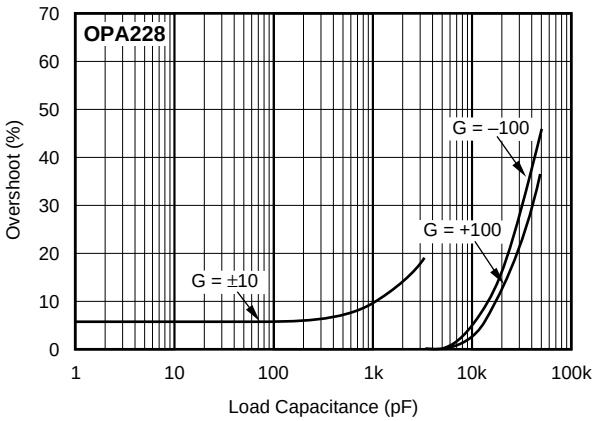
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, R_L = 10kΩ, and V_S = ±15V, unless otherwise noted.

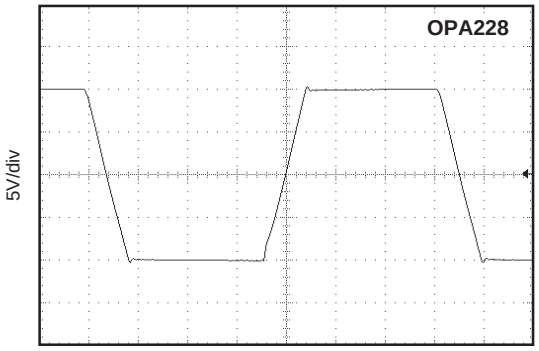
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



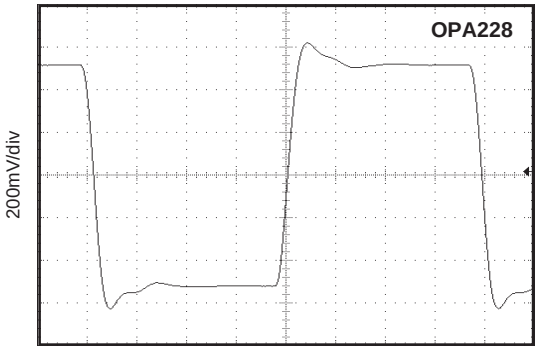
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



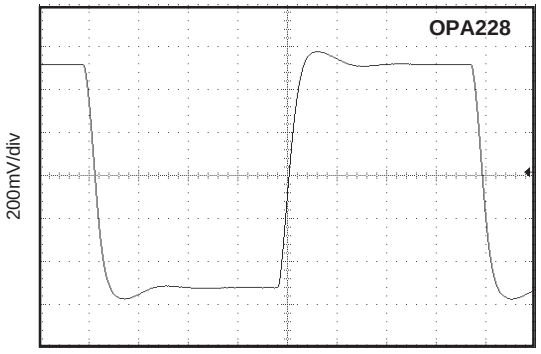
LARGE-SIGNAL STEP RESPONSE
G = –10, C_L = 100pF



SMALL-SIGNAL STEP RESPONSE
G = +10, C_L = 1000pF, R_L = 1.8kΩ



SMALL-SIGNAL STEP RESPONSE
G = +10, C_L = 5pF, R_L = 1.8kΩ



APPLICATIONS INFORMATION

The OPA227 and OPA228 series are precision op amps with very low noise. The OPA227 series is unity-gain stable with a slew rate of 2.3V/µs and 8MHz bandwidth. The OPA228 series is optimized for higher-speed applications with gains of 5 or greater, featuring a slew rate of 10V/µs and 33MHz bandwidth. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate.

OFFSET VOLTAGE AND DRIFT

The OPA227 and OPA228 series have very low offset voltage and drift. To achieve highest dc precision, circuit layout and mechanical conditions should be optimized. Connections of dissimilar metals can generate thermal potentials at the op amp inputs which can degrade the offset voltage and drift. These thermocouple effects can exceed the inherent drift of the amplifier and ultimately degrade its performance. The thermal potentials can be made to cancel by assuring that they are equal at both input terminals. In addition:

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield op amp and input circuitry from air currents such as those created by cooling fans.

OPERATING VOLTAGE

OPA227 and OPA228 series op amps operate from ±2.5V to ±18V supplies with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA227 series is specified for real-world applications; a single set of specifications applies over the ±5V to ±15V supply range. Specifications are assured for applications between ±5V and ±15V power supplies. Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPA227 and OPA228 series can operate with as little as 5V between the supplies and with up to 36V between the supplies. For example, the positive supply could be set to 25V with the negative supply at –5V or vice-versa. In addition, key parameters are assured over the specified temperature range, –40°C to +85°C. Parameters which vary significantly with operating voltage or temperature are shown in the Typical Performance Curves.

OFFSET VOLTAGE ADJUSTMENT

The OPA227 and OPA228 series are laser-trimmed for very low offset and drift so most applications will not require external adjustment. However, the OPA227 and OPA228 (single versions) provide offset voltage trim connections on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp. This adjustment should not be used to compensate for offsets created elsewhere in the system since this can introduce additional temperature drift.

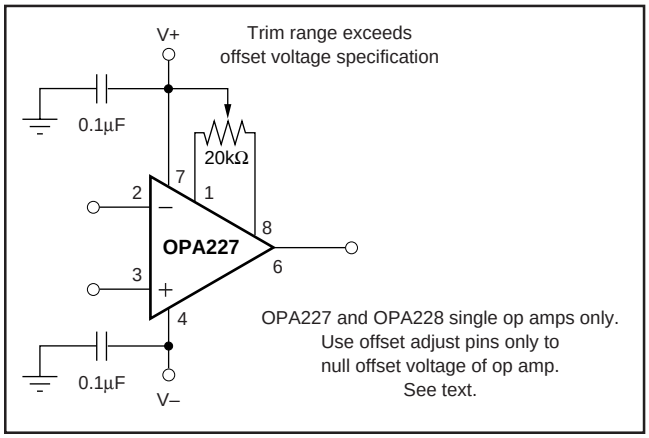


FIGURE 1. OPA227 Offset Voltage Trim Circuit.

INPUT PROTECTION

Back-to-back diodes (see Figure 2) are used for input protection on the OPA227 and OPA228. Exceeding the turn-on threshold of these diodes, as in a pulse condition, can cause current to flow through the input protection diodes due to the amplifier's finite slew rate. Without external current-limiting resistors, the input devices can be destroyed. Sources of high input current can cause subtle damage to the amplifier. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may shift.

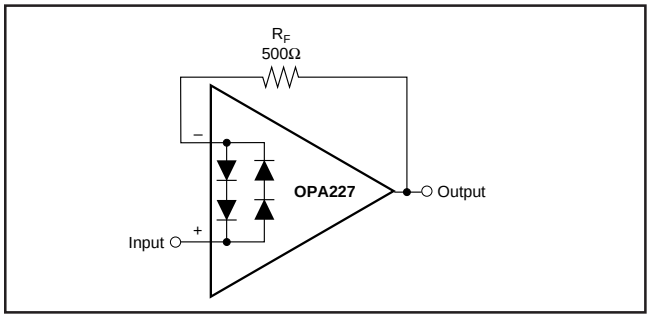


FIGURE 2. Pulsed Operation.

When using the OPA227 as a unity-gain buffer (follower), the input current should be limited to 20mA. This can be accomplished by inserting a feedback resistor or a resistor in series with the source. Sufficient resistor size can be calculated:

$$R_X = V_S/20mA - R_{SOURCE}$$

where R_X is either in series with the source or inserted in the feedback path. For example, for a 10V pulse (V_S = 10V), total loop resistance must be 500Ω. If the source impedance is large enough to sufficiently limit the current on its own, no additional resistors are needed. The size of any external resistors must be carefully chosen since they will increase noise. See the Noise Performance section of this data sheet for further information on noise calculation. Figure 2 shows an example implementing a current-limiting feedback resistor.

INPUT BIAS CURRENT CANCELLATION

The input bias current of the OPA227 and OPA228 series is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between with input bias current and the cancellation current. The residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately equal. A resistor added to cancel the effect of the input bias current (as shown in Figure 3) may actually increase offset and noise and is therefore not recommended.

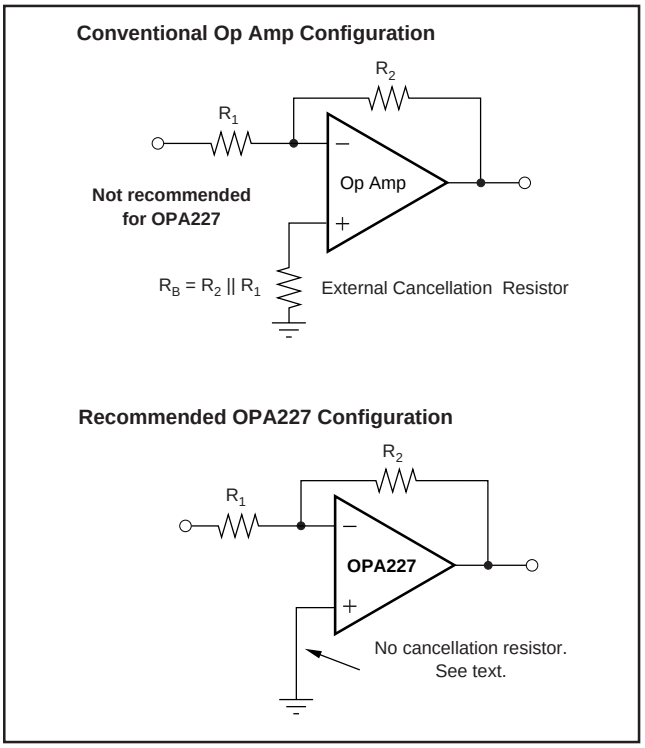


FIGURE 3. Input Bias Current Cancellation.

NOISE PERFORMANCE

Figure 4 shows total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, therefore no additional noise contributions). Two different op amps are shown with total circuit noise calculated. The OPA227 has very low voltage noise, making it ideal for low source impedances (less than 20kΩ). A similar precision op amp, the OPA277, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10kΩ to 100kΩ). Above 100kΩ, a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation is shown for the calculation of the total circuit noise. Note that e_n = voltage noise, i_n = current noise, R_S = source impedance, k = Boltzmann's constant = $1.38 \cdot 10^{-23}$ J/K and T is temperature in K. For more details on calculating noise, see the insert titled "Basic Noise Calculations."

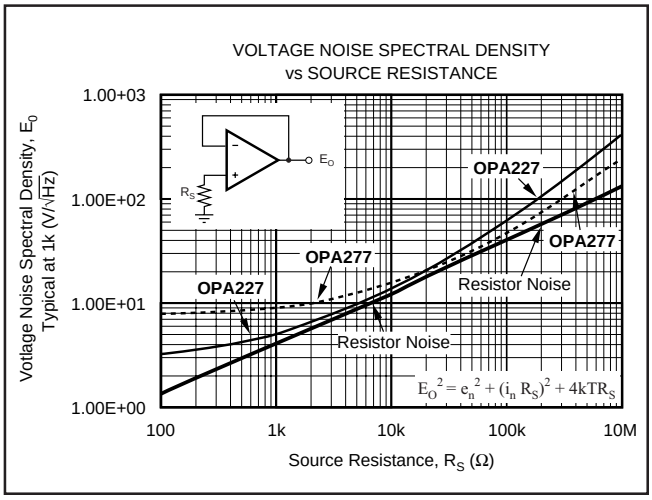


FIGURE 4. Noise Performance of the OPA227 in Unity-Gain Buffer Configuration.

BASIC NOISE CALCULATIONS

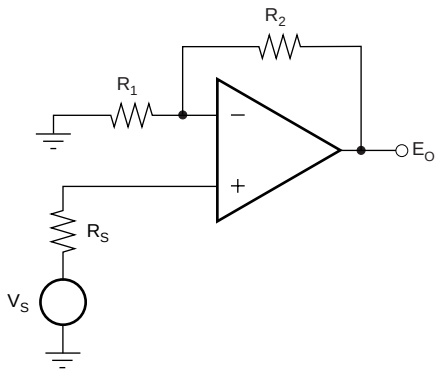
Design of low noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is shown plotted in Figure 4. Since the source impedance is usually fixed, select the op amp and the feedback resistors to minimize their contribution to the total noise.

Figure 4 shows total noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Consequently, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 5 shows both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

Noise in Noninverting Gain Configuration



Noise at the output:

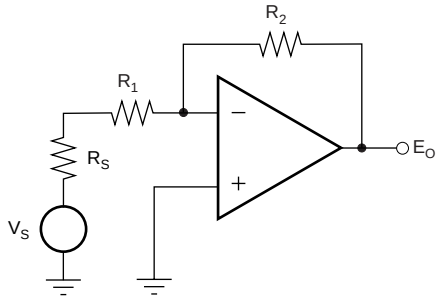
$$E_O^2 = \left(1+\frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2\left(1+\frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \bullet \left(1+\frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \bullet \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1+\frac{R_2}{R_1+R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \bullet \left(\frac{R_2}{R_1+R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \bullet \left(\frac{R_2}{R_1+R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA227 and OPA228 series op amps at 1kHz, $e_n = 3nV/\sqrt{Hz}$ and $i_n = 0.4pA/\sqrt{Hz}$.

FIGURE 5. Noise Calculation in Gain Configurations.

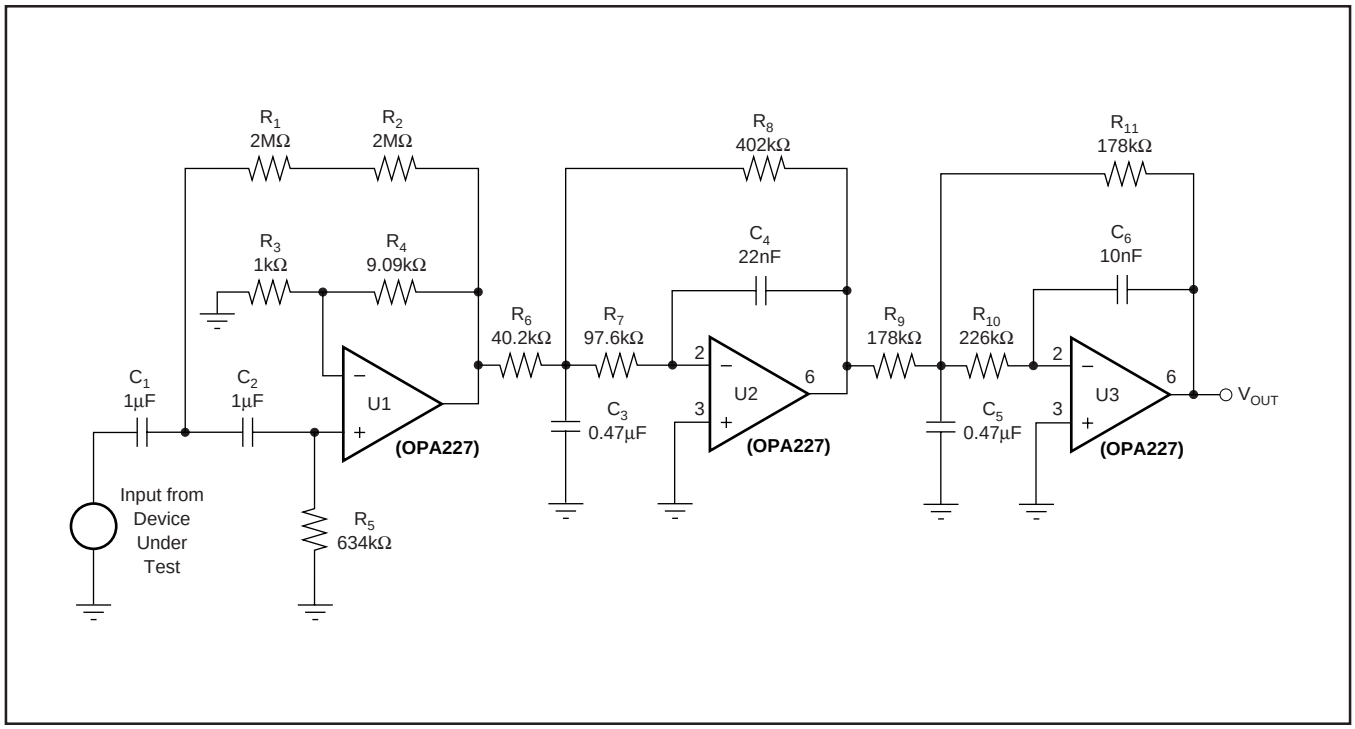


FIGURE 6. 0.1Hz to 10Hz Bandpass Filter Used to Test Wideband Noise of the OPA227 and OPA228 Series.

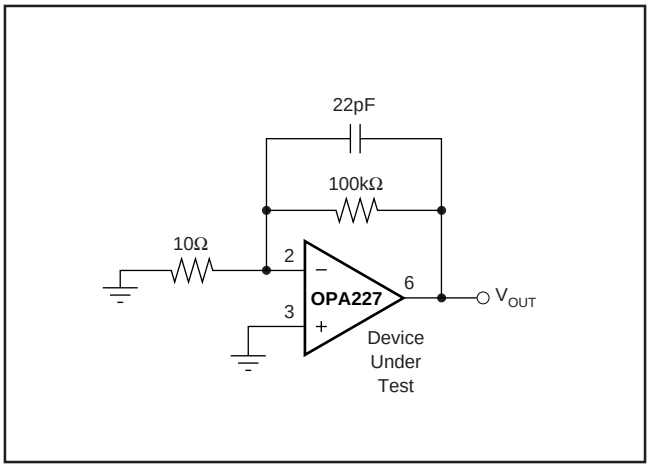


FIGURE 7. Noise Test Circuit.

Figure 6 shows the 0.1Hz 10Hz bandpass filter used to test the noise of the OPA227 and OPA228. The filter circuit was designed using Texas Instruments' FilterPro software (available at www.ti.com). Figure 7 shows the configuration of the OPA227 and OPA228 for noise testing.

USING THE OPA228 IN LOW GAINS

The OPA228 family is intended for applications with signal gains of 5 or greater, but it is possible to take advantage of their high speed in lower gains. Without external compensation, the OPA228 has sufficient phase margin to maintain stability in unity gain with purely resistive loads. However, the addition of load capacitance can reduce the phase margin and destabilize the op amp.

A variety of compensation techniques have been evaluated specifically for use with the OPA228. The recommended configuration consists of an additional capacitor (C_F) in parallel with the feedback resistance, as shown in Figures 8 and 11. This feedback capacitor serves two purposes in compensating the circuit. The op amp's input capacitance and the feedback resistors interact to cause phase shift that can result in instability. C_F compensates the input capacitance, minimizing peaking. Additionally, at high frequencies, the closed-loop gain of the amplifier is strongly influenced by the ratio of the input capacitance and the feedback capacitor. Thus, C_F can be selected to yield good stability while maintaining high speed.

Without external compensation, the noise specification of the OPA228 is the same as that for the OPA227 in gains of 5 or greater. With the additional external compensation, the output noise of the of the OPA228 will be higher. The amount of noise increase is directly related to the increase in high frequency closed-loop gain established by the C_{IN}/C_F ratio.

Figures 8 and 11 show the recommended circuit for gains of +2 and –2, respectively. The figures suggest approximate values for C_F. Because compensation is highly dependent on circuit design, board layout, and load conditions, C_F should be optimized experimentally for best results. Figures 9 and 10 show the large- and small-signal step responses for the G = +2 configuration with 100pF load capacitance. Figures 12 and 13 show the large- and small-signal step responses for the G = –2 configuration with 100pF load capacitance.

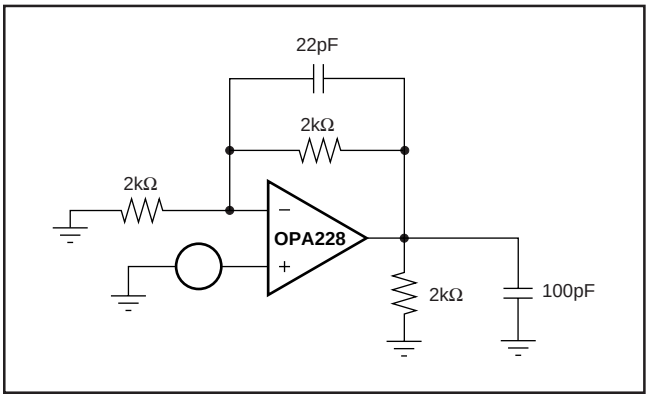


FIGURE 8. Compensation of the OPA228 for G =+2.

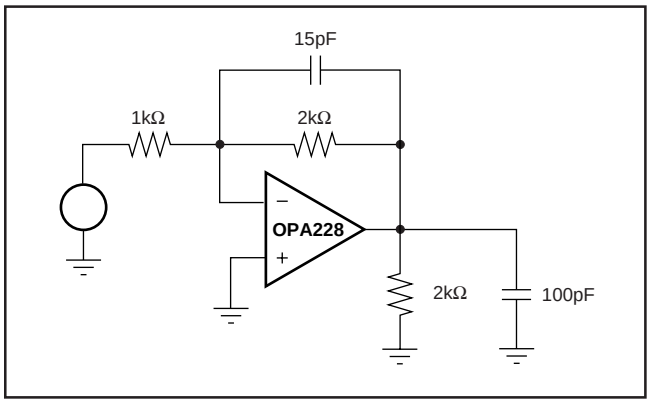


FIGURE 11. Compensation for OPA228 for G = –2.

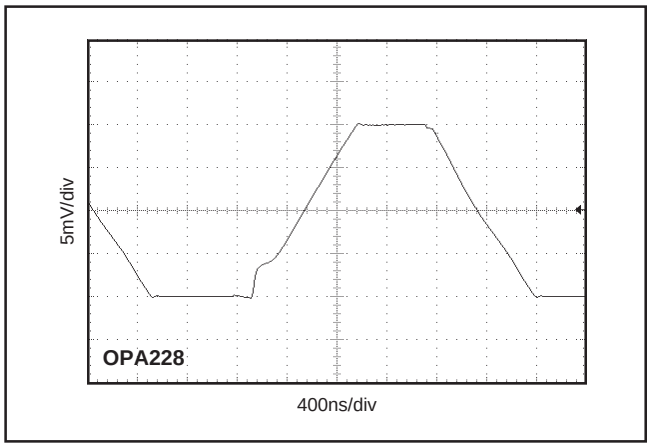


FIGURE 9. Large-Signal Step Response, G = +2, C_{LOAD} = 100pF, Input Signal = 5Vp-p.

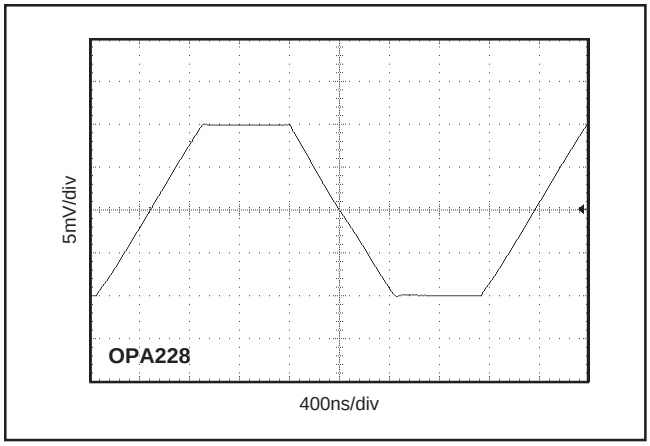


FIGURE 12. Large-Signal Step Response, G = –2, C_{LOAD} = 100pF, Input Signal = 5Vp-p.

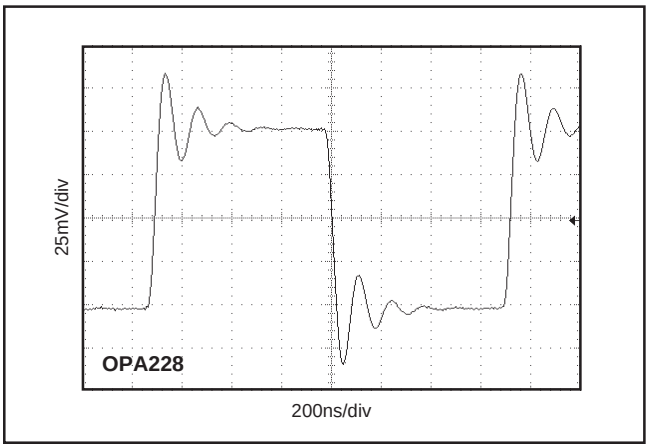


FIGURE 10. Small-Signal Step Response, G = +2, C_{LOAD} = 100pF, Input Signal = 50mVp-p.

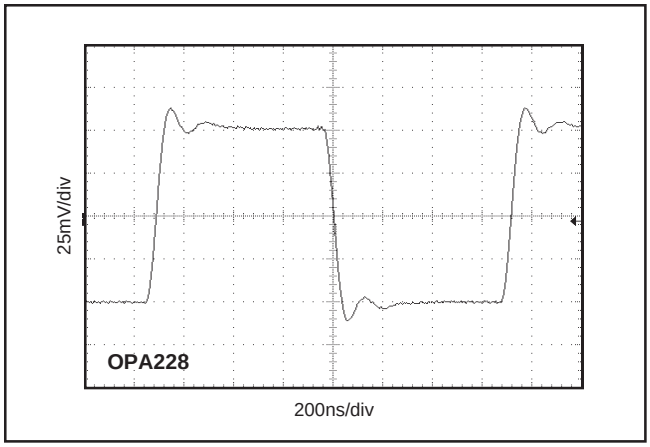


FIGURE 13. Small-Signal Step Response, G = –2, C_{LOAD} = 100pF, Input Signal = 50mVp-p.

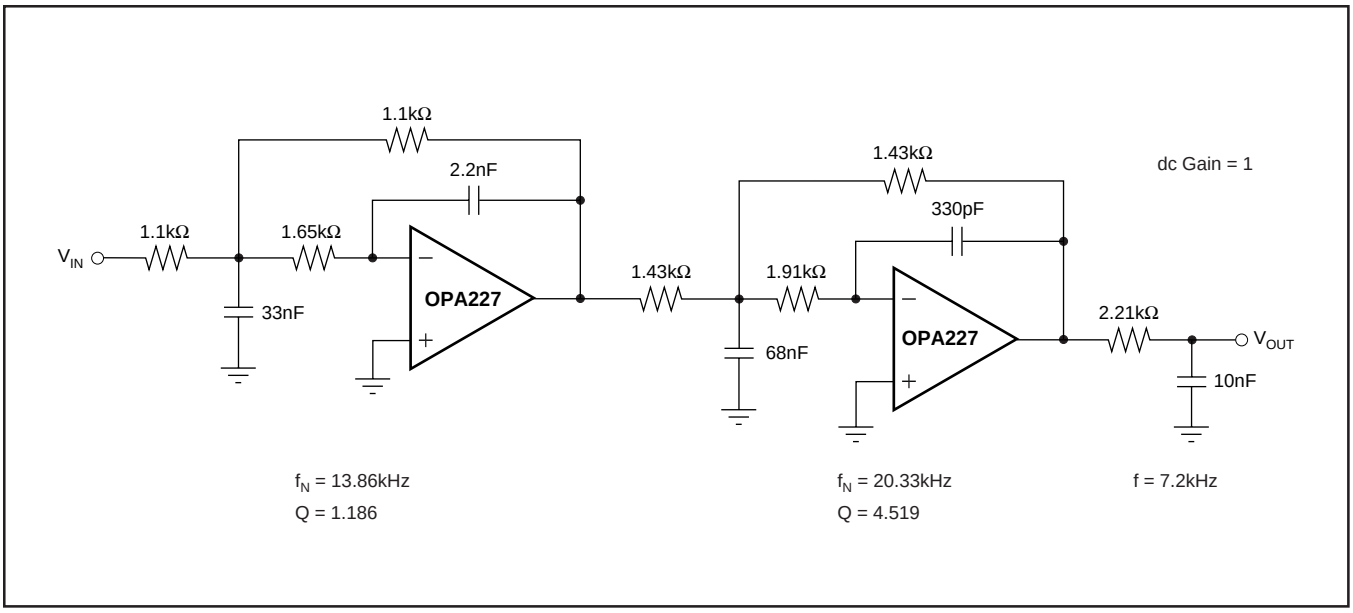


FIGURE 14. Three-Pole, 20kHz Low Pass, 0.5dB Chebyshev Filter.

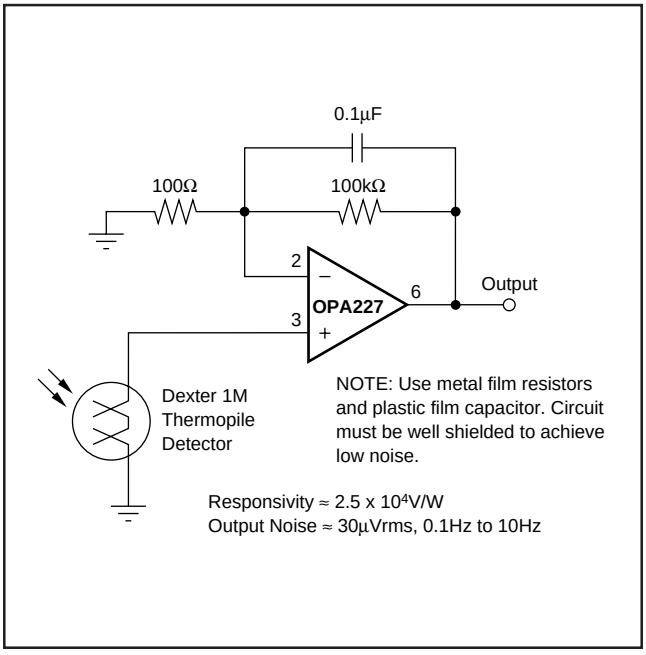


FIGURE 15. Long-Wavelength Infrared Detector Amplifier.

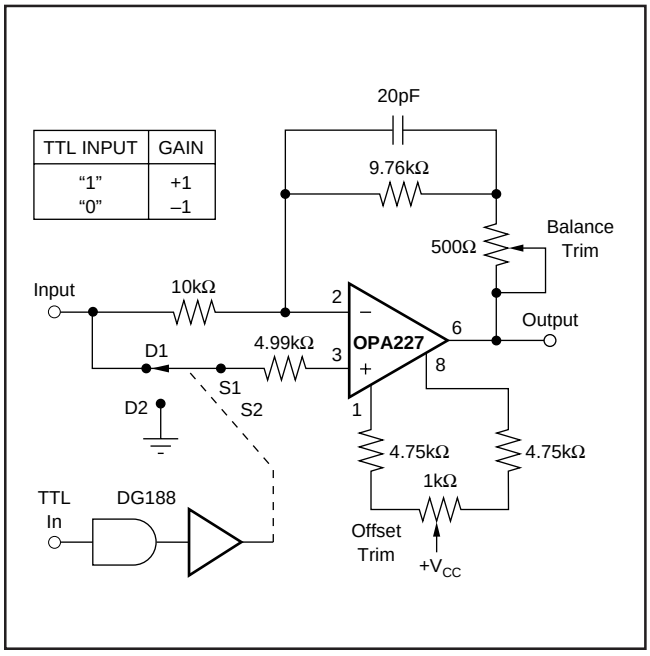


FIGURE 16. High Performance Synchronous Demodulator.

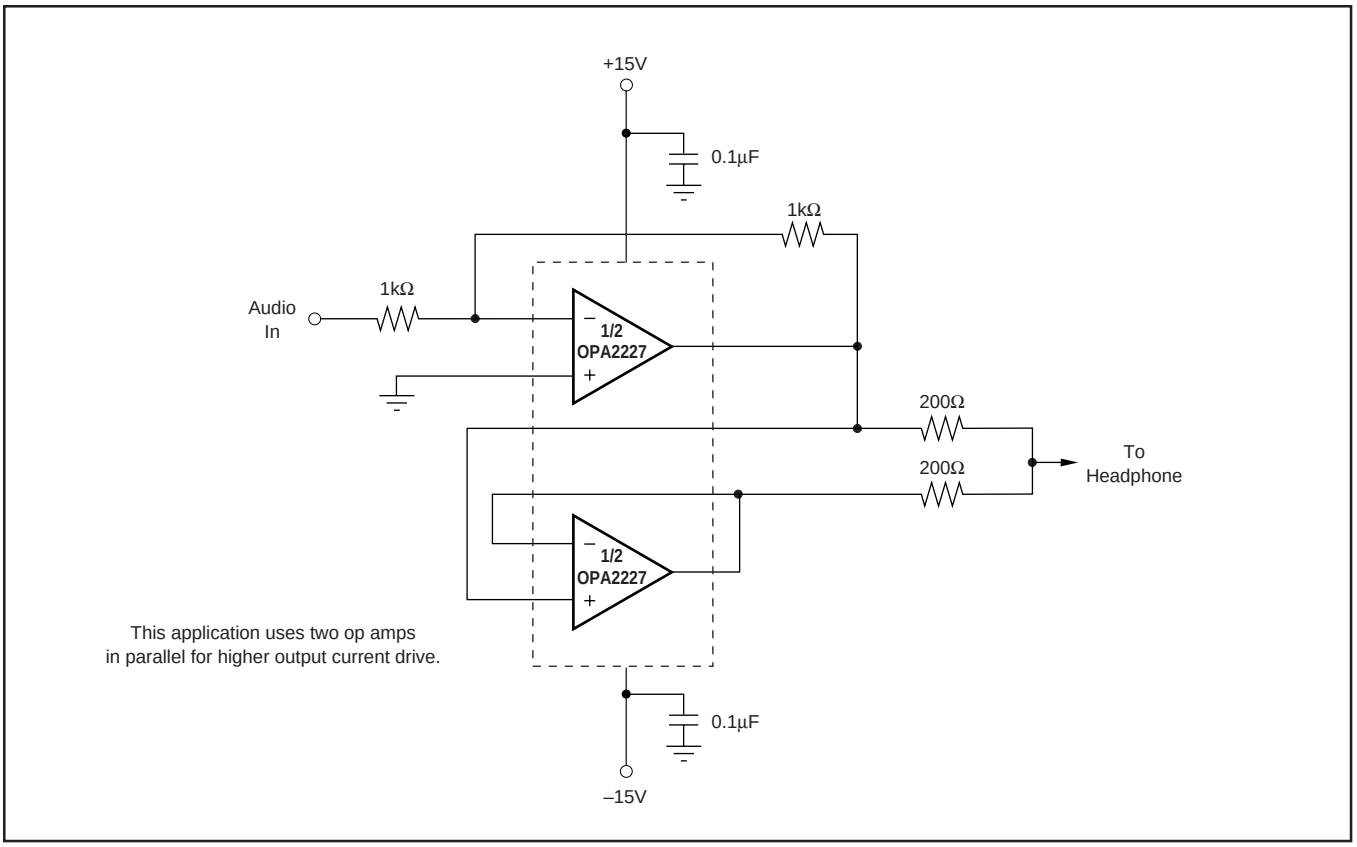


FIGURE 17. Headphone Amplifier.

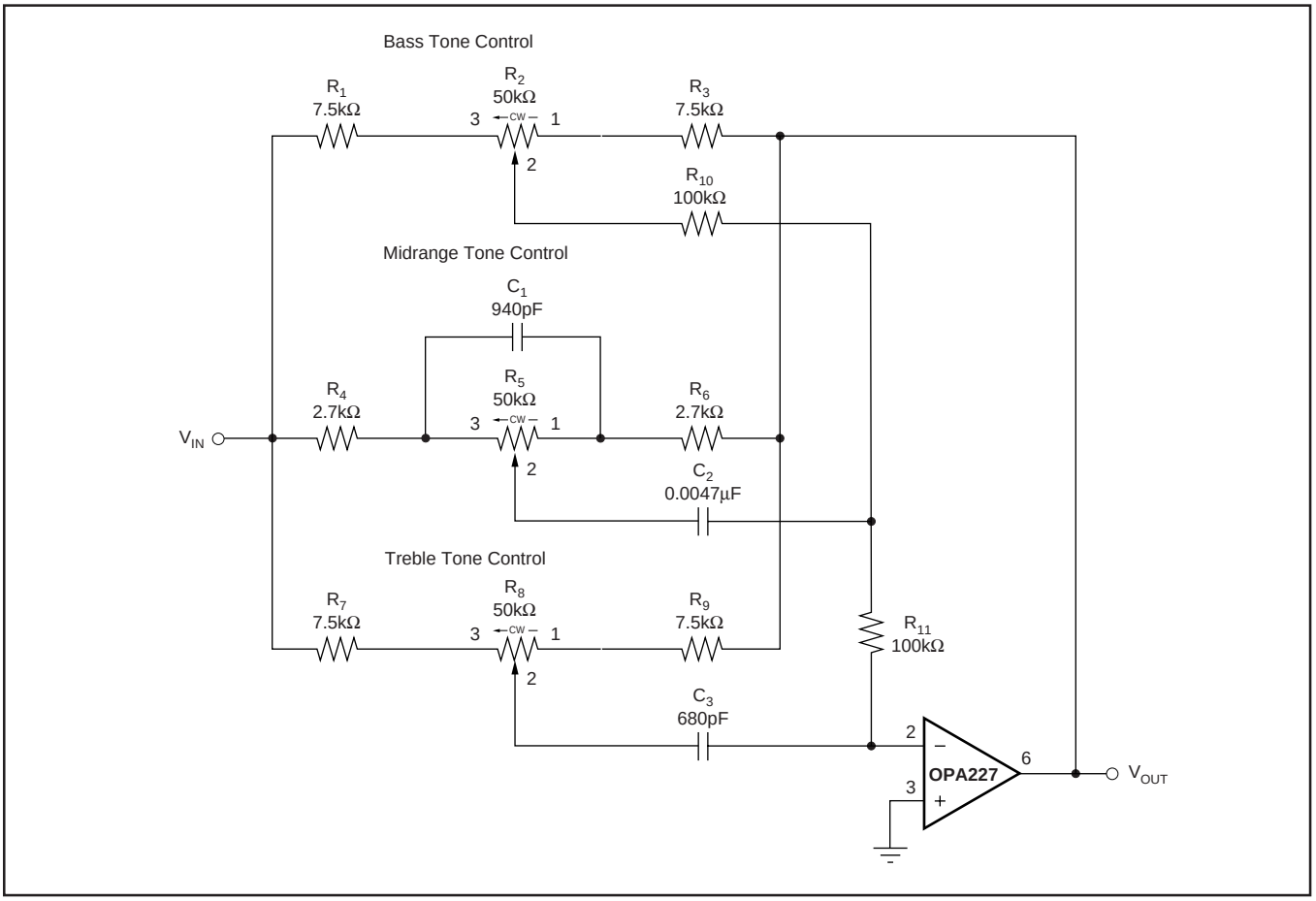


FIGURE 18. Three-Band ActiveTone Control (bass, midrange and treble).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA2227P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2227PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2227PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2227PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2227U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2227U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2227U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2227UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2227UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2227UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2227UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2227UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2227UE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2227UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2228P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2228PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2228PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2228PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2228U	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2228U/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2228U/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2228UA	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2228UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2228UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2228UAE4	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA2228UE4	ACTIVE	SOIC	D	8	100	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA227P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA227PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA227PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA227PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA227U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA227U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA227U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA227UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA227UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA227UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA227UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA227UE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA228P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA228PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA228PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA228PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA228U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA228UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA228UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA228UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA228UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA228UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4227PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4227PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4227UA	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA4227UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4227UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4227UAG4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4228PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4228PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4228UA	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4228UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4228UAE4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

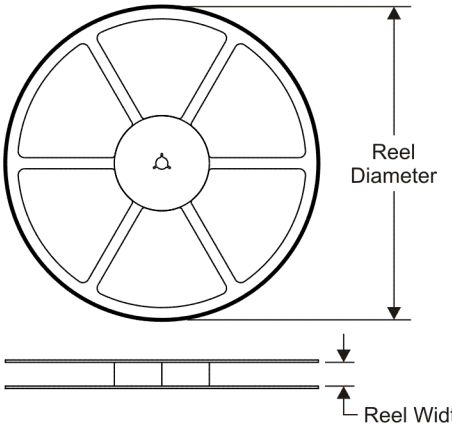
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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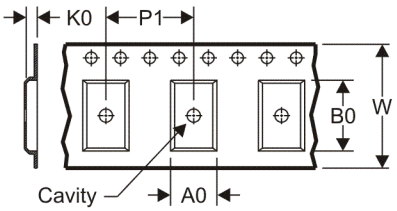
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

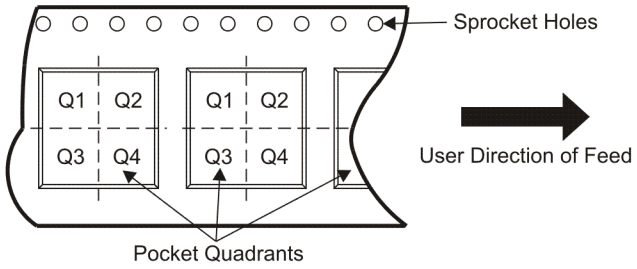


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

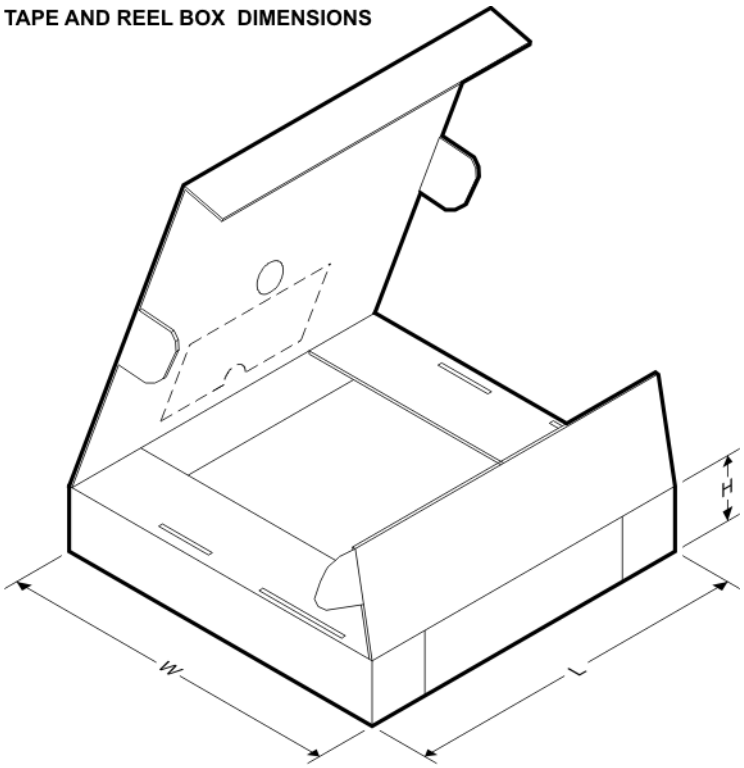
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2227U/2K5	SOIC	D	8	2500	330.0	12.0	6.0	5.0	2.0	8.0	12.0	Q1
OPA2227UA/2K5	SOIC	D	8	2500	330.0	12.0	6.0	5.0	2.0	8.0	12.0	Q1
OPA2228UA/2K5	SOIC	D	8	2500	330.0	12.0	6.0	5.0	2.0	8.0	12.0	Q1
OPA227U/2K5	SOIC	D	8	2500	330.0	12.0	6.0	5.0	2.0	8.0	12.0	Q1
OPA227UA/2K5	SOIC	D	8	2500	330.0	12.0	6.0	5.0	2.0	8.0	12.0	Q1
OPA228UA/2K5	SOIC	D	8	2500	330.0	12.0	6.0	5.0	2.0	8.0	12.0	Q1
OPA4227UA/2K5	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
OPA4228UA/2K5	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

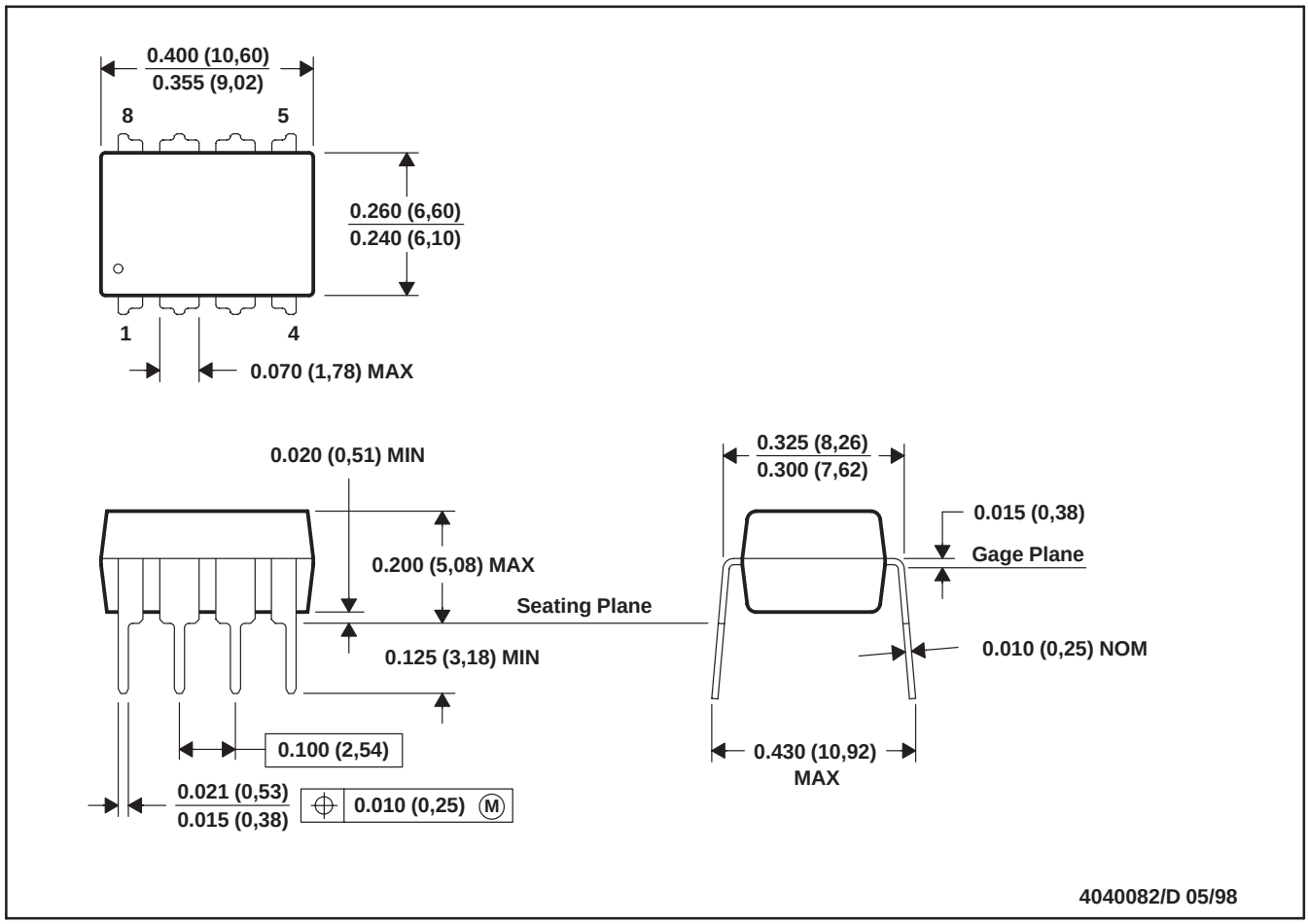


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2227U/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA2227UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA2228UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA227U/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA227UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA228UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA4227UA/2K5	SOIC	D	14	2500	346.0	346.0	33.0
OPA4228UA/2K5	SOIC	D	14	2500	346.0	346.0	33.0

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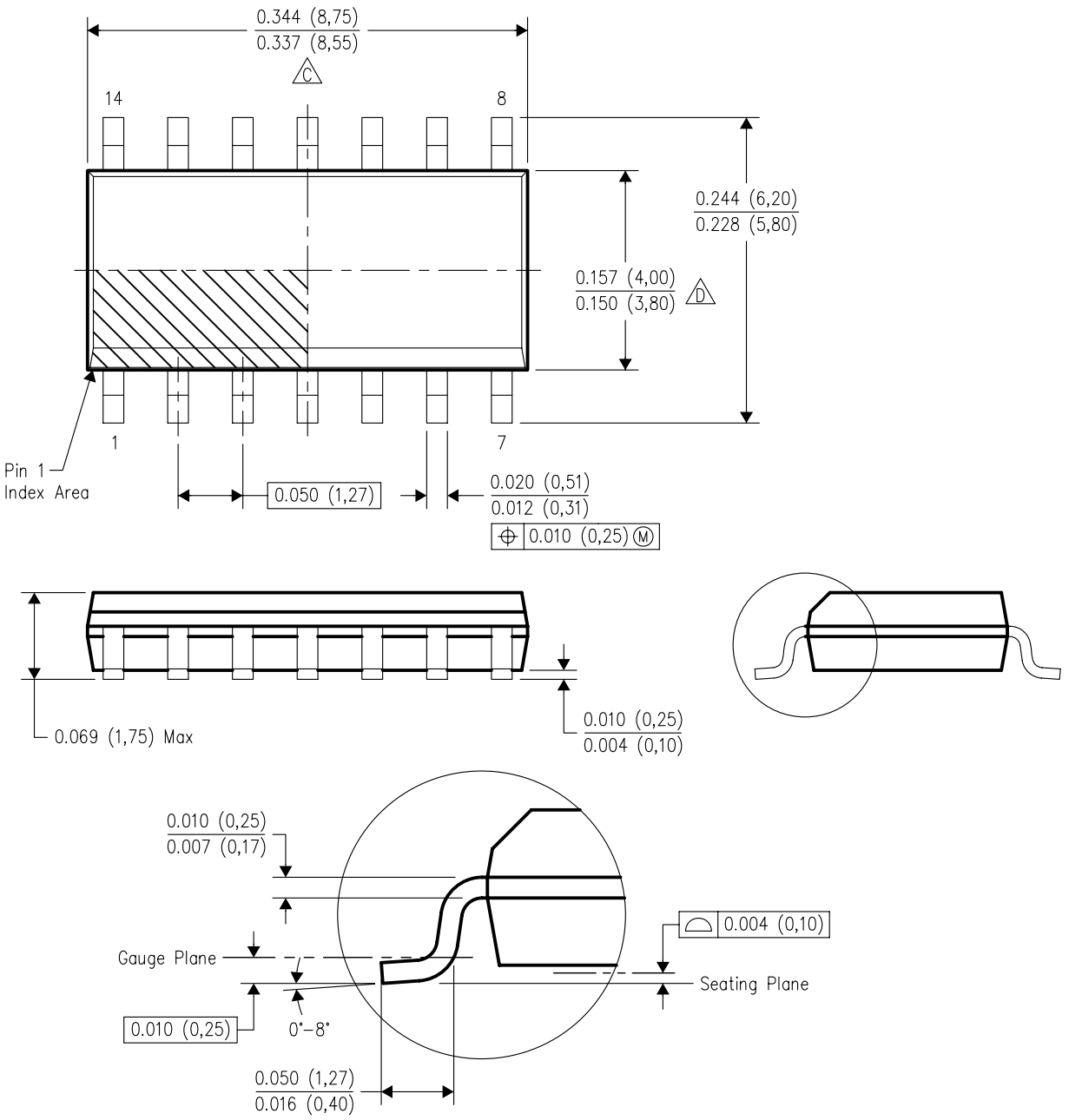
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

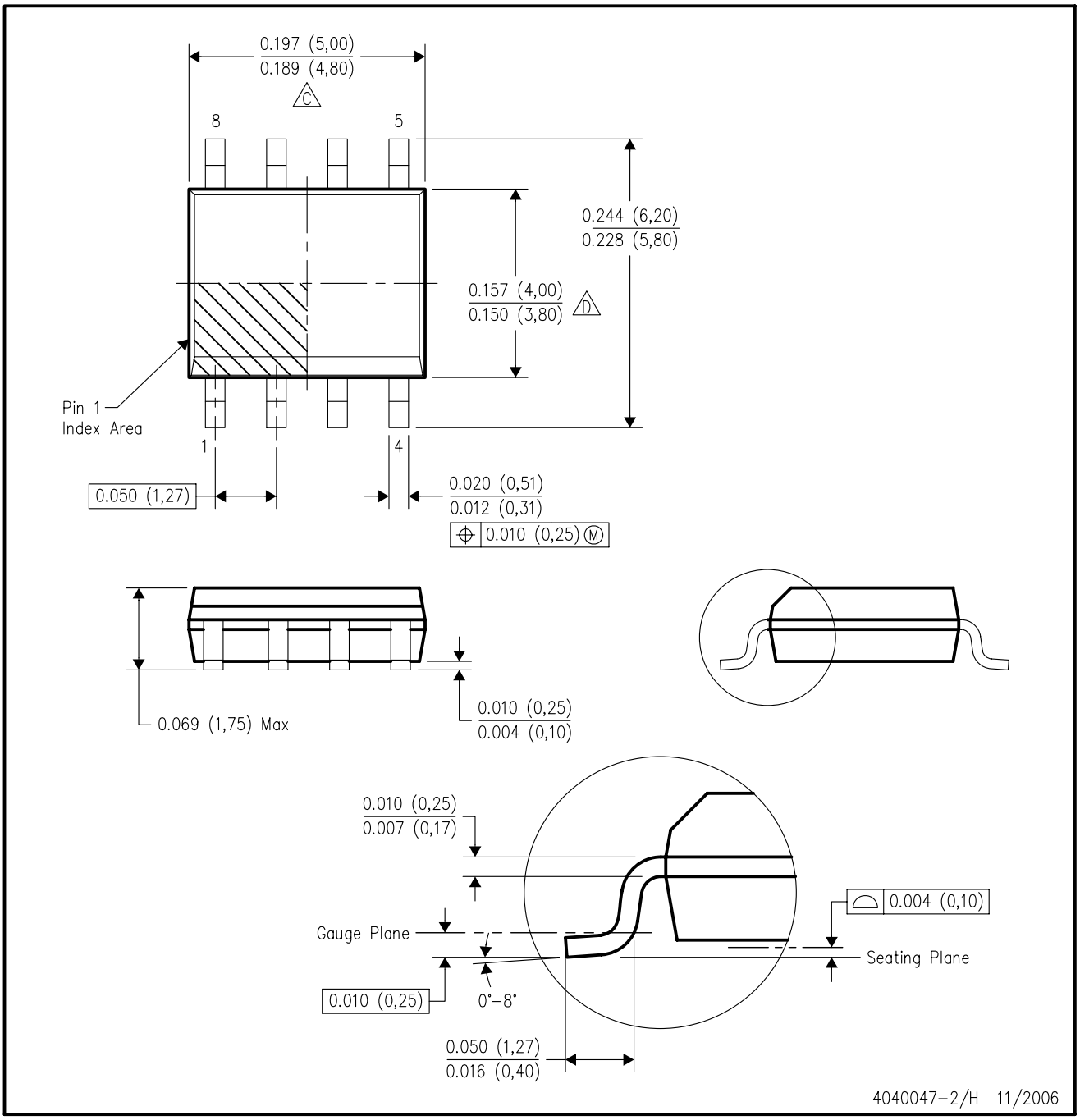
For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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