High-Efficiency 8-A or 14-A Synchronous Buck Converter with Eco-mode™

Check for Samples: TPS53318, TPS53319

FEATURES

- **Conversion Input Voltage Range: 1.5 V to 22 V**
- **VDD Input Voltage Range: 4.5 V to 25 V**
- **91% Efficiency from 12 V to 1.5 V at 14 A**
- **Output Voltage Range: 0.6 V to 5.5 V**
- **5-V LDO Output**
- **Supports Single Rail Input**
- **Integrated Power MOSFETs with 8-A (TPS53318) or 14-A (TPS53319) of Continuous Output Current**
- **Auto-Skip Eco-mode™ for Light-Load Efficiency**
- **<110 µA Shut Down Current**
- **D-CAP™ Mode with Fast Transient Response**
- **Selectable Switching Frequency from 250 kHz to 1 MHz with External Resistor**
- **Selectable Auto-Skip or PWM-Only Operation**
- **Built-in 1% 0.6-V Reference.**
- **0.7-ms, 1.4-ms, 2.8-ms and 5.6-ms Selectable Internal Voltage Servo Soft-Start**
- **Integrated Boost Switch**
- **Pre-Charged Start-up Capability**
- **Adjustable Overcurrent Limit with Thermal Compensation**
- **Overvoltage, Undervoltage, UVLO and Over-Temperature Protection**
- **Supports All Ceramic Output Capacitors**
- **Open-Drain Power Good Indication**
- **Incorporates NexFET™ Power Block Technology**
- **22-pin QFN Package with PowerPAD™**

APPLICATIONS

- **Server/Storage**
- **Workstations and Desktops**
- **Telecommunications Infrastructure**

DESCRIPTION

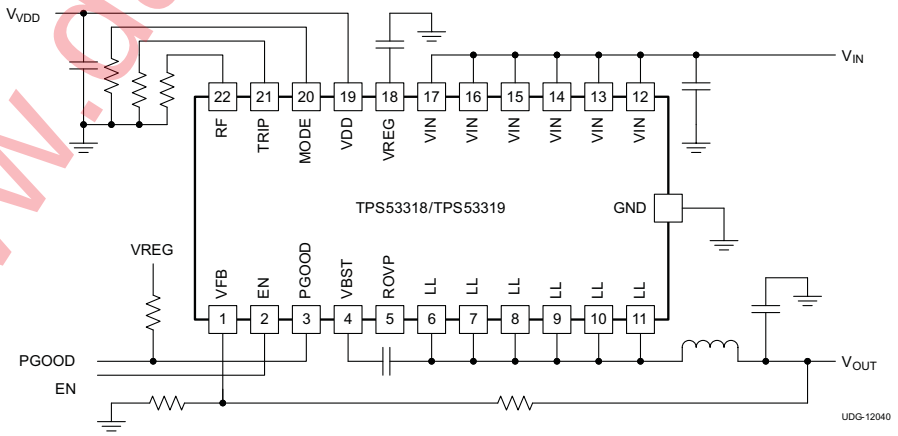
The TPS53318 and TPS53319 are D-CAP™ mode, 8-A or 14-A synchronous switchers with integrated MOSFETs. They are designed for ease of use, low external component count, and space-conscious power systems.

These devices feature accurate 1%, 0.6-V reference, and integrated boost switch. A sample of competitive features include: 1.5-V to 22-V wide conversion input voltage range, very low external component count, D-CAP™ mode control for super fast transient, auto-skip mode operation, internal soft-start control, selectable frequency, and no need for compensation.

The conversion input voltage ranges from 1.5 V to 22 V, the supply voltage range is from 4.5 V to 25 V, and the output voltage range is from 0.6 V to 5.5 V.

These devices are available in 5 mm x 6 mm, 22-pin QFN package and is specified from –40°C to 85°C.

SIMPLIFIED APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	ORDERING PART NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
–40°C to 85°C	Plastic QFN (DQP)	TPS53318DQPR	22	Tape and reel	2500	Pb-Free (RoHS Exempt)
		TPS53318DQPT		Mini reel	250	
		TPS53319DQPR		Tape and reel	2500	
		TPS53319DQPT		Mini reel	250	

ABSOLUTE MAXIMUM RATINGS(1)

			VALUE		UNIT
			MIN	MAX	
Input voltage range	VIN (main supply)		–0.3	30	V
	VDD		–0.3	28	
	VBST		–0.3	32	
	VBST(with respect to LL)		–0.3	7	
	EN, TRIP, VFB, RF, MODE, ROVP		–0.3	7	
Output voltage range	LL	DC	–2	30	V
		Pulse < 20ns, E=5 µJ	–7	32	
	PGOOD, VREG		–0.3	7	
	GND		–0.3	0.3	
Source/Sink current	VBST		50		mA
Operating free-air temperature, T_A			–40	85	°C
Storage temperature range, T_{stg}			–55	150	
Junction temperature range, T_J			–40	150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				300	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS53319	UNITS
		DQP (22 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	27.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	17.1	
θ_{JB}	Junction-to-board thermal resistance	5.9	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	5.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VIN (main supply)	1.5	22	V
	VDD	4.5	25	
	VBST	4.5	28	
	VBST(with respect to LL)	4.5	6.5	
	EN, TRIP, VFB, RF, MODE, ROVP	–0.1	6.5	
Output voltage range	LL	–1	27	V
	PGOOD, VREG	–0.1	6.5	
Junction temperature range, T_J		–40	125	°C

ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range, V_{VDD}=12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{VIN}	VIN pin power conversion input voltage		1.5		22	V
V_{VDD}	Supply input voltage		4.5		25.0	V
$I_{VIN(leak)}$	VIN pin leakage current	V_{EN} = 0 V			1	µA
I_{VDD}	VDD supply current	T_A = 25°C, No load, V_{EN} = 5 V, V_{VFB} = 0.630 V		420	590	µA
I_{VDDSDN}	VDD shutdown current	T_A = 25°C, No load, V_{EN} = 0 V			110	µA
INTERNAL REFERENCE VOLTAGE						
V_{VFB}	VFB regulation voltage	CCM condition(1)		0.600		V
V_{VFB}	VFB regulation voltage	T_A = 25°C	0.597	0.600	0.603	V
		0°C ≤ T_A ≤ 85°C	0.5952	0.600	0.6048	
		–40°C ≤ T_A ≤ 85°C	0.594	0.600	0.606	
I_{VFB}	VFB input current	V_{VFB} = 0.630 V, T_A = 25°C		0.01	0.20	µA
LDO OUTPUT						
V_{VREG}	LDO output voltage	0 mA ≤ I_{VREG} ≤ 30 mA	4.77	5.00	5.36	V
I_{VREG}	LDO output current(1)	Maximum current allowed from LDO			30	mA
V_{DO}	Low drop out voltage	V_{VDD} = 4.5 V, I_{VREG} = 30 mA			250	mV
BOOT STRAP SWITCH						
V_{FBST}	Forward voltage	$V_{VREG-VBST}$, I_F = 10 mA, T_A = 25°C		0.1	0.2	V
I_{VBSTLK}	VBST leakage current	V_{VBST} = 23 V, V_{SW} = 17 V, T_A = 25°C		0.01	1.50	µA
DUTY AND FREQUENCY CONTROL						
$t_{OFF(min)}$	Minimum off-time	T_A = 25°C	150	260	400	ns
$t_{ON(min)}$	Minimum on-time	V_{IN} = 17 V, V_{OUT} = 0.6 V, f_{SW} = 1 MHz, T_A = 25 °C(1)		35		ns
SOFT START						
t_{SS}	Internal soft-start time from V_{OUT} = 0 V to 95% of V_{OUT}	R_{MODE} = 39 kΩ		0.7		ms
		R_{MODE} = 100 kΩ		1.4		
		R_{MODE} = 200 kΩ		2.8		
		R_{MODE} = 470 kΩ		5.6		
OUTPUT VOLTAGE DISCHARGE						
I_{DSCHG}	Output voltage discharge current	V_{EN}= 0 V, V_{SW}= 0.5 V	5.0	6.6	9.0	mA

(1) Ensured by design. Not production tested.

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ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range, V_{VDD}=12 V (unless otherwise noted)

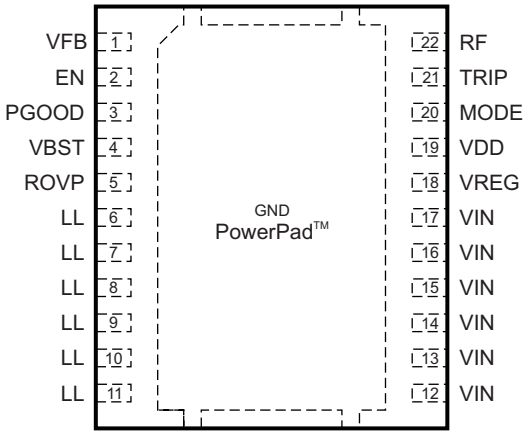
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWERGOOD							
V_{THPG}	PG threshold		PG in from lower	92.5%	95.0%	98.5%	
			PG in from higher	107.5%	110.0%	112.5%	
			PG hysteresis	2.5%	5.0%	7.5%	
R_{PG}	PG transistor on-resistance			15	30	60	Ω
t_{PGDEL}	PG delay		Delay for PG in	0.8	1	1.2	ms
LOGIC THRESHOLD AND SETTING CONDITIONS							
V_{EN}	EN Voltage		Enable	1.0	1.3	1.6	V
			Disable	0.8	1.0	1.2	
I_{EN}	EN Input current		V_{EN} = 5 V			1.0	µA
f_{SW}	Switching frequency		R_{RF} = 0 Ω to GND, T_A = 25°C(1)	200	250	300	kHz
			R_{RF} = 187 kΩ to GND, T_A = 25°C(1)	250	300	350	
			R_{RF} = 619 kΩ, to GND, T_A = 25°C(1)	350	400	450	
			R_{RF} = Open, T_A= 25°C(1)	450	500	550	
			R_{RF} = 866 kΩ to VREG, T_A = 25°C(1)	540	600	660	
			R_{RF} = 309 kΩ to VREG, T_A = 25°C(1)	670	750	820	
			R_{RF} = 124 kΩ to VREG, T_A = 25°C(1)	770	850	930	
			R_{RF} = 0 Ω to VREG, T_A = 25°C(1)	880	970	1070	
PROTECTION: CURRENT SENSE							
I_{TRIP}	TRIP source current		V_{TRIP} = 1 V, T_A = 25°C		10		µA
TC_{ITRIP}	TRIP current temperature coeffficient		On the basis of 25°C(2)		3000		ppm/°C
V_{TRIP}	Current limit threshold setting range	TPS53318	$V_{TRIP-GND}$	0.4		1.5	V
		TPS53319		0.4		2.4	
V_{OCL}	Current limit threshold		V_{TRIP} = 1.2 V		37.5		mV
			V_{TRIP} = 0.4		12.5		
V_{OCLN}	Negative current limit threshold		V_{TRIP} = 1.2 V		–37.5		mV
			V_{TRIP} = 0.4 V		–12.5		
I_{OCP}	Valley current limit threshold		R_{TRIP} = 66.5 kΩ, 0°C ≤ T_A ≤ 125°C	4.6	5.4	6.3	A
			R_{TRIP} = 66.5 kΩ, –40°C ≤ T_A ≤ 125°C	4.4	5.4	6.3	
V_{AZCADJ}	Auto zero cross adjustable range		Positive	3	15		mV
			Negative		–15	–3	
PROTECTION: UVP and OVP							
V_{OVP}	OVP trip threshold		OVP detect	115%	120%	125%	
t_{OVPDEL}	OVP proprogation delay		VFB delay with 50-mV overdrive		1		µs
V_{UVP}	Output UVP trip threshold		UVP detect	65%	70%	75%	
t_{UVPDEL}	Output UVP proprogation delay			0.8	1.0	1.2	ms
t_{UVPEN}	Output UVP enable delay		From enable to UVP workable	1.5	2.3	3.0	ms
UVLO							
V_{UVVREG}	VREG UVLO threshold		Wake up	4.00	4.20	4.33	V
			Hysteresis		0.25		
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold		Shutdown temperature(2)		145		°C
			Hysteresis(2)		10		

(1) Not production tested. Test condition is V_{IN}= 12 V, V_{OUT}= 1.2 V, I_{OUT} = 5 A using application circuit shown in Figure 1.
(2) Ensured by design. Not production tested.

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DEVICE INFORMATION

DQP PACKAGE
22 PINS
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O/P(1)	DESCRIPTION
NAME	NO.		
EN	2	I	Enable pin.Typical turn-on threshold voltage is 1.3 V. Typical turn-off threshold voltage is 1.0 V.
GND		G	Ground and thermal pad of the device. Use proper number of vias to connect to ground plane.
LL	6	B	Output of converted power. Connect this pin to the output Inductor.
	7		
	8		
	9		
	10		
	11		
MODE	20	I	Soft-start and mode selection. Connect a resistor to select soft-start time using Table 1. The soft-start time is detected and stored into internal register during start-up.
PGOOD	3	O	Open drain power good flag. Provides 1-ms start-up delay after VFB falls in specified limits. When VFB goes out of the specified limits PGOOD goes low after a 2-µs delay
ROVP	5	I	Redundant overvoltage protection (OVP) input. Use a resistor divider to connect this pin to V_{OUT}. Internally pulled down to GND with 1.5-MΩ resistor. Float this pin or connect to GND if redundant OVP is not needed.
RF	22	I	Switching frequency selection. Connect a resistor to GND or VREG to select switching frequency using Table 2. The switching frequency is detected and stored during the startup.
TRIP	21	I	OCL detection threshold setting pin. I_{TRIP} = 10 µA at room temperature, 3000 ppm/°C current is sourced and set the OCL trip voltage as follows.
			$V_{OCL}=V_{TRIP}/32$ ($V_{TRIP} \le 2.4$ V, $V_{OCL} \le 75$ mV)
VBST	4	P	Supply input for high-side FET gate driver (boost terminal). Connect capacitor from this pin to LL node. Internally connected to VREG via bootstrap MOSFET switch.
VDD	19	P	Controller power supply input. VDD input voltage range is from 4.5 V to 25 V.
VFB	1	I	Output feedback input. Connect this pin to V_{OUT} through a resistor divider.
VIN	12	P	Conversion power input.The conversion input voltage range is from 1.5 V to 22 V.
	13		
	14		
	15		
	16		
	17		

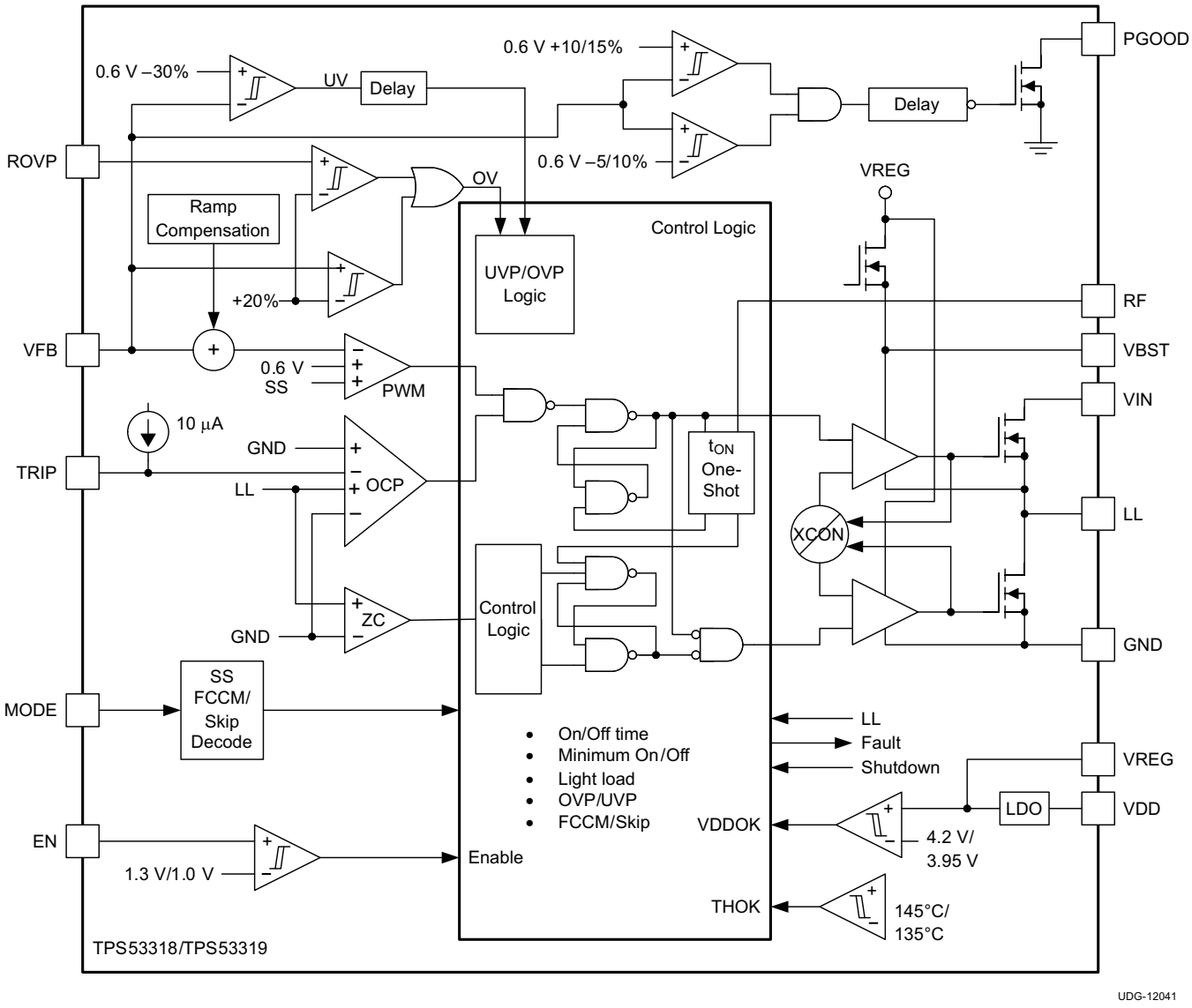
(1) I=Input, O=Output, B=Bidirectional, P=Supply, G=Ground

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PIN FUNCTIONS (continued)

PIN		I/O/P(1)	DESCRIPTION
NAME	NO.		
VREG	18	P	5-V low drop out (LDO) output. Supplies the internal analog circuitry and driver circuitry.

BLOCK DIAGRAM



NOTE

The thresholds shown in this diagram are typical numbers. Refer to the ELECTRICAL CHARACTERISTICS table for threshold tolerance.

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APPLICATION CIRCUIT DIAGRAM

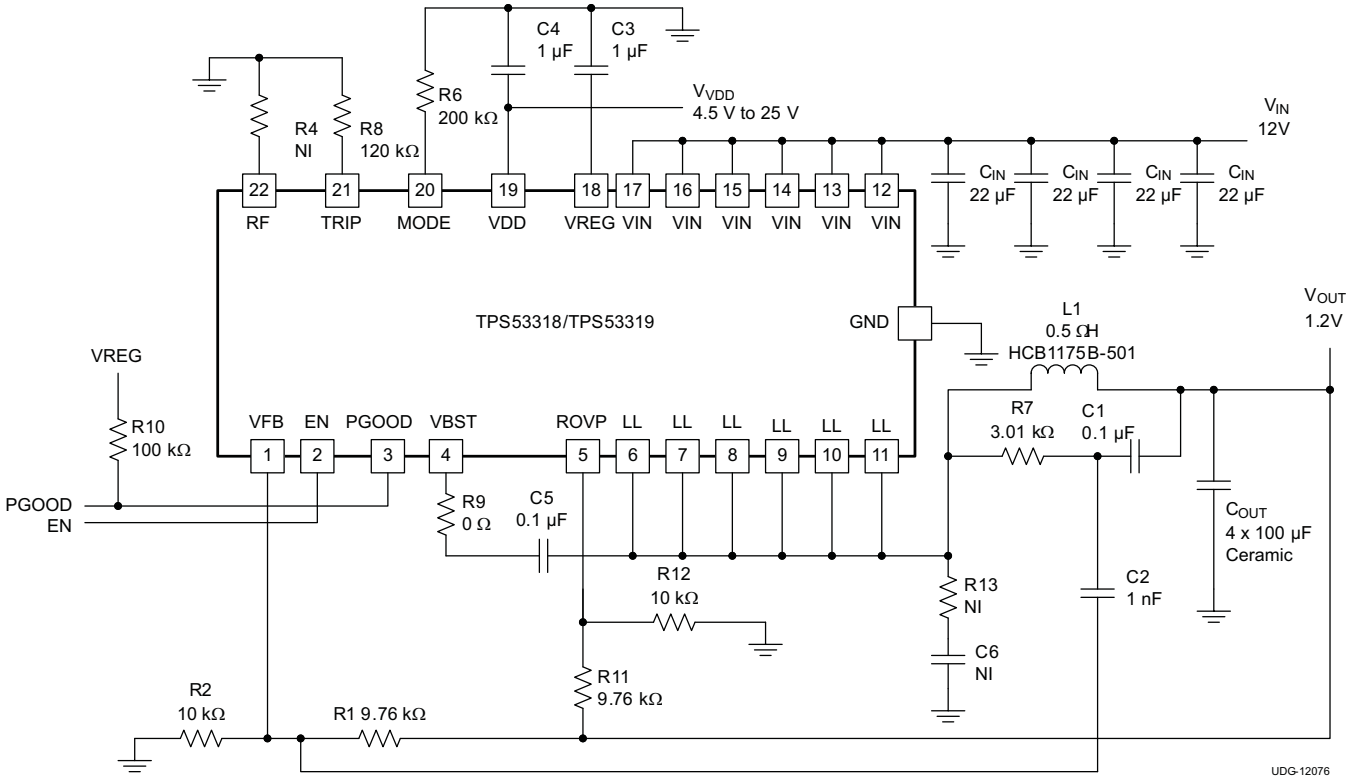


Figure 1. Typical Application Circuit with Ceramic Output Capacitors, ROVP Function Used

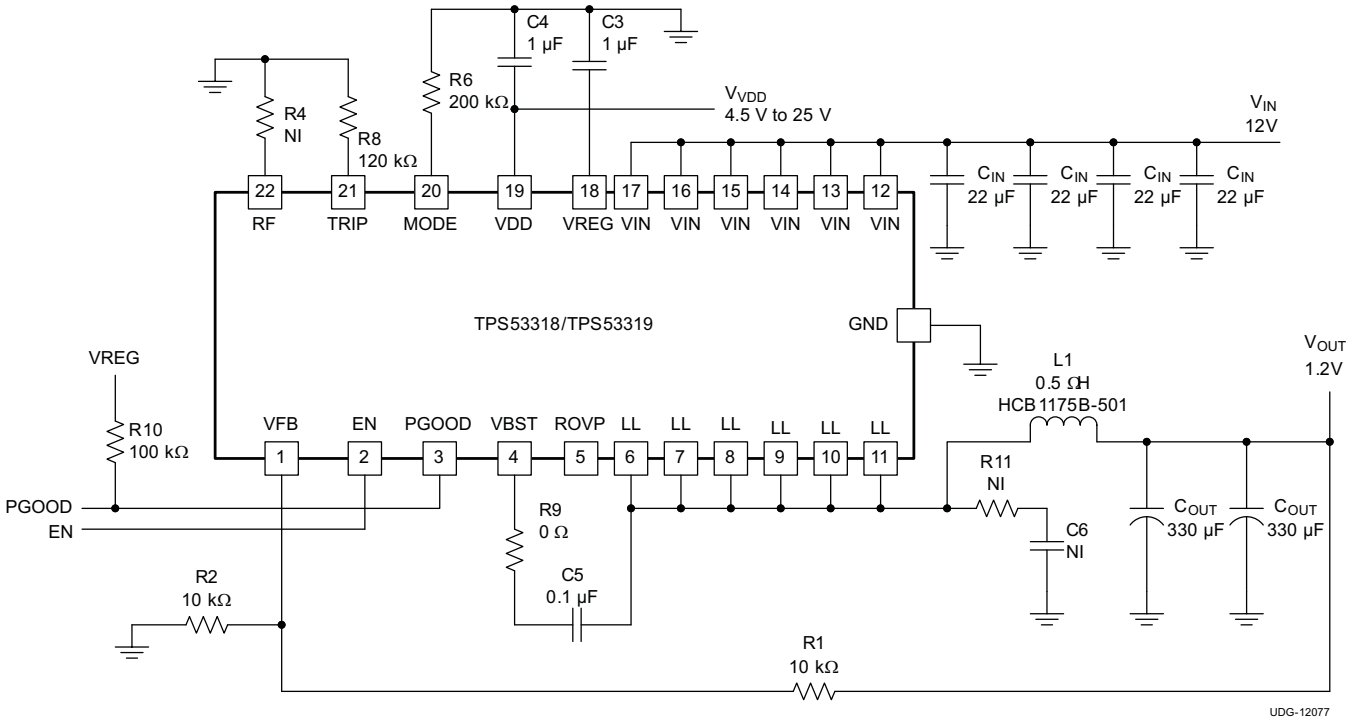


Figure 2. Typical Application Circuit with Bulk Output Capacitors, ROVP Function Not Used

TYPICAL CHARACTERISTICS

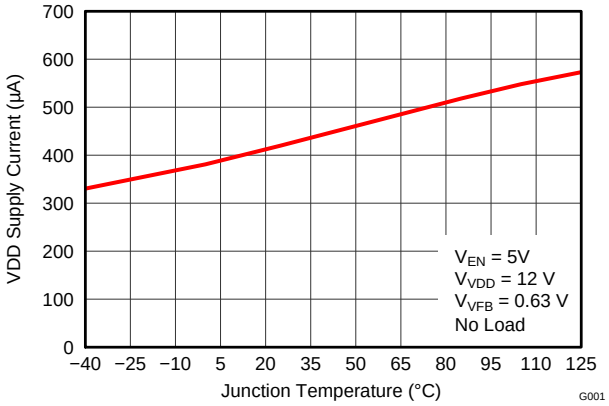


Figure 3. VDD Supply Current vs. Junction Temperature

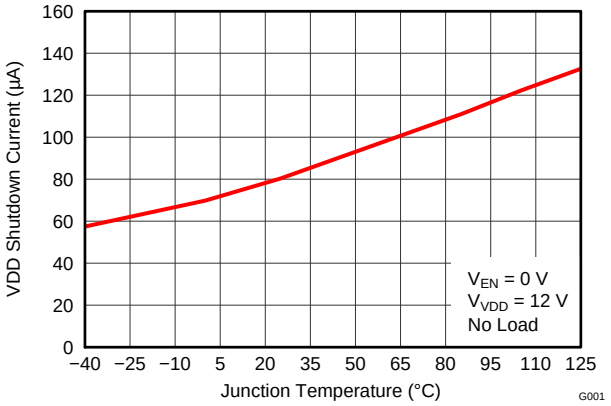


Figure 4. VDD Shutdown Current vs. Junction Temperature

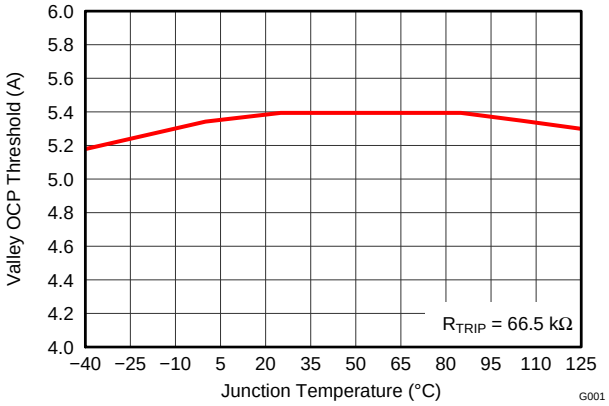


Figure 5. Valley OCP Threshold vs Temperature

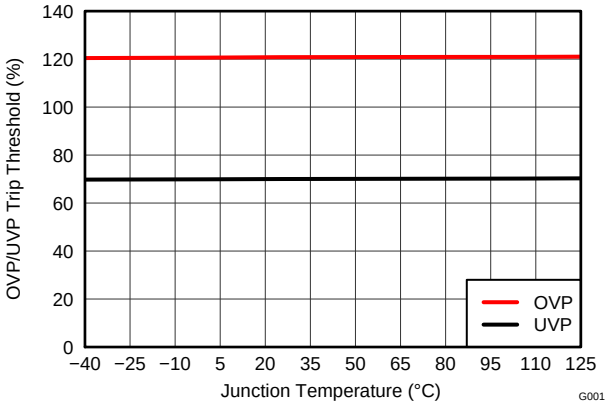


Figure 6. OVP/UVP Trip Threshold vs. Junction Temperature

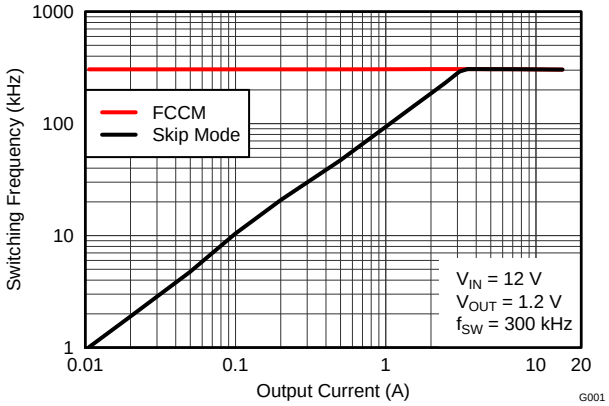


Figure 7. Switching Frequency vs. Output Current

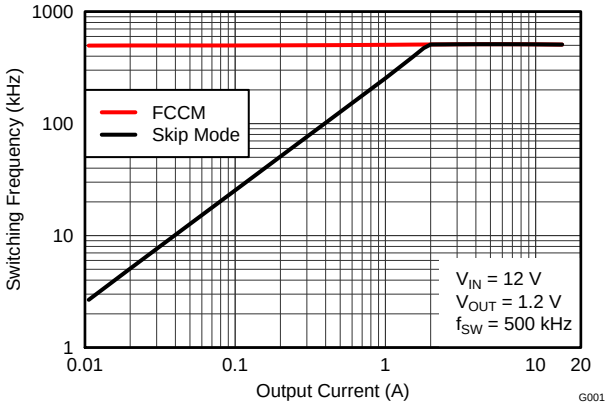


Figure 8. Switching Frequency vs. Output Current

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TYPICAL CHARACTERISTICS (continued)

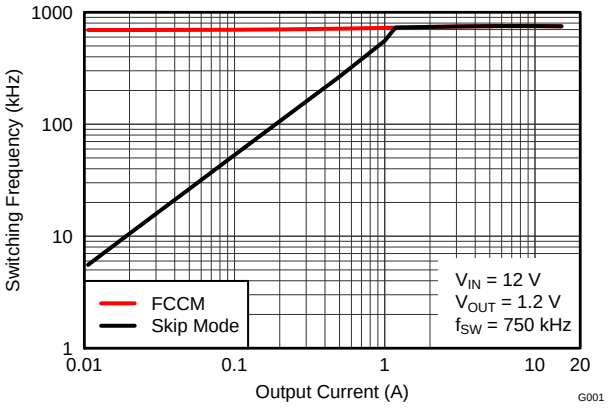


Figure 9. Switching Frequency vs. Output Current

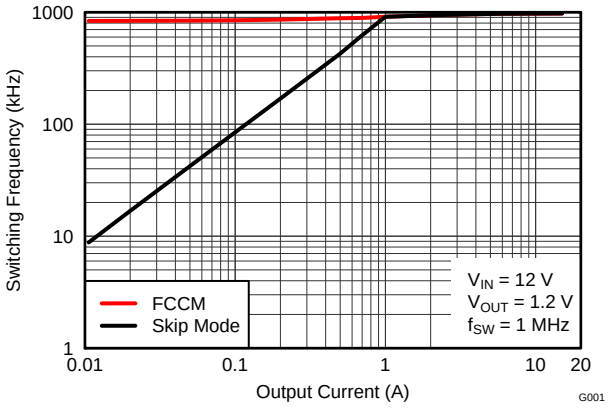


Figure 10. Switching Frequency vs. Output Current

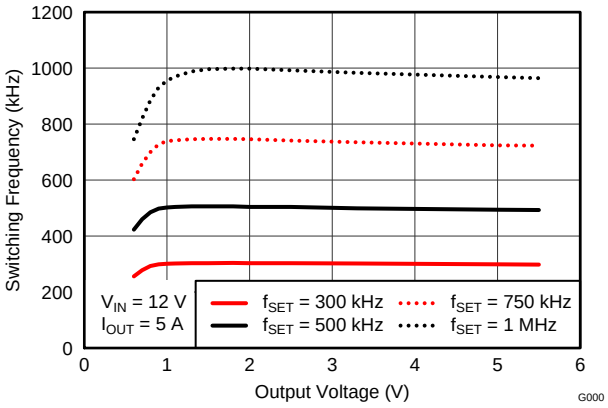


Figure 11. Switching Frequency vs. Output Voltage

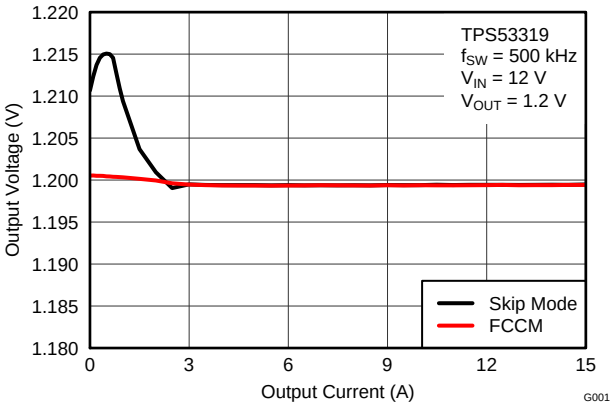


Figure 12. Output Voltage vs. Output Current

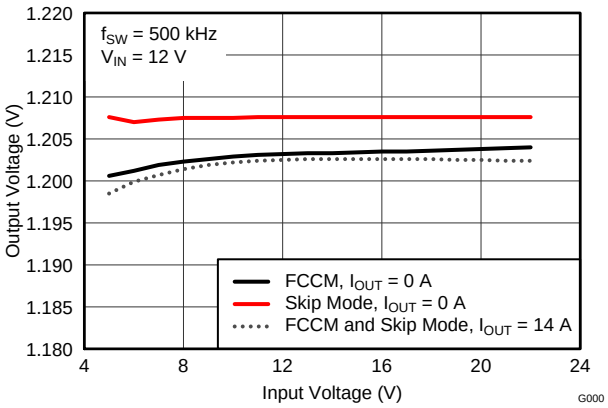


Figure 13. Output Voltage vs. Input Voltage

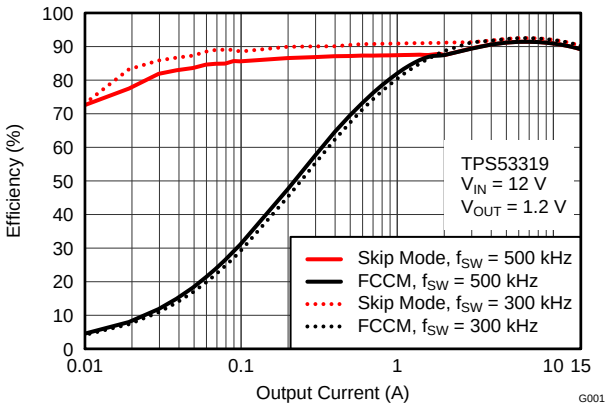


Figure 14. Efficiency vs Output Current

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TPS53319 TYPICAL CHARACTERISTICS

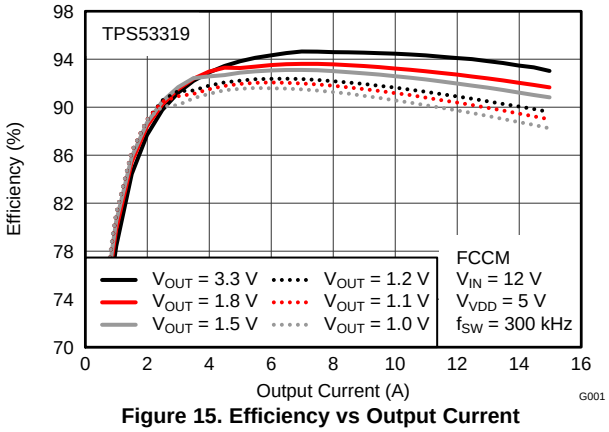


Figure 15. Efficiency vs Output Current

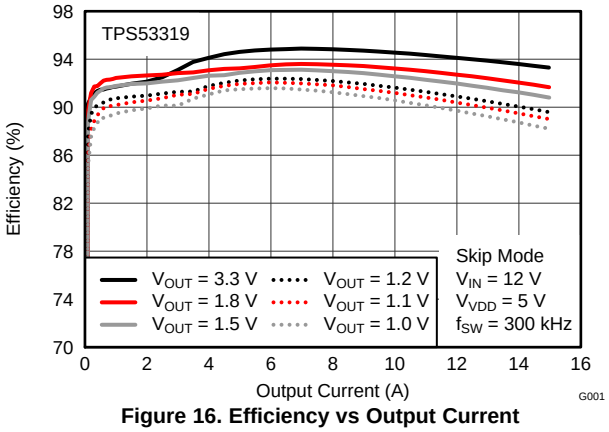


Figure 16. Efficiency vs Output Current

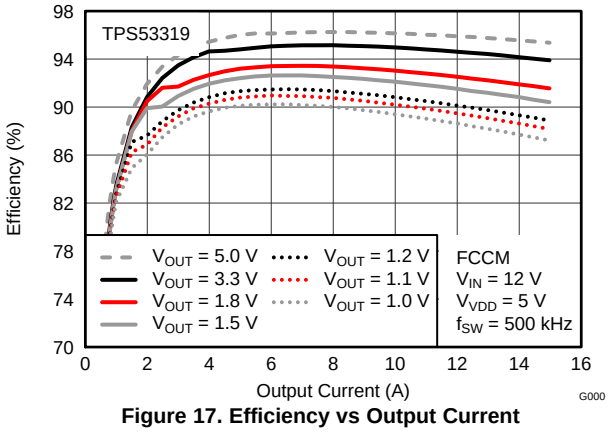


Figure 17. Efficiency vs Output Current

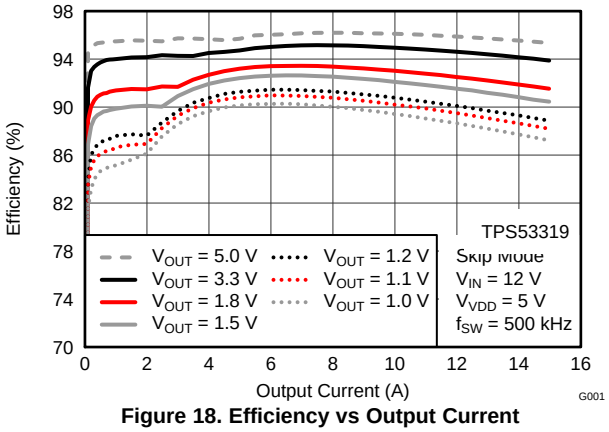


Figure 18. Efficiency vs Output Current

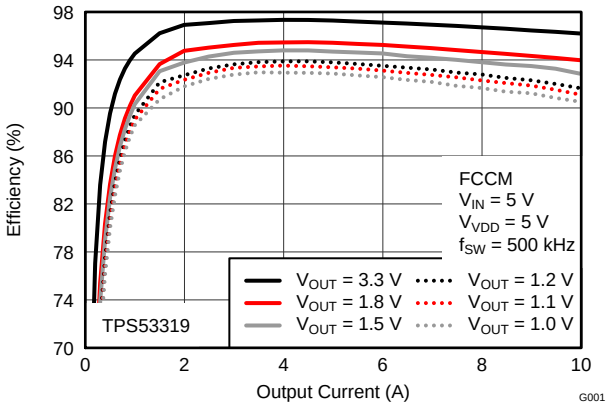


Figure 19. Efficiency vs Output Current

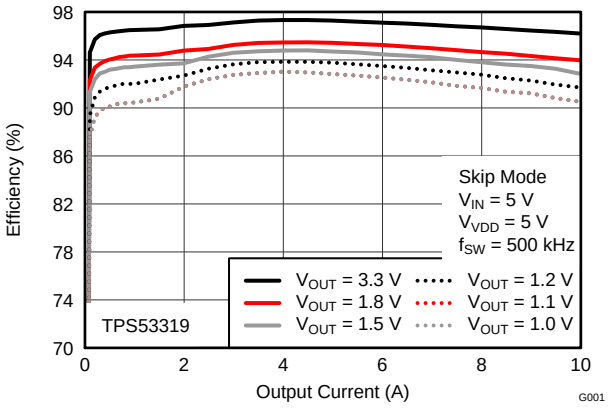


Figure 20. Efficiency vs Output Current

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TPS53318 TYPICAL CHARACTERISTICS

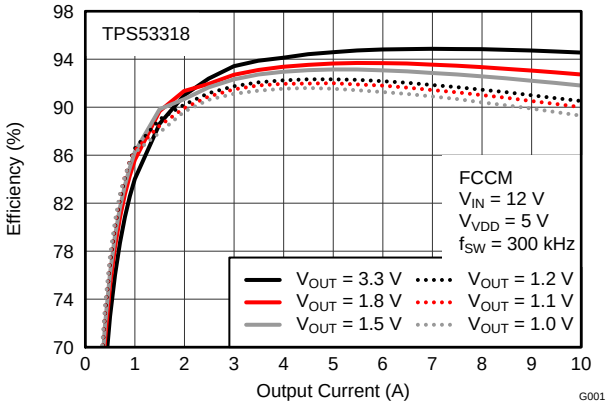


Figure 21. Efficiency vs Output Current

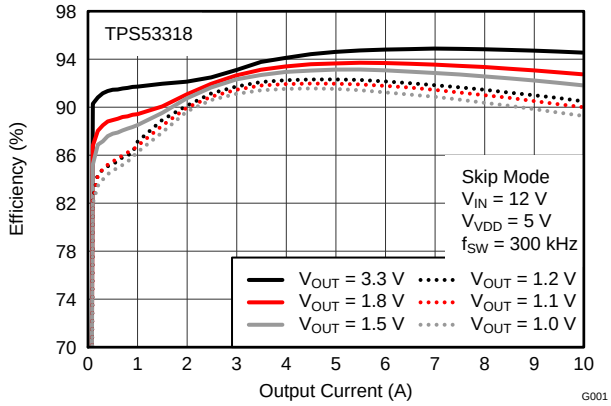


Figure 22. Efficiency vs Output Current

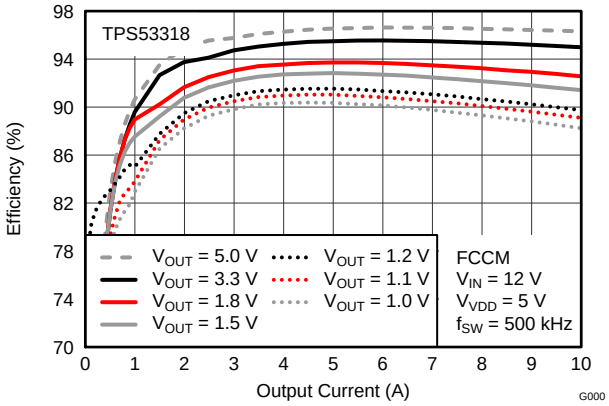


Figure 23. Efficiency vs Output Current

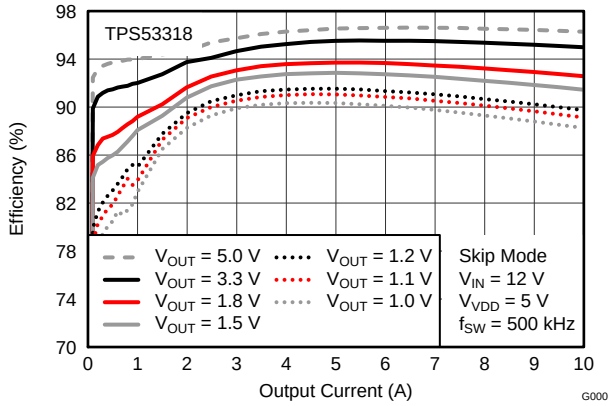


Figure 24. Efficiency vs Output Current

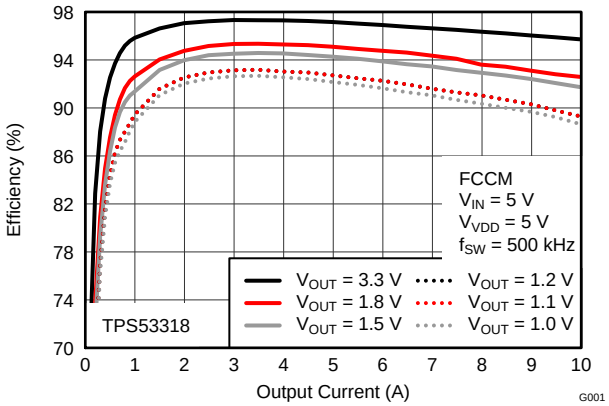


Figure 25. Efficiency vs Output Current

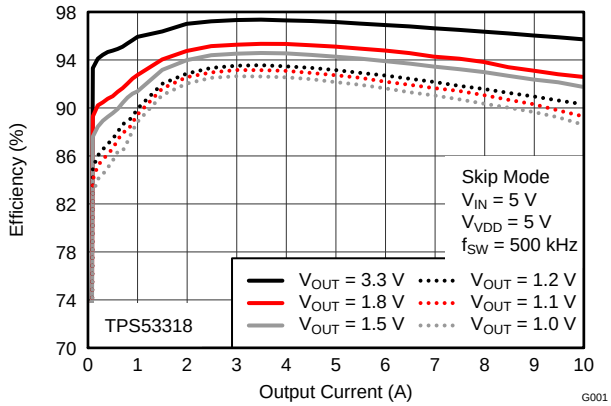


Figure 26. Efficiency vs Output Current

TYPICAL CHARACTERISTICS

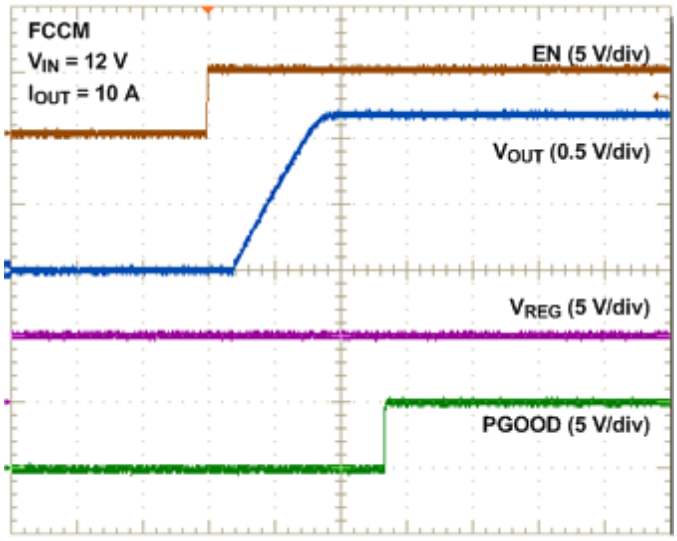


Figure 27. Start-Up

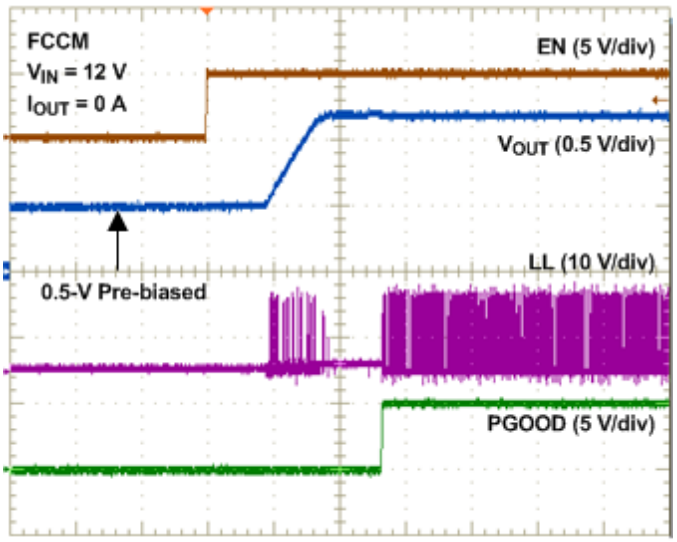


Figure 28. Pre-Bias Start-Up

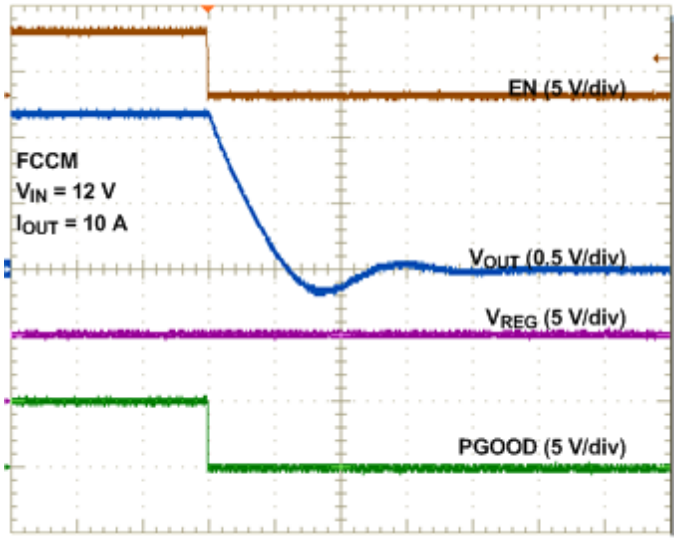


Figure 29. Shutdown

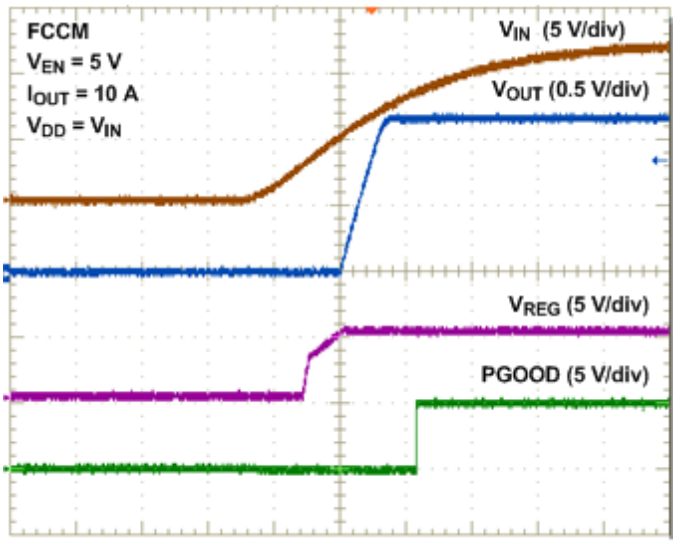


Figure 30. UVLO Start-Up

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TYPICAL CHARACTERISTICS (continued)

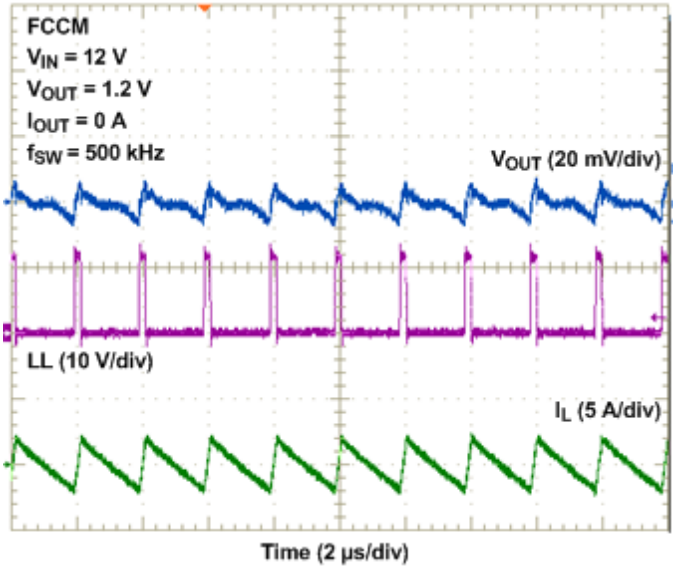


Figure 31. 1.1-V Output FCCM Mode Steady-State Operation

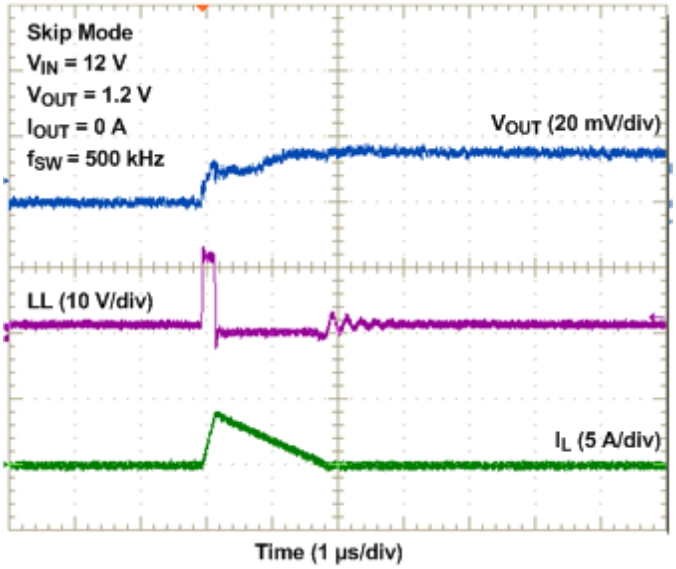


Figure 32. 1.1-V Output Skip Mode Steady-State Operation

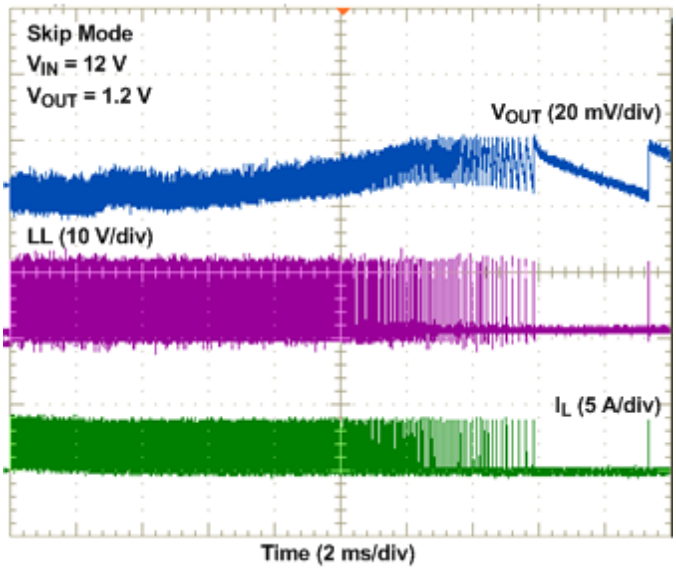


Figure 33. CCM to DCM Transition

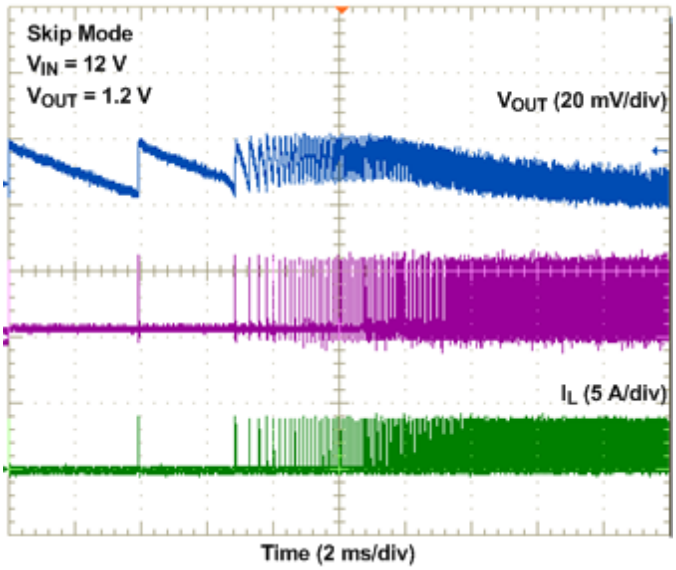


Figure 34. DCM to CCM Transition

TYPICAL CHARACTERISTICS (continued)

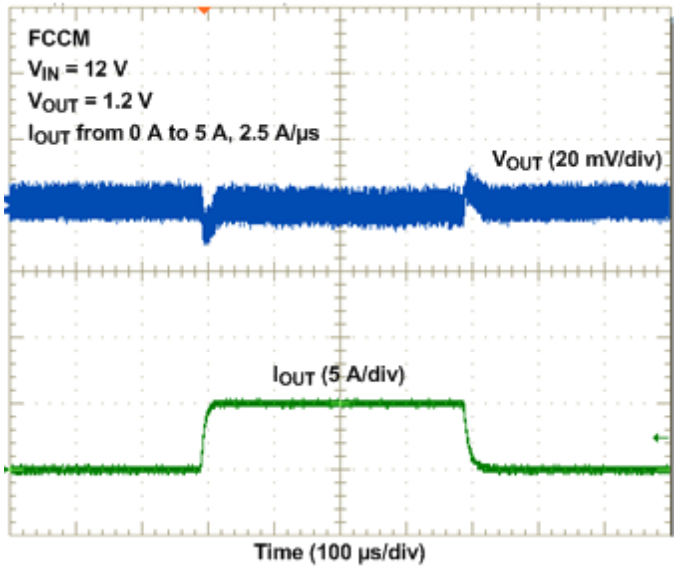


Figure 35. FCCM Load Transient

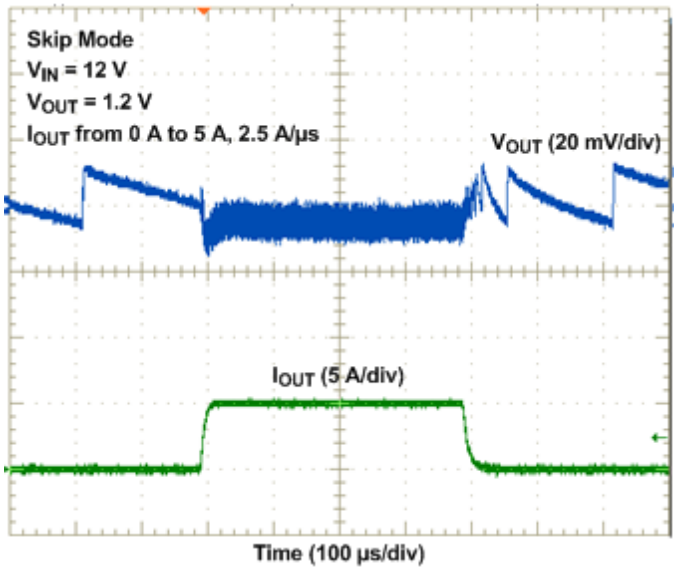


Figure 36. Skip Mode Load Transeint

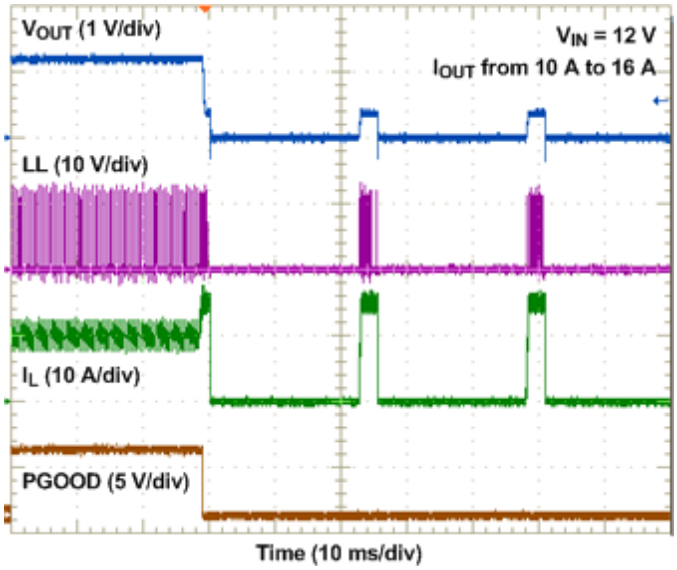


Figure 37. Overcurrent Protection

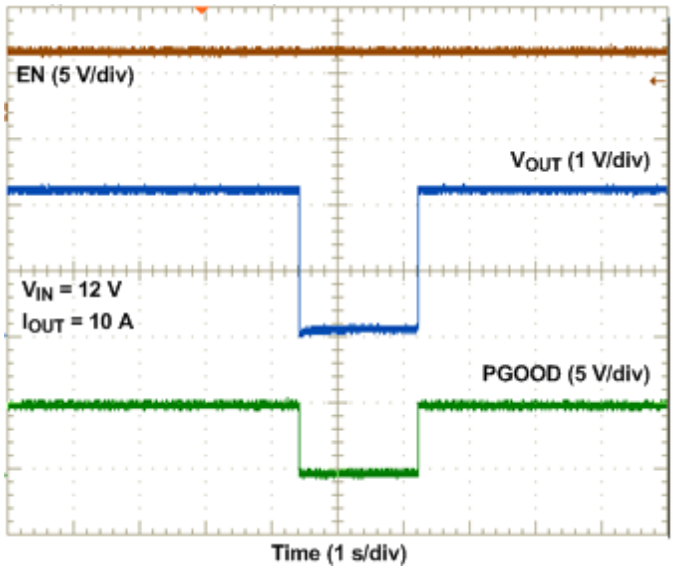


Figure 38. Over-temperature Protection

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TYPICAL CHARACTERISTICS (continued)

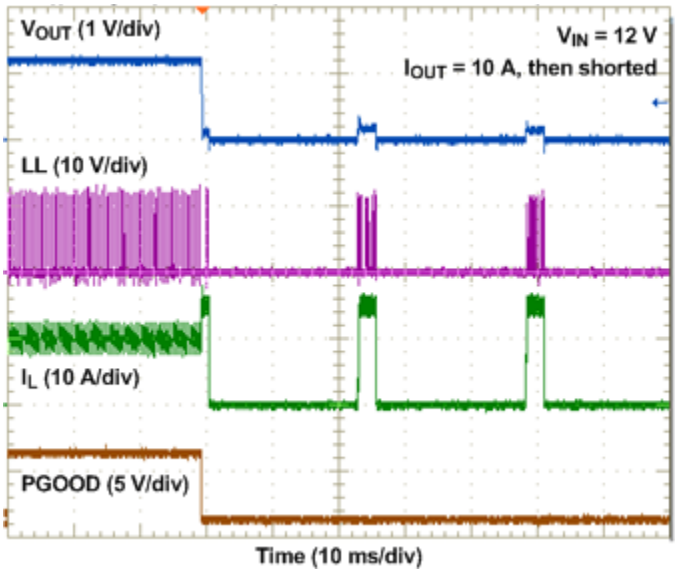


Figure 39. Short Circuit Protection

THERMAL CHARACTERISTICS

Thermal signatures for the TPS53319 EVM, V_{IN} = 12 V, I_{OUT} = 14 A, f_{SW} = 500 kHz, T_A = 25°C, No airflow

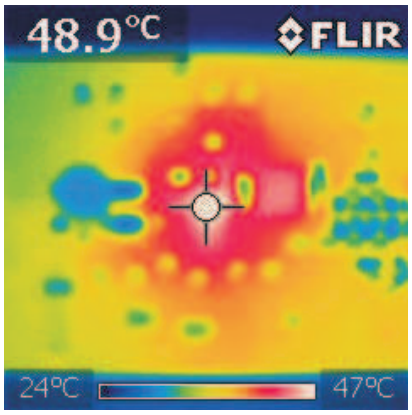


Figure 40. V_{OUT} = 1.2 V

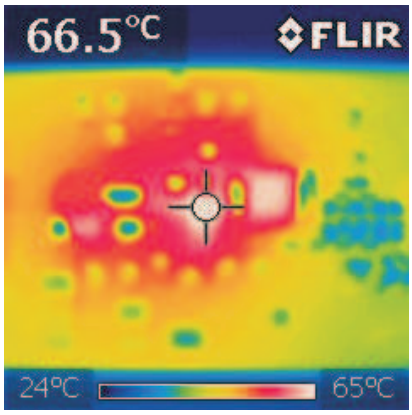


Figure 41. V_{OUT} = 5.0 V

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APPLICATION INFORMATION

General Description

The TPS53318 and TPS53319 are high-efficiency, single channel, synchronous buck converters suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V to 22 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP™ mode uses the equivalent series resistance (ESR) of the output capacitor(s) to sense the device current . One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

These devices have a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms as shown in Table 1.

5-V LDO and VREG Start-Up

Both the TPS53318 and TPS53319 have an internal 5-V LDO feature using input from VDD and output to VREG. When the VDD voltage rises above 1 V, the internal LDO is enabled and outputs voltage to the VREG pin. The VREG voltage provides the bias voltage for the internal analog circuitry. It also provides the supply voltage for the gate drives.

NOTE

The 5-V LDO is not controlled by the EN pin. It starts up whenever VDD rises to approximately 2 V. (see Figure 31).

Enable, Soft Start, and Mode Selection

When the EN pin voltage rises above the enable threshold voltage (typically 1.3 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5 V at the VREG pin. The controller then uses the first 250 µs to calibrate the switching frequency setting resistance attached to the RF pin and stores the switching frequency code in internal registers. During this period, the MODE pin also senses the resistance attached to this pin and determines the soft-start time . Switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

Table 1. Soft-Start and MODE Settings

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R_{MODE} (kΩ)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM(1)	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

(1) Device enters FCCM after the PGOOD pin goes high when MODE is connected to PGOOD through the resistor R_{MODE}.

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After soft-start begins, the MODE pin becomes the input of an internal comparator which determines auto skip or FCCM mode operation. If MODE voltage is higher than 1.3 V, the converter enters into FCCM mode. Otherwise it will be in auto skip mode at light load condition. Typically, when FCCM mode is selected, the MODE pin is connected to PGOOD through the R_{MODE} resistor, so that before PGOOD goes high the converter remains in auto skip mode.

Adaptive On-Time D-CAP™ Control and Frequency Selection

Neither the TPS53318 nor the TPS53319 has a dedicated oscillator to determine switching frequency. However, the device operates with pseudo-constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage ($t_{ON} \propto V_{OUT}/V_{IN}$).

This makes the switching frequency fairly constant in steady state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in Table 2. (Maintaining open resistance sets the switching frequency to 500 kHz.)

Table 2. Resistor and Switching Frequency

RESISTOR (R_{RF}) CONNECTIONS		SWITCHING FREQUENCY (f_{SW}) (kHz)
VALUE (kΩ)	CONNECT TO	
0	GND	250
187	GND	300
619	GND	400
OPEN	n/a	500
866	VREG	600
309	VREG	750
124	VREG	850
0	VREG	970

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a set signal to terminate the off time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal is valid if the inductor current level is below the OCP threshold, otherwise the off time is extended until the current level falls below the threshold.

Figure 42 , Figure 43 show two on-time control schemes.

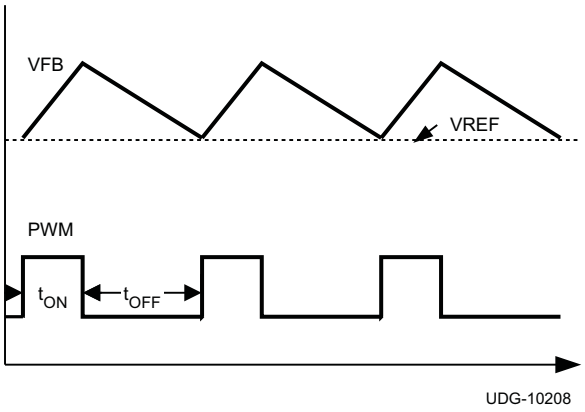


Figure 42. On-Time Control Without Ramp Compensation

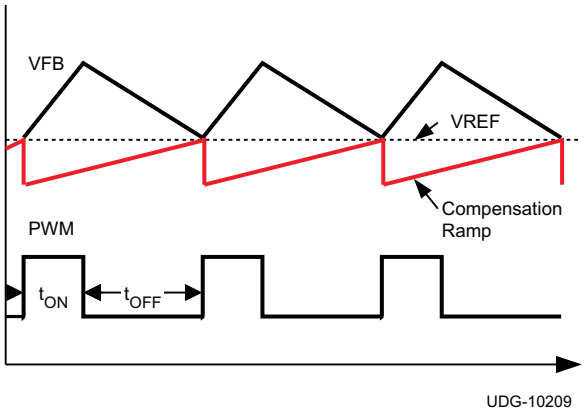


Figure 43. On-Time Control With Ramp Compensation

Ramp Signal

The TPS53318 and TPS53319 add a ramp signal to the 0.6-V reference in order to improve jitter performance. As described in the previous section, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the signal-to-noise ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with –7 mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady state.

During skip mode operation, under discontinuous conduction mode (DCM), the switching frequency is lower than the nominal frequency and the off-time is longer than the off-time in CCM. Because of the longer off-time, the ramp signal extends after crossing 0 mV. However, it is clamped at 3 mV to minimize the DC offset.

Auto-Skip Eco-mode™ Light Load Operation

While the MODE pin is pulled low via R_{MODE}, the controller automatically reduces the switching frequency at light load conditions to maintain high efficiency. Detailed operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light-load operation $I_{OUT(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated as shown in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

where

- f_{SW} is the PWM switching frequency

Switching frequency versus output current in the light load condition is a function of L, V_{IN} and V_{OUT}, but it decreases almost proportionally to the output current from the $I_{OUT(LL)}$ given in Equation 1. For example, it is 60 kHz at $I_{OUT(LL)}$/5 if the frequency setting is 300 kHz.

Adaptive Zero Crossing

The TPS53318 and TPS53319 have an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) in light load condition. In this mode, switching frequency is kept almost constant over the entire load range which is suitable for applications need tight control of the switching frequency at a cost of lower efficiency.

Output Discharge Control

When the EN pin becomes low, the TPS53318 and TPS53319 discharge the output capacitor using the internal MOSFET connected between the SW pin and the PGND pin while the high-side and low-side MOSFETs are maintained in the OFF state. The typical discharge resistance is 75 Ω. The soft discharge occurs only as EN becomes low. The discharge circuit is powered by VDD. While VDD remains high, the discharge circuit remains active.

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Power-Good

The TPS53318 and TPS53319 have power-good output that indicates high when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within +10% and –5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-µs) internal delay. The power-good output is an open drain output and must be pulled up externally.

The power-good MOSFET is powered through the VDD pin. V_{VDD} must be >1 V in order to have a valid power-good logic. It is recommended to pull PGOOD up to VREG (or a voltage divided from VREG) so that the power-good logic is still valid even without VDD supply.

Current Sense, Overcurrent and Short Circuit Protection

The TPS53318 and TPS53319 have cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller maintains the *OFF* state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS53319 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. The TRIP terminal sources current (I_{TRIP}) which is 10 µA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in Equation 2.

$$V_{TRIP}\,(mV) = R_{TRIP}\,(k\Omega) \times I_{TRIP}\,(\mu A) \tag{2}$$

The inductor current is monitored by the LL pin. The GND pin is used as the positive current sensing node and the LL pin is used as the negative current sense node. The trip current, I_{TRIP} has a 3000ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. For each device, I_{TRIP} is also adjusted based on the device-specific on-resistance measurement in production tests to eliminate the any OCP variation from device to device.

As the comparison is made during the *OFF* state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP}, can be calculated as shown in Equation 3.

$$I_{OCP} = \frac{V_{TRIP}}{\left(32 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{R_{TRIP}}{12.3} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{3}$$

where

- R_{TRIP} is in kΩ

In an overcurrent or short circuit condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to decrease. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms with 0.7 ms sort-start), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

For the TPS53318, the OCP threshold is internally clamped to 10.5 A. The R_{TRIP} for TPS53318 should be less than 150 kΩ.

Overvoltage and Undervoltage Protection

The TPS53318 and TPS53319 monitor the resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the TPS53319 latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (16 ms with 0.7 ms soft-start). This function is enabled 1.5-ms after the soft-start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. Before the latch-off action for both the high-side and low-side drivers, the output voltage must be pulled down below the UVP threshold voltage for a period of 1 ms. After the 1 ms period, the drivers are latched off.

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Redundant Overvoltage Protection (OVP)

The TPS53318 and TPS53319 have a redundant input for OVP protection. The ROVP pin senses the voltage divided from output voltage and sends it to the OVP comparator. If this voltage is higher than 120% of the target voltage, the overvoltage protection engages and the low-side FET is turned on. When the output voltage is lower than the UVP threshold then the device latches off.

This redundant OVP function typically protects again the feedback loop open or VFB short to GND. The ROVP pin has an internal 1.5-MΩ pull-down resistor. If the redundent OVP feature is not needed then simply leave the ROVP pin floating or connect it to GND.

UVLO Protection

The TPS53318 and TPS53319 use VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than 3.95 V, the device shuts off. When the VREG voltage is higher than 4.2V, the device restarts. This is a non-latch protection.

Thermal Shutdown

The TPS53318 and TPS53319 monitor the internal die temperature. If the temperature exceeds the threshold value (typically 145°C), the device shuts down. When the temperature falls about 10°C below the threshold value, the device will turn back on. This is a non-latch protection.

Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in Figure 44.

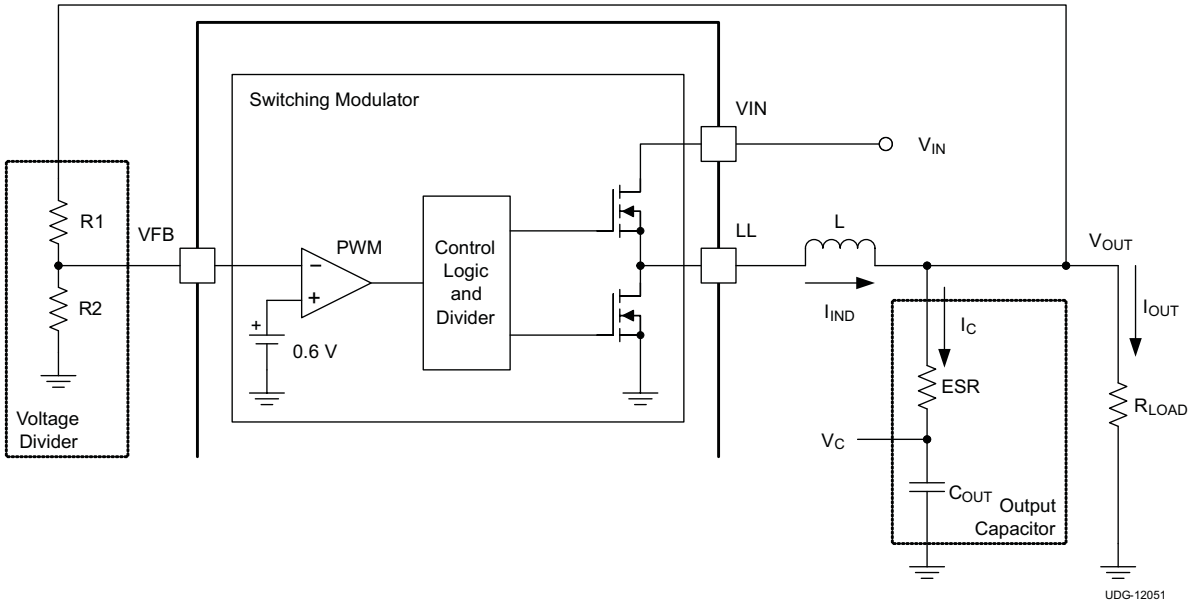


Figure 44. Simplified Modulator Model

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on cycle substantially constant.

$$H(s) = \frac{1}{s \times ESR \times C_{OUT}} \tag{4}$$

For loop stability, the 0-dB frequency, f_0, defined below need to be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \le \frac{f_{SW}}{4} \tag{5}$$

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According to the equation above, the loop stability of D-CAP™ mode modulator is mainly determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have an output capacitance in the order of several 100 µF and ESR in range of 10 mΩ. These makes f_0 on the order of 100 kHz or less, creating a stable loop. However, ceramic capacitors have an f_0 at more than 700 kHz, and need special care when used with this modulator. An application circuit for ceramic capacitor is described in the External Component Selection Using All Ceramic Output Capacitors section.

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External Component Selection

The external components selection is a simple process when using organic semiconductors or special polymer output capacitors.

1. SELECT OPERATION MODE AND SOFT-START TIME

   Select operation mode and soft-start time using Table 1.

2. SELECT SWITCHING FREQUENCY

   Select the switching frequency from 250 kHz to 1 MHz using Table 2.

3. CHOOSE THE INDUCTOR

   The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps ensure stable operation, but increases inductor core loss. Using 1/3 ripple current to maximum output current ratio, the inductance can be determined by Equation 6.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (6)$$

   The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 7.

$$I_{IND(peak)} = \frac{V_{TRIP}}{32 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (7)$$

4. CHOOSE THE OUTPUT CAPACITOR(S)

   When organic semiconductor capacitor(s) or specialty polymer capacitor(s) are used, for loop stability, capacitance and ESR should satisfy Equation 5. For jitter performance, Equation 8 is a good starting point to determine ESR.

$$ESR = \frac{V_{OUT} \times 10\,mV \times (1 - D)}{0.6\,V \times I_{IND(ripple)}} = \frac{10\,mV \times L \times f_{SW}}{0.6\,V} = \frac{L \times f_{SW}}{60}(\Omega) \quad (8)$$

   where

   - D is the duty factor.
   - The required output ripple slope is approximately 10 mV per t_{SW} (switching period) in terms of VFB terminal voltage.

5. DETERMINE THE VALUE OF R1 AND R2

   The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 44. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is from 10 kΩ to 20 kΩ. Determine R1 using Equation 9.

$$R1 = \frac{V_{OUT} - \frac{I_{IND(ripple)} \times ESR}{2} - 0.6}{0.6} \times R2 \quad (9)$$

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6. CHOOSE THE OVERCURRENT SETTING RESISTOR

The overcurrent setting resistor, R_{TRIP}, can be determined by Equation 10.

$$R_{TRIP} = \left(I_{OCP} - \left(\frac{1}{2 \times L \times f_{SW}} \right) \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \right) \times 12.3 \quad (10)$$

where

- R_{TRIP} is in kΩ

External Component Selection Using All Ceramic Output Capacitors

When a ceramic output capacitor is used, the stability criteria in Equation 5 cannot be satisfied. The ripple injection approach as shown in Figure 2 is implemented to increase the ripple on the VFB pin and make the system stable. In addition to the selections made using steps 1 through step 6 in the External Component Selection section, the ripple injection components must be selected. The C2 value can be fixed at 1 nF. The value of C1 can be selected between 10 nF to 200 nF.

$$\frac{L \times C_{OUT}}{R7 \times C1} > N \times \frac{t_{ON}}{2} \quad (11)$$

where

- N is the coefficient to account for L and C_{OUT} variation

N is also used to provide enough margin for stability. It is recommended N=2 for $V_{OUT} \leq 1.8$ V and N=4 for $V_{OUT} \geq 3.3$ V or when L ≤ 250 nH. The higher V_{OUT} needs a higher N value because the effective output capacitance is reduced significantly with higher DC bias. For example, a 6.3-V, 22-µF ceramic capacitor may have only 8 µF of effective capacitance when biased at 5 V.

Because the VFB pin voltage is regulated at the valley, the increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from the VOUT pin and they can be calculated using Equation 12 and Equation 13 when neglecting the output voltage ripple caused by equivalent series inductance (ESL).

$$V_{INJ_SW} = \frac{V_{IN} - V_{OUT}}{R7 \times C1} \times \frac{D}{f_{SW}} \quad (12)$$

$$V_{INJ_OUT} = ESR \times I_{IND(ripple)} + \frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (13)$$

It is recommended that V_{INJ_SW} to be less than 50 mV. If the calculated V_{INJ_SW} is higher than 50 mV, then other parameters need to be adjusted to reduce it. For example, C_{OUT} can be increased to satisfy Equation 11 with a higher R7 value, thereby reducing V_{INJ_SW}.

The DC voltage at the VFB pin can be calculated by Equation 14:

$$V_{VFB} = 0.6 + \frac{V_{INJ_SW} + V_{INJ_OUT}}{2} \quad (14)$$

And the resistor divider value can be determined by Equation 15:

$$R1 = \frac{V_{OUT} - V_{VFB}}{V_{VFB}} \times R2 \quad (15)$$

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LAYOUT CONSIDERATIONS

Certain points must be considered before beginining a design using the TPS53318 or TPS53319.

- The power components (including input/output capacitors, inductor and TPS53318 or TPS53319) should be placed on one side of the PCB (solder side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as LL, VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC current loop.
- Because the TPS53319 controls output voltage referring to voltage across VOUT capacitor, the top-side resistor of the voltage divider should be connected to the positive node of the VOUT capacitor. The GND of the bottom side resistor should be connected to the GND pad of the device. The trace from these resistors to the VFB pin should be short and thin.
- Place the frequency setting resistor (R_F), OCP setting resistor (R_{TRIP}) and mode setting resistor (R_{MODE}) as close to the device as possible. Use the common GND via to connect them to GND plane if applicable.
- Place the VDD and VREG decoupling capacitors as close to the device as possible. Ensure to provide GND vias for each decoupling capacitor and make the loop as small as possible.
- The PCB trace defined as switch node, which connects the LL pins and high-voltage side of the inductor, should be as short and wide as possible.
- Connect the ripple injection V_{OUT} signal (V_{OUT} side of the C1 capacitor in Figure 2) from the terminal of ceramic output capacitor. The AC coupling capacitor (C2 in Figure 2) should be placed near the device, and R7 and C1 can be placed near the power stage.
- Use separated vias or trace to connect LL node to snubber, boot strap capacitor and ripple injection resistor. Do not combine these connections.

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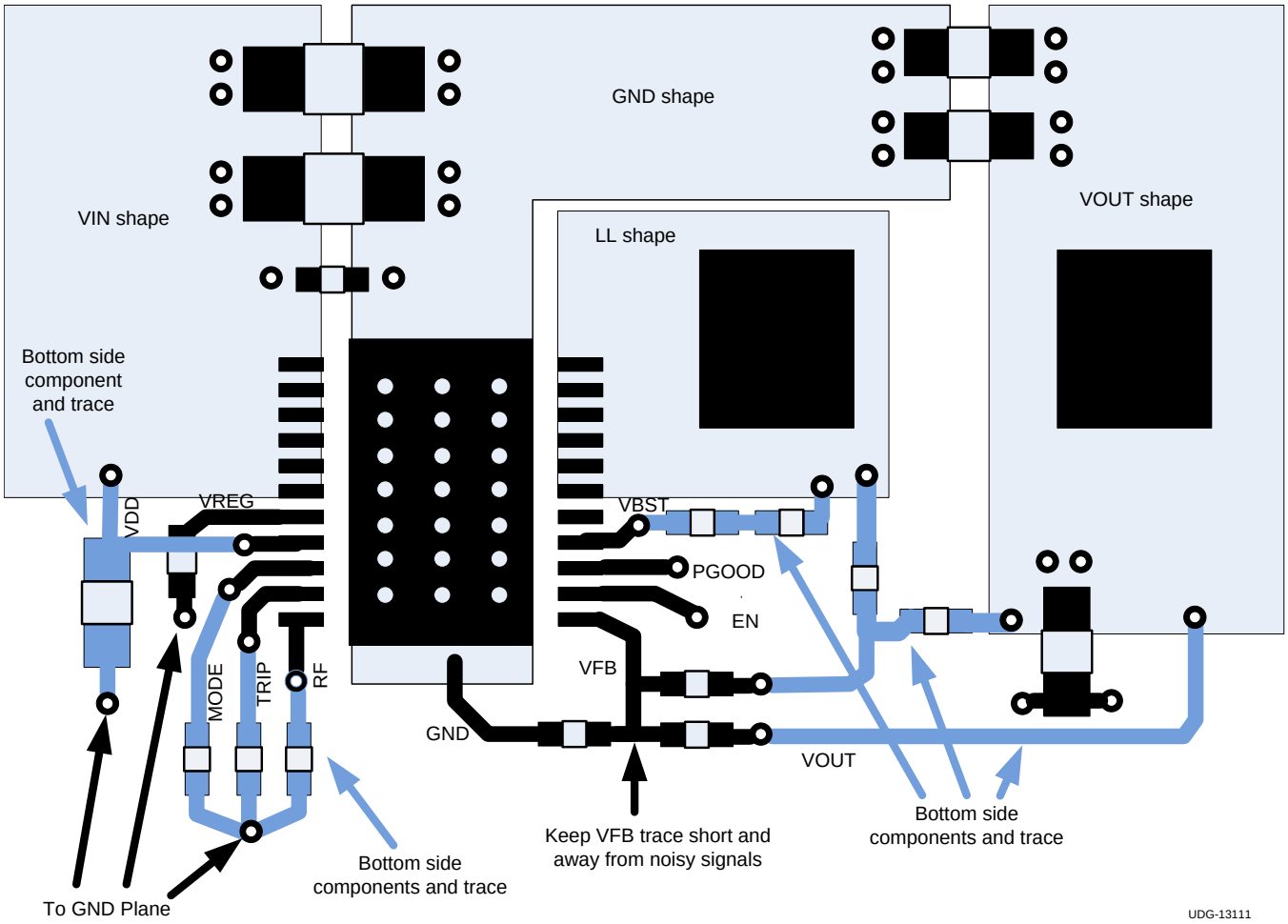


Figure 45. Layout Recommendation

REVISION HISTORY

Changes from Original (JUNE 2012) to Revision A **Page**

- Changed "<100 µA Shut Down Current" to "<110 µA Shut Down Current" in FEATURES 1
- Changed "Green (RoHS and no Pb/Br)" to "Pb-Free (RoHS Exempt)" in ORDERING INFORMATION table 2

Changes from Revision A (AUGUST 2012) to Revision B **Page**

- Added clarity to Overvoltage and Undervoltage Protection section 19
- Changed updated Figure 45 25

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS53318DQPR	ACTIVE	SON	DQP	22	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	53318DQP	Samples
TPS53318DQPT	ACTIVE	SON	DQP	22	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	53318DQP	Samples
TPS53319DQPR	ACTIVE	SON	DQP	22	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	53319DQP	Samples
TPS53319DQPT	ACTIVE	SON	DQP	22	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	53319DQP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

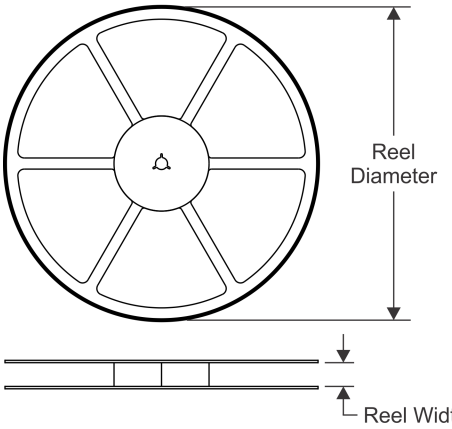
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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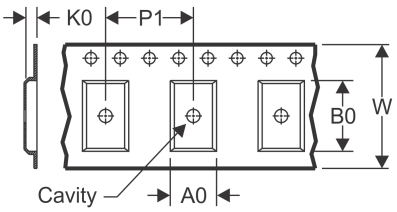
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

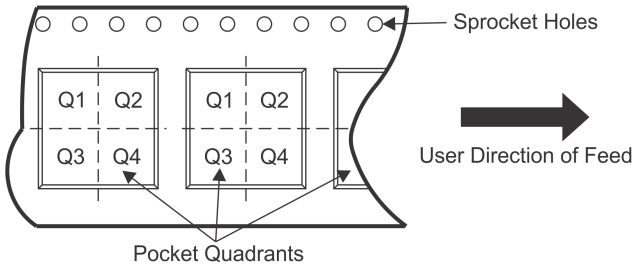


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

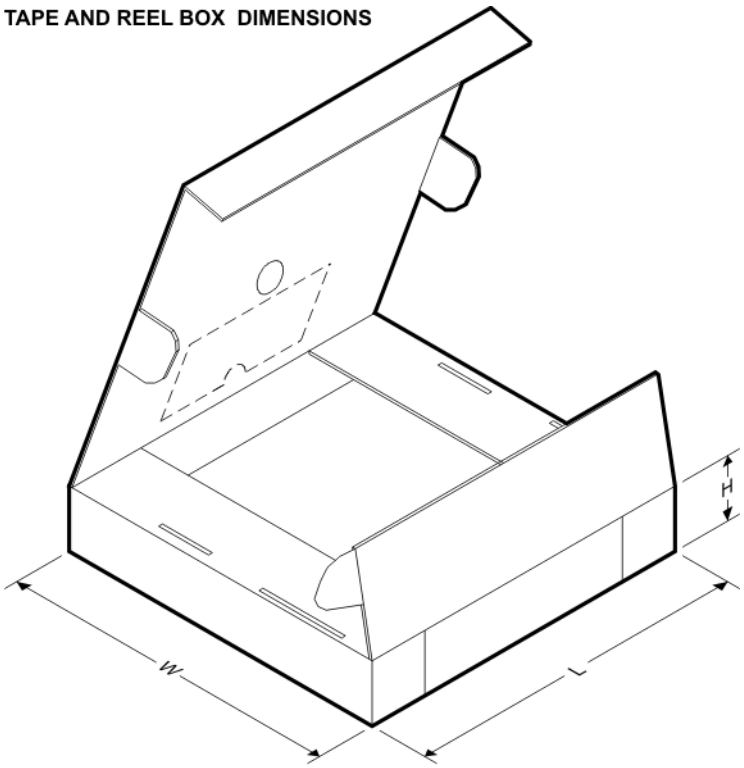
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53318DQPR	SON	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53318DQPT	SON	DQP	22	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53319DQPR	SON	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53319DQPT	SON	DQP	22	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

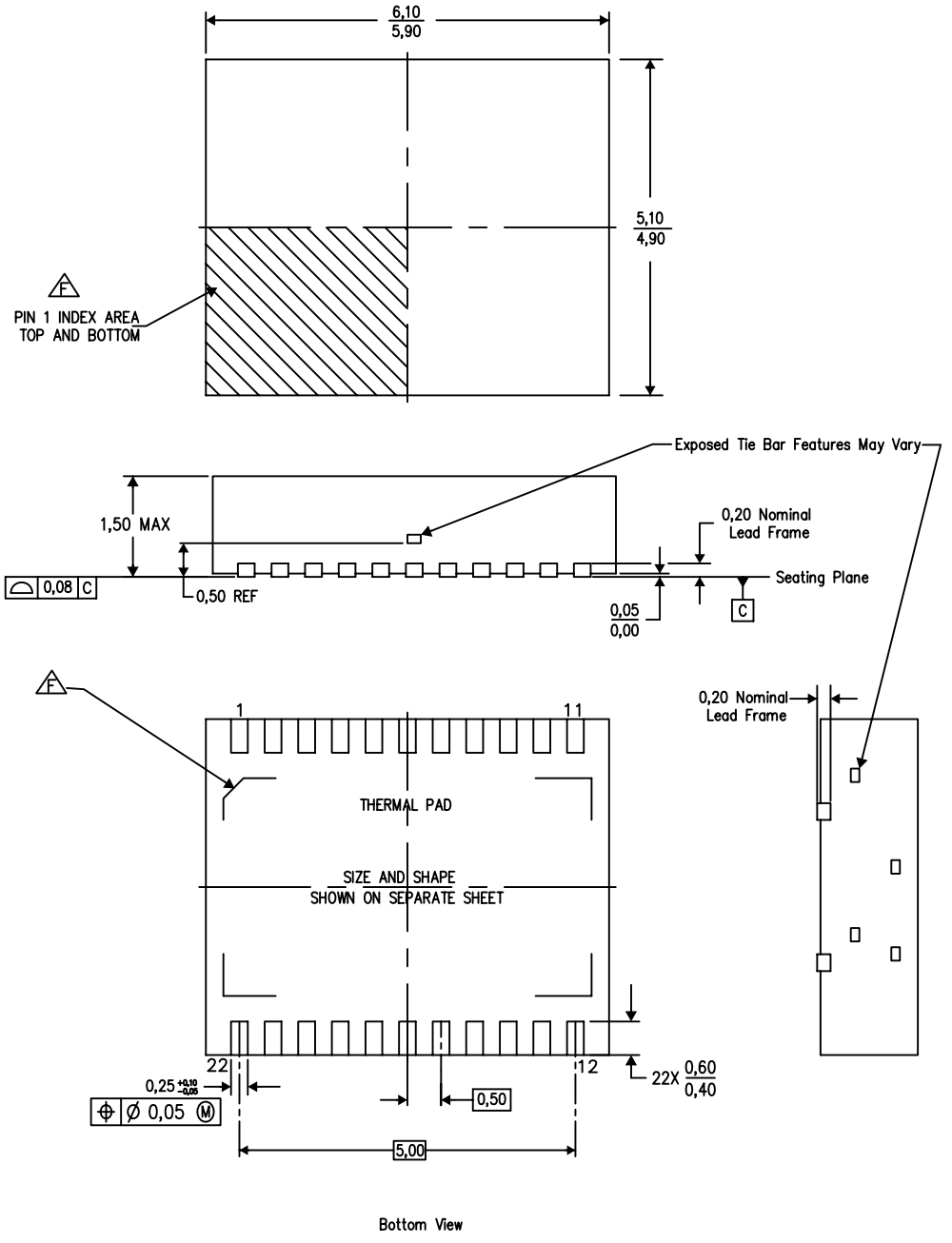
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53318DQPR	SON	DQP	22	2500	367.0	367.0	35.0
TPS53318DQPT	SON	DQP	22	250	210.0	185.0	35.0
TPS53319DQPR	SON	DQP	22	2500	367.0	367.0	35.0
TPS53319DQPT	SON	DQP	22	250	210.0	185.0	35.0

DQP (R–PSON–N22) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

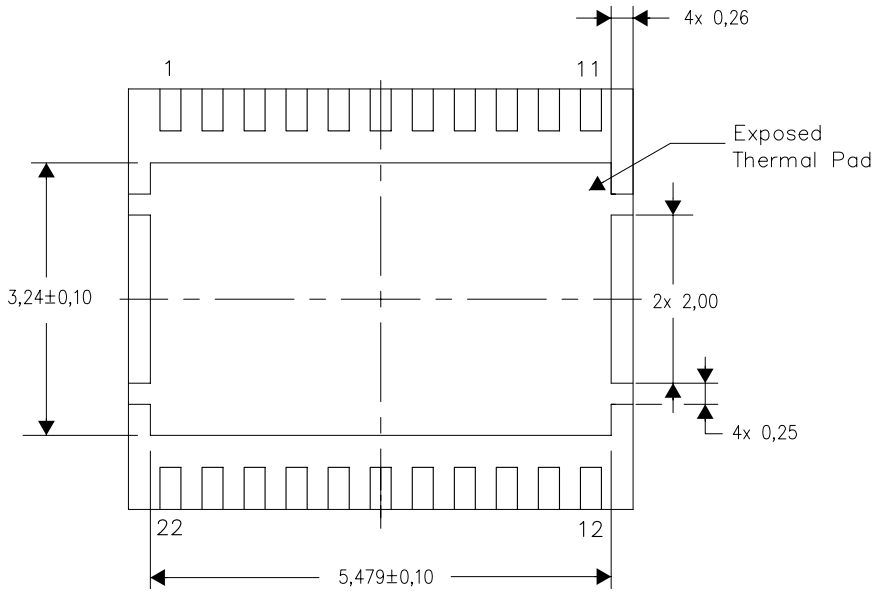
DQP (R–PSON–N22) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



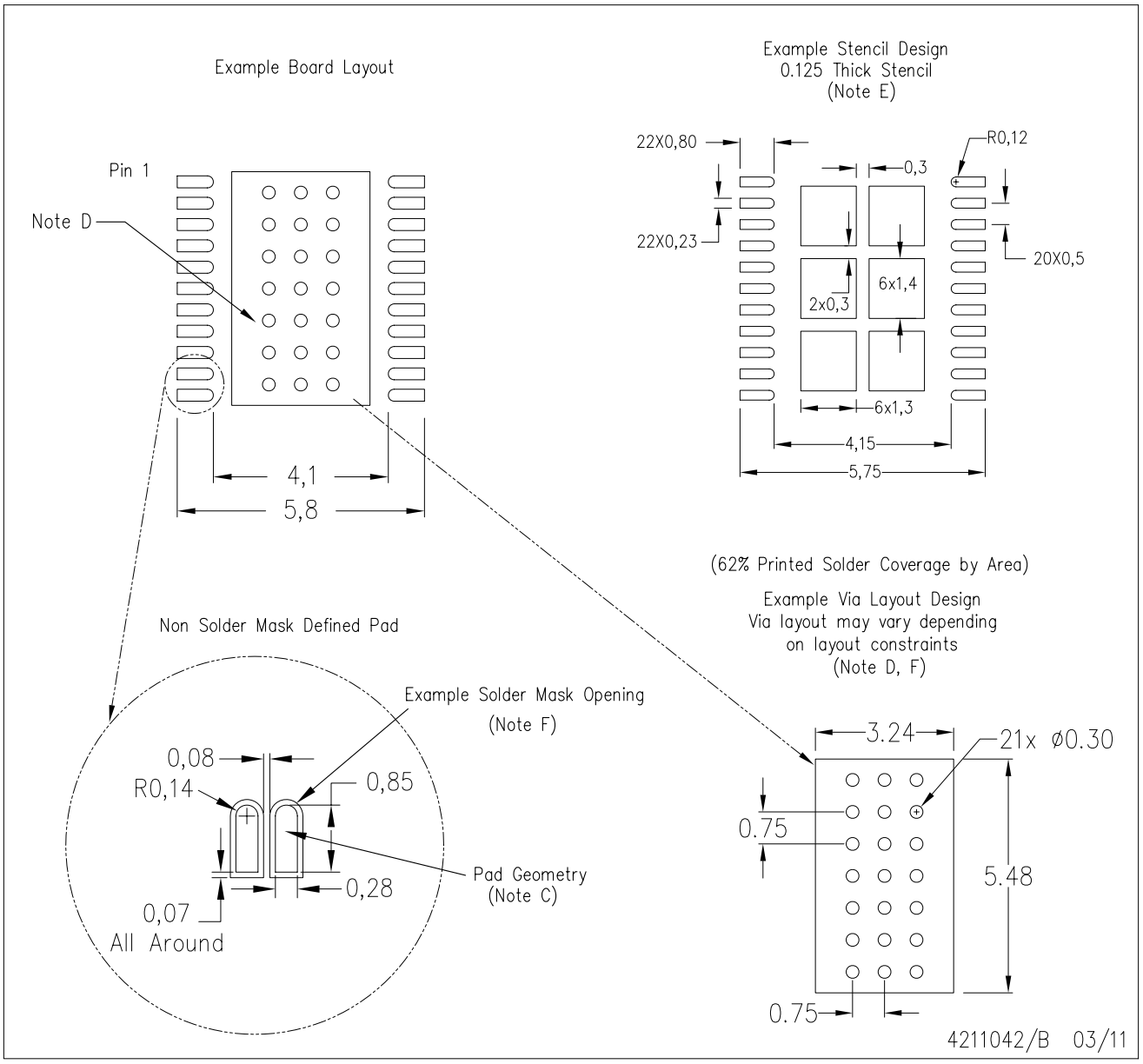
Bottom View

Exposed Thermal Pad Dimensions

4211024–3/E 03/12

NOTE: All linear dimensions are in millimeters

DQP (R–PSON–N22) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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