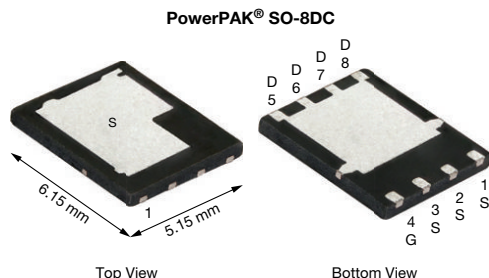


N-Channel 100 V (D-S) MOSFET



FEATURES

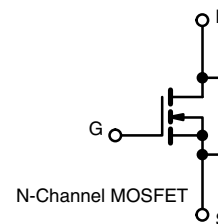
- TrenchFET® Gen IV power MOSFET
- Very low $R_{DS(on)}$ - Q_g figure-of-merit (FOM)
- Tuned for the lowest $R_{DS(on)}$ - Q_{oss} FOM
- Top side cooling feature provides additional venue for thermal transfer
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converters
- OR-ing
- Power supplies
- Motor drive control
- Battery and load switch



PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00480
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.00505
Q_g typ. (nC)	55
I_D (A)	95
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8DC
Lead (Pb)-free and halogen-free	SiDR668DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	95	A
	$T_C = 70$ °C		76	
	$T_A = 25$ °C		23.2 ^{b, c}	
	$T_A = 70$ °C		18.6 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)		I_{DM}	200	
Continuous source-drain diode current	$T_C = 25$ °C	I_S	94	
	$T_A = 25$ °C		5.6 ^{b, c}	
Single pulse avalanche current	$L = 0.1$ mH	I_{AS}	35	mJ
Single pulse avalanche energy		E_{AS}	61.2	
Maximum power dissipation	$T_C = 25$ °C	P_D	125	W
	$T_C = 70$ °C		80	
	$T_A = 25$ °C		6.25 ^{b, c}	
	$T_A = 70$ °C		4 ^{b, c}	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) °C			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	$t \leq 10$ s	R_{thJA}	15	20	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	0.8	1	
Maximum junction-to-case (source)	Steady state	R_{thJC}	1.1	1.4	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 54 °C/W
- $T_C = 25$ °C



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	70	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-7.2	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	-	3.4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	40	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.00400	0.00480	Ω
		V _{GS} = 7.5 V, I _D = 15 A	-	0.00420	0.00505	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A	-	85	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	-	5400	-	pF
Output capacitance	C _{oss}		-	280	-	
Reverse transfer capacitance	C _{rss}		-	38	-	
Total gate charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 10 A	-	72	108	nC
		V _{DS} = 50 V, V _{GS} = 7.5 V, I _D = 10 A	-	55	83	
Gate-source charge	Q _{gs}		-	21.6	-	
Gate-drain charge	Q _{gd}		-	12	-	
Output charge	Q _{oss}	V _{DS} = 50 V, V _{GS} = 0 V	-	61	-	
Gate resistance	R _g	f = 1 MHz	0.3	0.9	1.6	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	17	34	ns
Rise time	t _r		-	22	44	
Turn-off delay time	t _{d(off)}		-	30	60	
Fall time	t _f		-	11	22	
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω, I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	22	44	
Rise time	t _r		-	25	50	
Turn-off delay time	t _{d(off)}		-	38	76	
Fall time	t _f		-	28	56	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	94	A
Pulse diode forward current	I _{SM}		-	-	200	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.73	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	59	118	ns
Body diode reverse recovery charge	Q _{rr}		-	115	230	nC
Reverse recovery fall time	t _a		-	37	-	ns
Reverse recovery rise time	t _b		-	22	-	

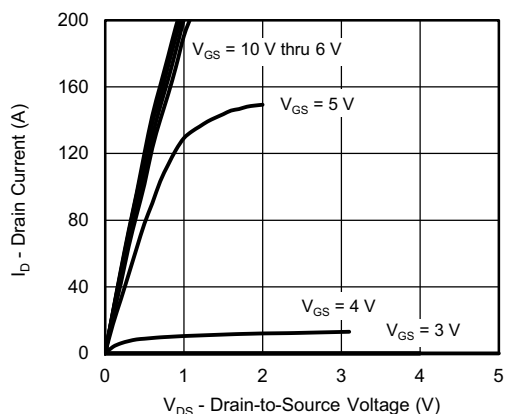
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

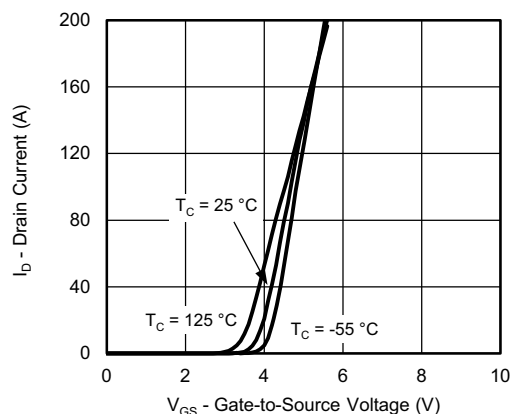
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



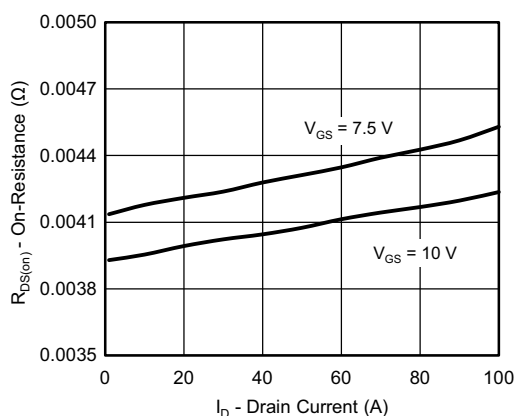
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



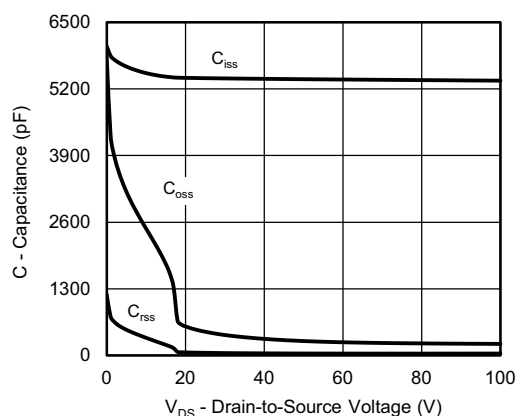
Output Characteristics



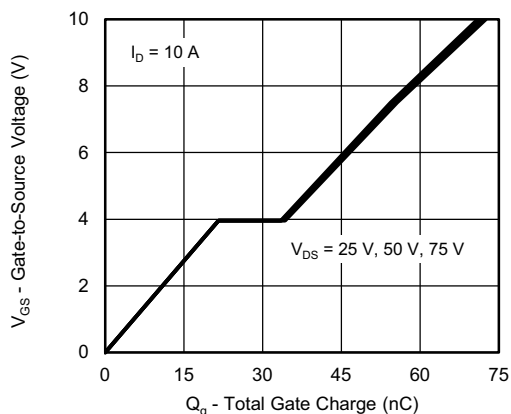
Transfer Characteristics



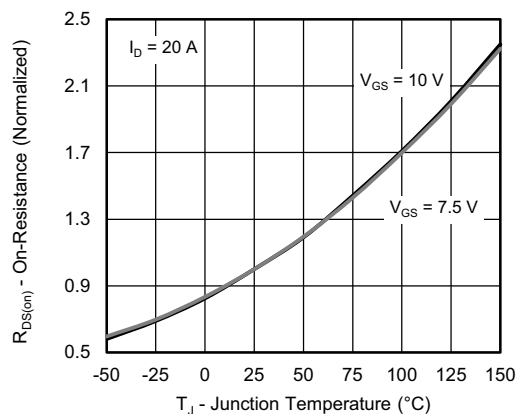
On-Resistance vs. Drain Current and Gate Voltage



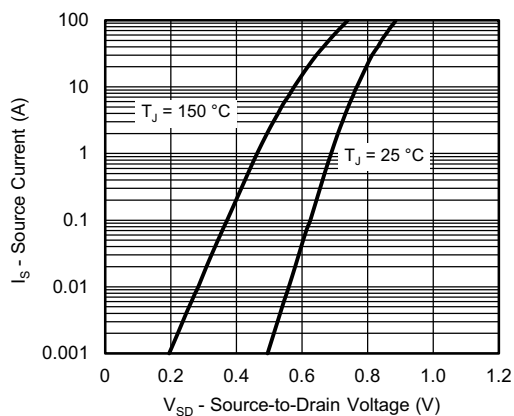
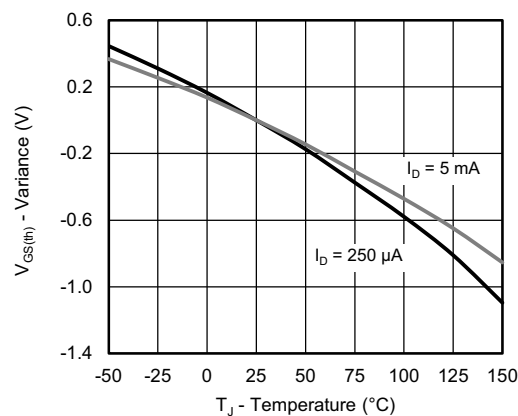
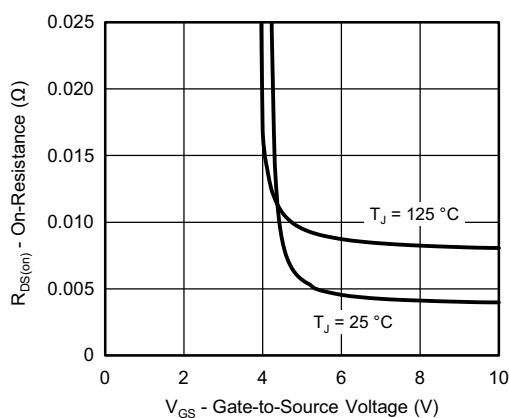
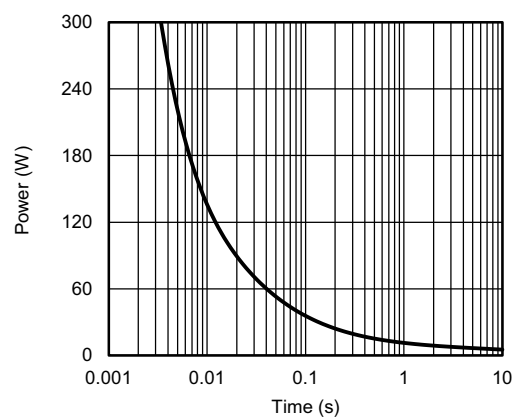
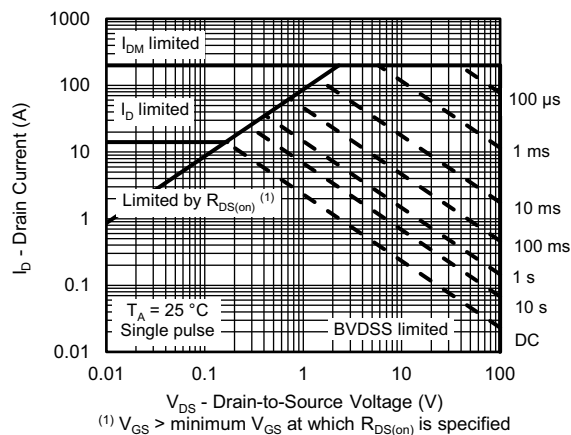
Capacitance



Gate Charge

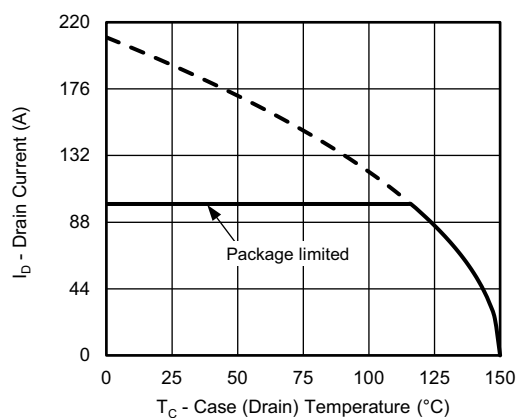


On-Resistance vs. Junction Temperature

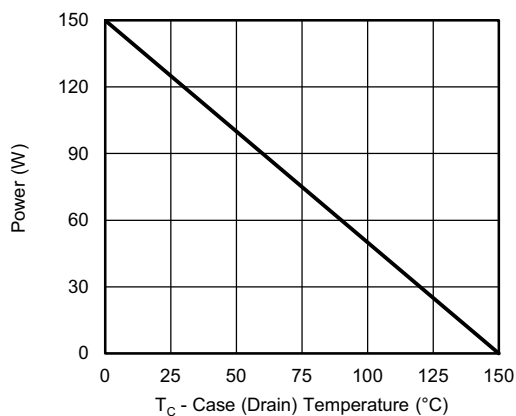
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient



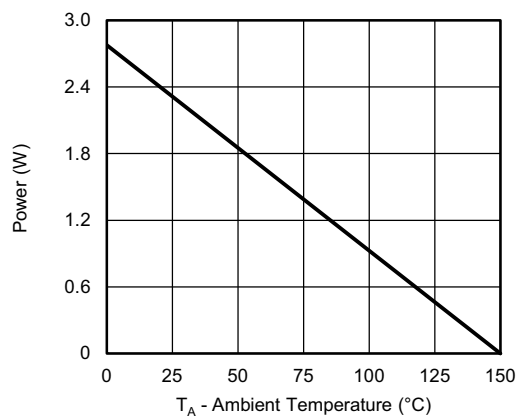
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



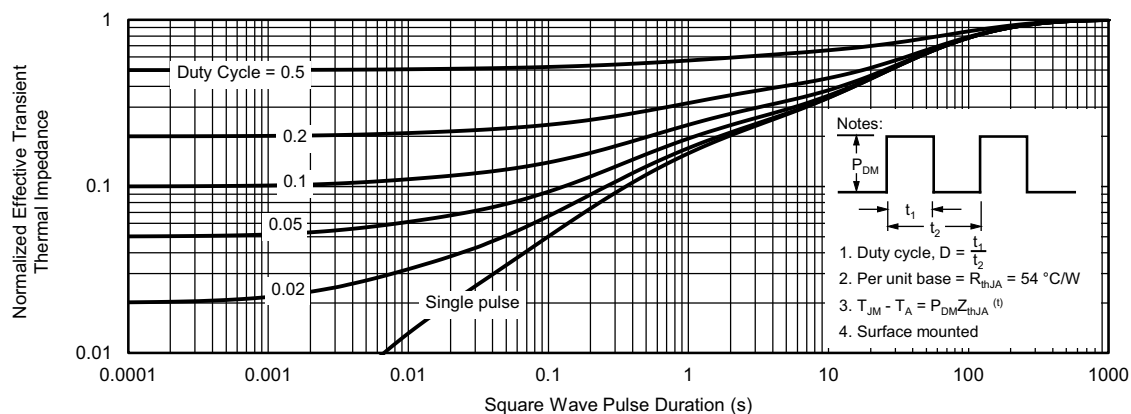
Power, Junction-to-Ambient

Note

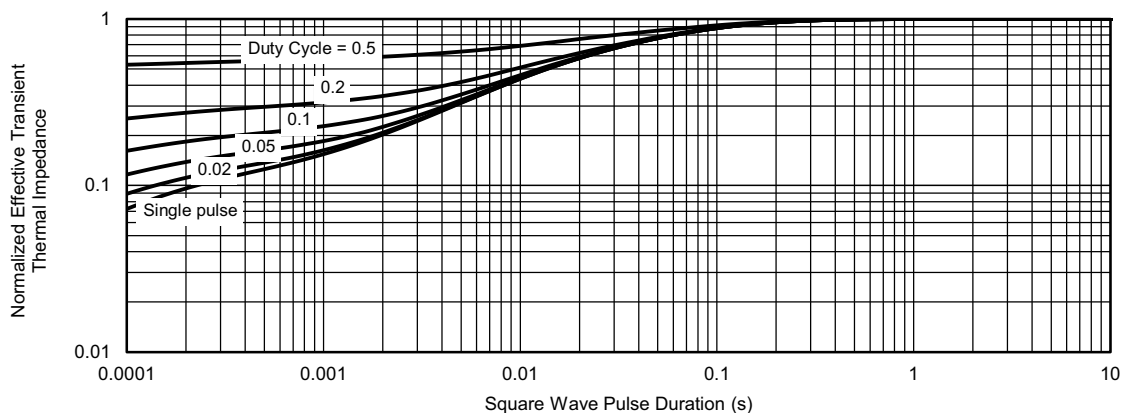
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



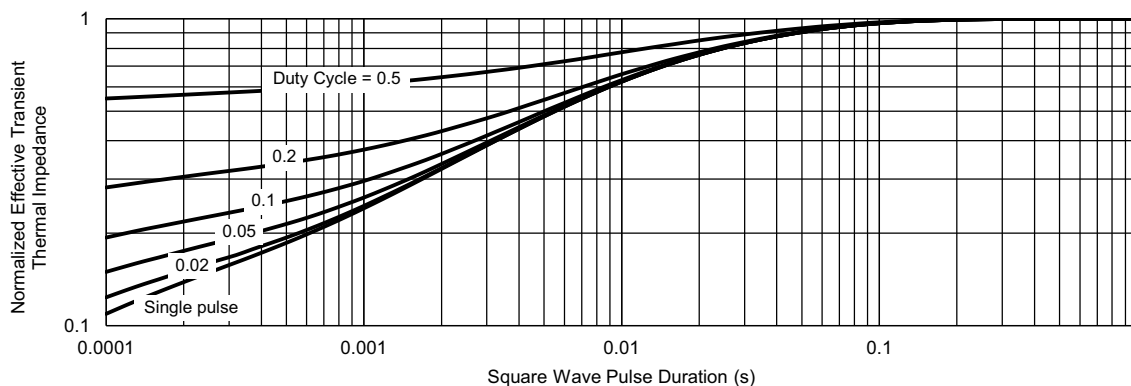
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain)

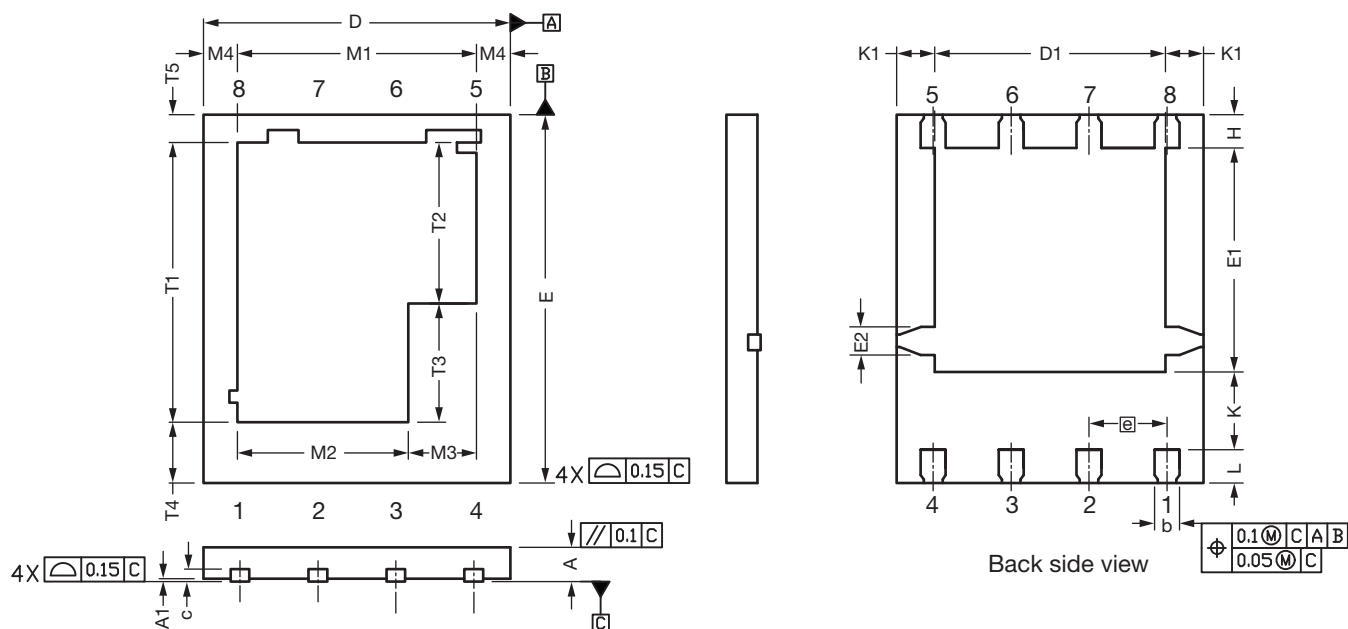


Normalized Thermal Transient Impedance, Junction-to-Case (Source)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75751.

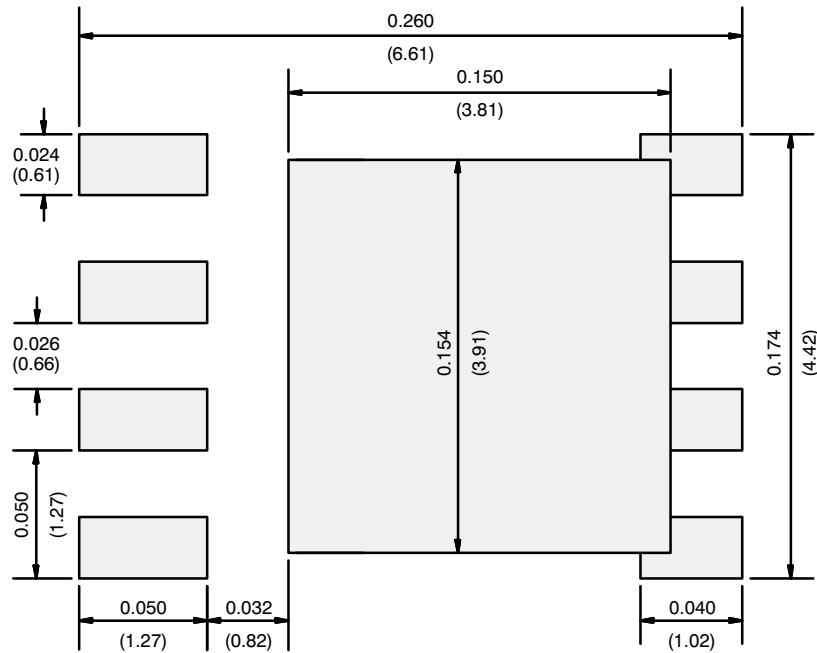


PowerPAK® SO-8 Double Cooling Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.51	0.56	0.61	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.36	0.41	0.46	0.014	0.016	0.018
c	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	3.71	3.76	3.81	0.146	0.148	0.150
e	1.27 BSC			0.050 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.60	3.65	3.70	0.142	0.144	0.146
E2	0.46 typ.			0.018 typ.		
H	0.49	0.54	0.59	0.019	0.021	0.023
K	1.22	1.27	1.32	0.048	0.050	0.052
K1	0.64 typ.			0.025 typ.		
L	0.49	0.54	0.59	0.019	0.021	0.023
M1	3.8	3.90	4.00	0.150	0.154	0.158
M2	2.69	2.79	2.89	0.106	0.110	0.114
M3	1.01	1.11	1.21	0.040	0.044	0.048
M4	0.56 typ.			0.022 typ.		
N	8			8		
T1	4.46	4.56	4.66	0.176	0.180	0.184
T2	2.53	2.63	2.73	0.100	0.104	0.108
T3	1.83	1.93	2.03	0.072	0.076	0.080
T4	0.97 typ.			0.038 typ.		
T5	0.48 typ.			0.019 typ.		
ECN: T24-0304-Rev. C, 29-Jul-2024						
DWG: 6048						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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