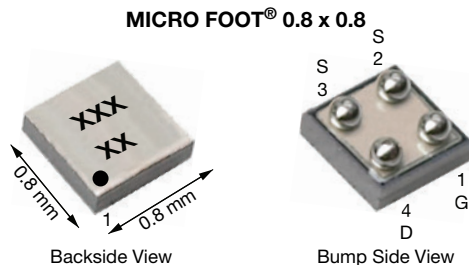


P-Channel 20 V (D-S) MOSFET



Marking code: AF

PRODUCT SUMMARY	
V_{DS} (V)	-20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.076
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -2.5$ V	0.100
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.8$ V	0.145
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.5$ V	0.320
Q_g typ. (nC)	7.5
I_D (A) ^{a, e}	-2.9
Configuration	Single

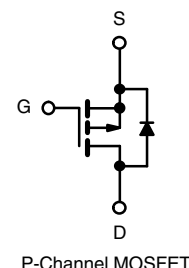
FEATURES

- TrenchFET[®] power MOSFET
- Small 0.8 mm x 0.8 mm outline area
- Low 0.4 mm max. profile
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load switches and chargers switches
- Battery management
- DC/DC converters
- For smart phones and tablet PCs



P-Channel MOSFET

ORDERING INFORMATION	
Package	MICRO FOOT 0.8 x 0.8
Lead (Pb)-free and halogen-free	Si8817DB-T2-E1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GS}	± 8	
Continuous drain current ($T_J = 150$ °C)	$T_A = 25$ °C	I_D	-2.9 ^a	A
	$T_A = 70$ °C		-2.3 ^a	
	$T_A = 25$ °C		-2.1 ^b	
	$T_A = 70$ °C		-1.7 ^b	
Pulsed drain current ($t = 300$ μ s)		I_{DM}	-15	
Continuous source-drain diode current	$T_C = 25$ °C	I_S	-0.7 ^a	
	$T_A = 25$ °C		-0.4 ^b	
Maximum power dissipation	$T_A = 25$ °C	P_D	0.9 ^a	W
	$T_A = 70$ °C		0.6 ^a	
	$T_A = 25$ °C		0.5 ^b	
	$T_A = 70$ °C		0.3 ^b	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Package reflow conditions ^c	VPR		260	
	IR/convection		260	

Notes

- Surface mounted on 1" x 1" FR4 board with full copper, $t = 5$ s
- Surface mounted on 1" x 1" FR4 board with minimum copper, $t = 5$ s
- Refer to IPC/JEDEC[®] (J-STD-020), no manual or hand soldering
- In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump
- Based on $T_A = 25$ °C

**THERMAL RESISTANCE RATINGS**

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, b}	$t = 5 \text{ s}$	R_{thJA}	105	135	$^{\circ}\text{C/W}$
Maximum junction-to-ambient ^{c, d}	$t = 5 \text{ s}$		200	260	

Notes

- a. Surface mounted on 1" x 1" FR4 board with full copper
b. Maximum under steady state conditions is 185 $^{\circ}\text{C/W}$
c. Surface mounted on 1" x 1" FR4 board with minimum copper
d. Maximum under steady state conditions is 330 $^{\circ}\text{C/W}$

SPECIFICATIONS ($T_J = 25^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{\text{GS}} = 0 \text{ V}, I_{\text{D}} = -250 \mu\text{A}$	-20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{\text{DS}}/T_J$	$I_{\text{D}} = -250 \mu\text{A}$	-	-12	-	$\text{mV}/^{\circ}\text{C}$
$V_{\text{GS(th)}}$ temperature coefficient	$\Delta V_{\text{GS(th)}}/T_J$		-	2.5	-	
Gate-source threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = -250 \mu\text{A}$	-0.4	-	-1	V
Gate-source leakage	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = \pm 8 \text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}} = -20 \text{ V}, V_{\text{GS}} = 0 \text{ V}$	-	-	-1	μA
		$V_{\text{DS}} = -20 \text{ V}, V_{\text{GS}} = 0 \text{ V}, T_J = 70^{\circ}\text{C}$	-	-	-10	
On-state drain current ^a	$I_{\text{D(on)}}$	$V_{\text{DS}} \leq -5 \text{ V}, V_{\text{GS}} = -4.5 \text{ V}$	-5	-	-	A
Drain-source on-state resistance ^a	$R_{\text{DS(on)}}$	$V_{\text{GS}} = -4.5 \text{ V}, I_{\text{D}} = -1 \text{ A}$	-	0.061	0.076	Ω
		$V_{\text{GS}} = -2.5 \text{ V}, I_{\text{D}} = -1 \text{ A}$	-	0.080	0.100	
		$V_{\text{GS}} = -1.8 \text{ V}, I_{\text{D}} = -0.5 \text{ A}$	-	0.110	0.145	
		$V_{\text{GS}} = -1.5 \text{ V}, I_{\text{D}} = -0.5 \text{ A}$	-	0.165	0.320	
Forward transconductance ^a	g_{fs}	$V_{\text{DS}} = -10 \text{ V}, I_{\text{D}} = -1 \text{ A}$	-	5	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{\text{DS}} = -10 \text{ V}, V_{\text{GS}} = 0 \text{ V}, f = 1 \text{ MHz}$	-	615	-	pF
Output capacitance	C_{oss}		-	90	-	
Reverse transfer capacitance	C_{rss}		-	75	-	
Total gate charge	Q_{g}	$V_{\text{DS}} = -10 \text{ V}, V_{\text{GS}} = -8 \text{ V}, I_{\text{D}} = -1 \text{ A}$	-	12.5	19	nC
		$V_{\text{DS}} = -10 \text{ V}, V_{\text{GS}} = -4.5 \text{ V}, I_{\text{D}} = -1 \text{ A}$	-	7.5	12	
Gate-source charge	Q_{gs}		-	1	-	
Gate-drain charge	Q_{gd}		-	1.9	-	
Gate resistance	R_{g}	$V_{\text{GS}} = -0.1 \text{ V}, f = 1 \text{ MHz}$	-	14	-	Ω
Turn-on delay time	$t_{\text{d(on)}}$	$V_{\text{DD}} = -10 \text{ V}, R_{\text{L}} = 10 \Omega$ $I_{\text{D}} \cong -1 \text{ A}, V_{\text{GEN}} = -4.5 \text{ V}, R_{\text{g}} = 1 \Omega$	-	20	40	ns
Rise time	t_{r}		-	20	40	
Turn-off delay time	$t_{\text{d(off)}}$		-	52	100	
Fall time	t_{f}		-	22	45	
Turn-on delay time	$t_{\text{d(on)}}$	$V_{\text{DD}} = -10 \text{ V}, R_{\text{L}} = 10 \Omega$ $I_{\text{D}} \cong -1 \text{ A}, V_{\text{GEN}} = -8 \text{ V}, R_{\text{g}} = 1 \Omega$	-	6	15	
Rise time	t_{r}		-	10	20	
Turn-off delay time	$t_{\text{d(off)}}$		-	60	120	
Fall time	t_{f}		-	23	45	



SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_A = 25\text{ }^{\circ}\text{C}$	-	-	-0.7	A
Pulse diode forward current	I_{SM}		-	-	-15	
Body diode voltage	V_{SD}	$I_S = -1\text{ A}$, $V_{GS} = 0\text{ V}$	-	-0.75	-1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = -1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$	-	30	60	ns
Body diode reverse recovery charge	Q_{rr}		-	14	30	nC
Reverse recovery fall time	t_a		-	13	-	ns
Reverse recovery rise time	t_b		-	17	-	

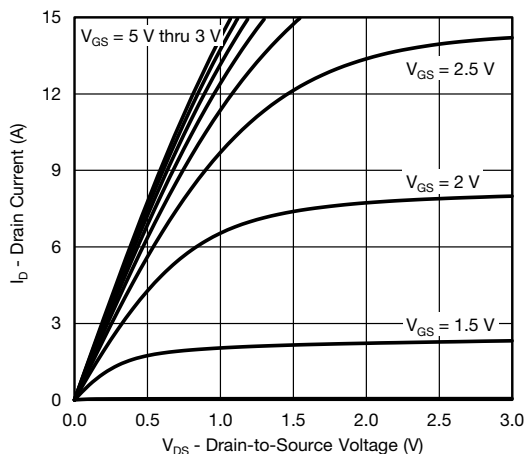
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\text{ }\%$
- Guaranteed by design, not subject to production testing

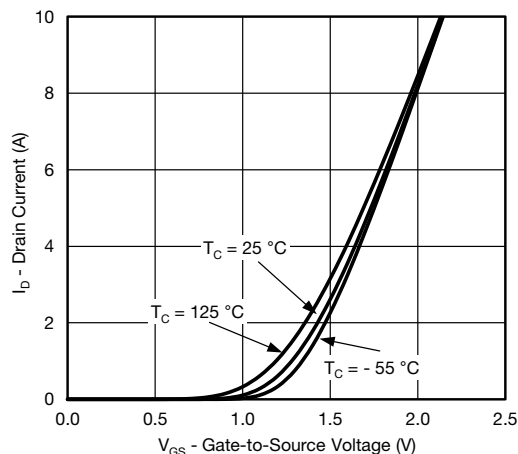
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



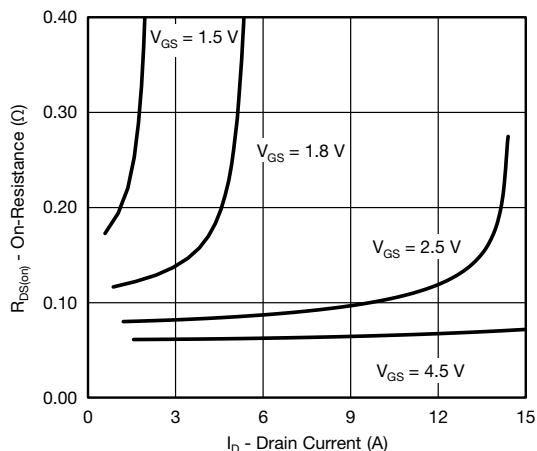
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



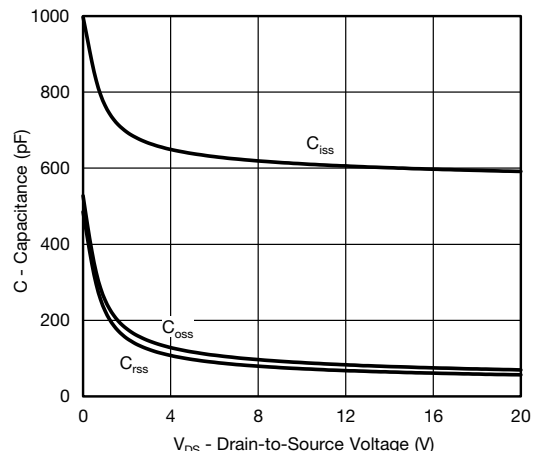
Output Characteristics



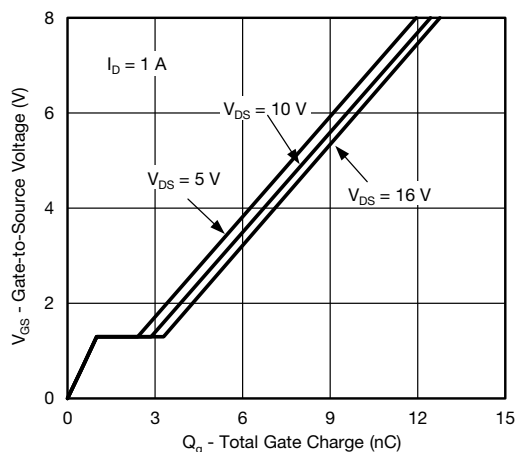
Transfer Characteristics



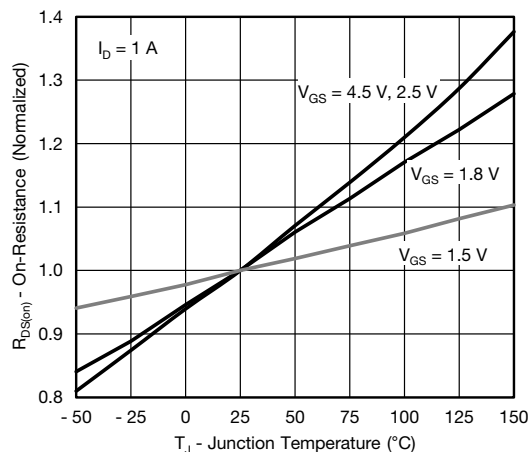
On-Resistance vs. Drain Current and Gate Voltage



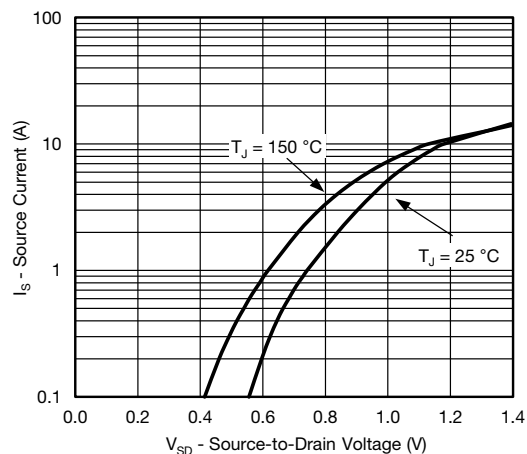
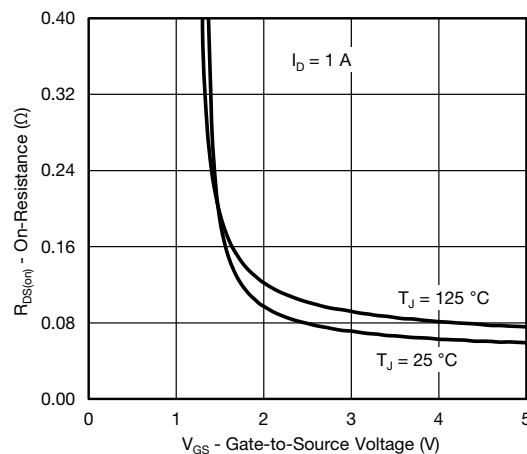
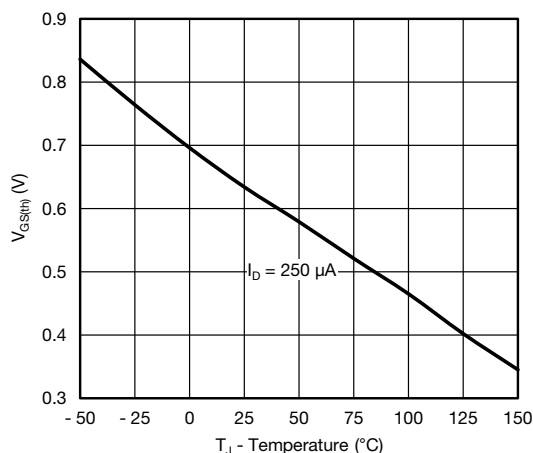
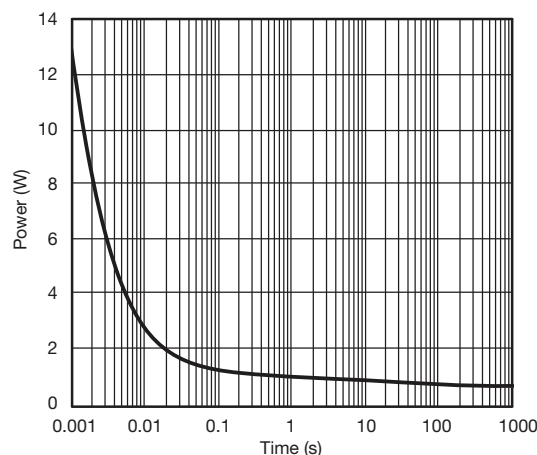
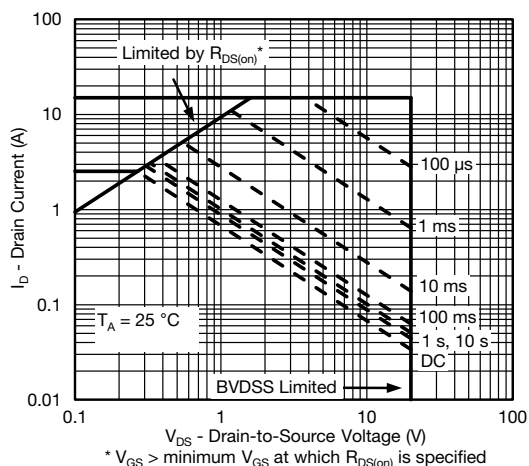
Capacitance



Gate Charge

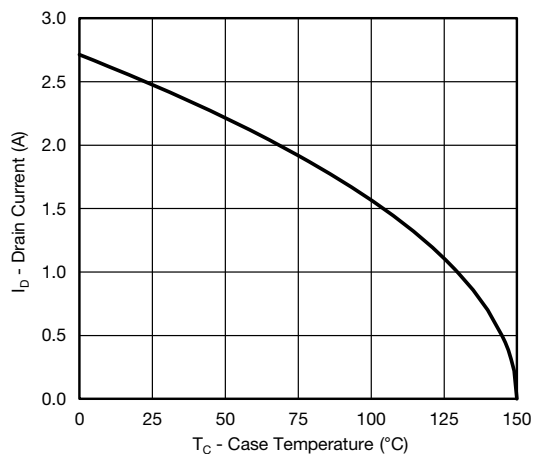


On-Resistance vs. Junction Temperature

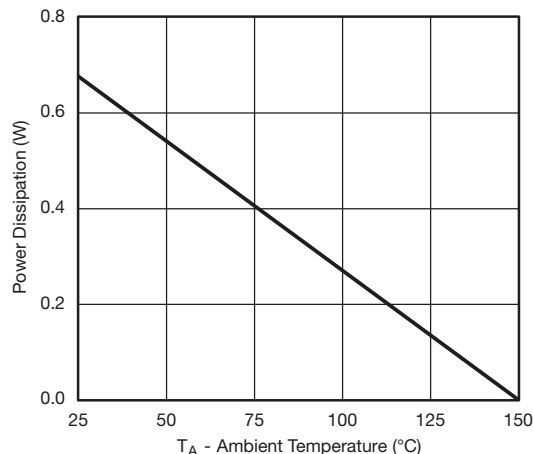
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



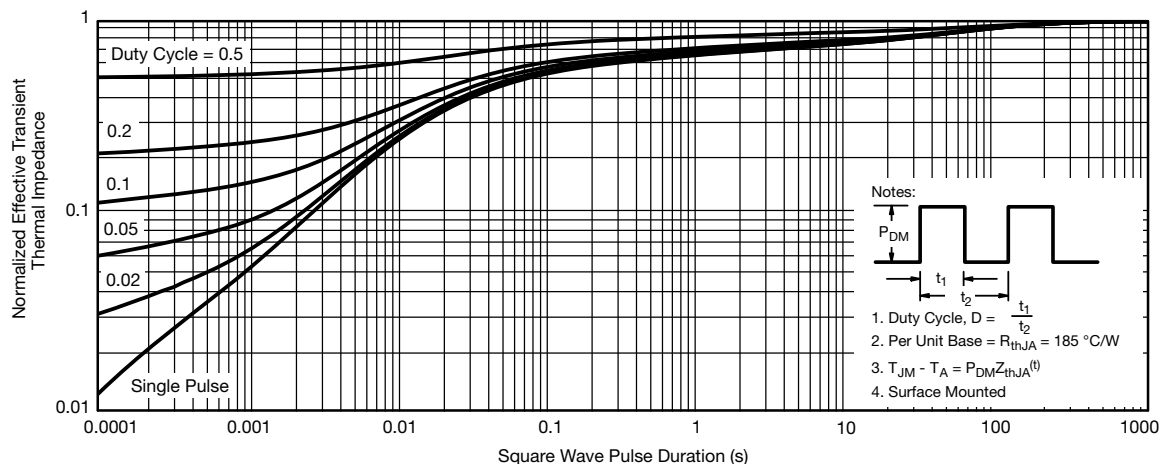
Power Derating

Notes

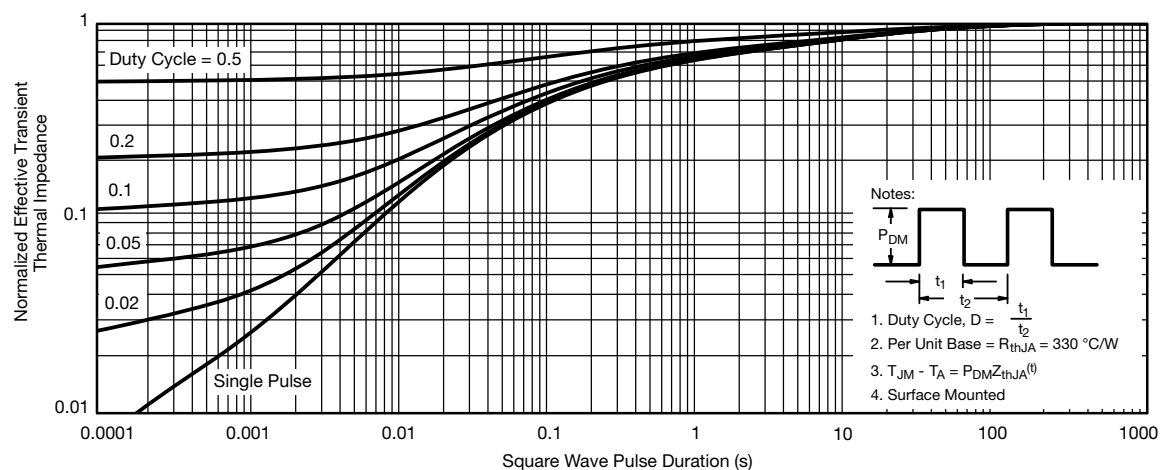
- When mounted on 1" x 1" FR4 with full copper
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 Board with Maximum Copper)

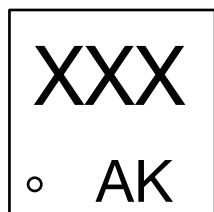


Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 Board with Minimum Copper)

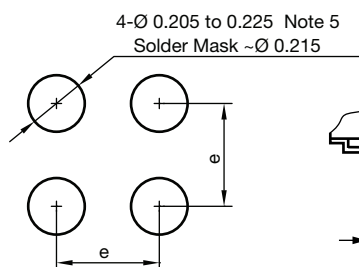
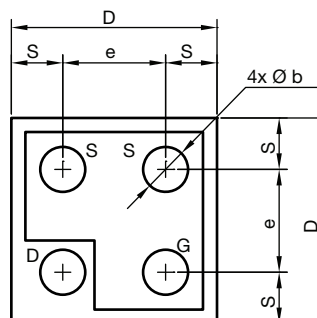
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62759.



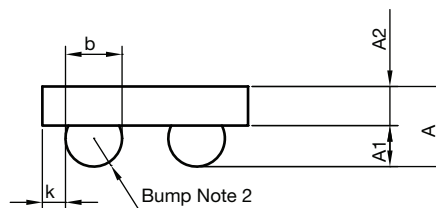
MICRO FOOT®: 4-Bump (0.8 mm x 0.8 mm, 0.4 mm Pitch)



Mark on Backside of die



Note 4



Notes

- (1) Laser mark on the backside surface of die
- (2) Bumps are 95.5 % Sn, 3.8 % Ag, 0.7 % Cu
- (3) "i" is the location of pin 1
- (4) "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
- (5) Non-solder mask defined copper landing pad.

DIM.	MILLIMETERS ^a			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.328	0.365	0.402	0.0129	0.0144	0.0158
A1	0.136	0.160	0.184	0.0053	0.0062	0.0072
A2	0.192	0.205	0.218	0.0076	0.0081	0.0086
b	0.200	0.220	0.240	0.0078	0.0086	0.0094
b1	0.175			0.0068		
e	0.400			0.0157		
S	0.160	0.180	0.200	0.0062	0.0070	0.0078
D	0.720	0.760	0.800	0.0283	0.0299	0.0314
K	0.040	0.070	0.100	0.0015	0.0027	0.0039

Note

- a. Use millimeters as the primary measurement.

ECN: T15-0053-Rev. A, 16-Feb-15
DWG: 6033



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