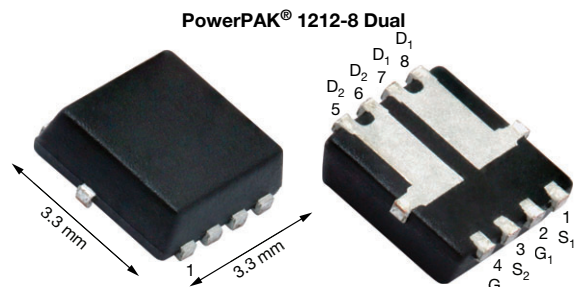


Dual P-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY

V_{DS} (V)	-30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.0264
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -6$ V	0.0312
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.0372
Q_g typ. (nC)	12.6
I_D (A) ^{f, g}	6
Configuration	Dual

FEATURES

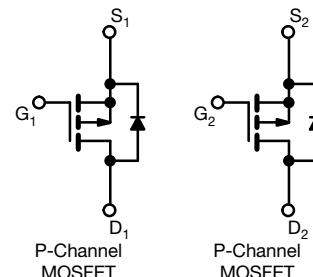
- TrenchFET® Gen III p-channel power MOSFET
- 62 % smaller package footprint than SO-8
- Thermally enhanced PowerPAK® package
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load switch
- Battery protection
- Adapter and charger switch
- Hand-held and mobile devices



ORDERING INFORMATION

Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	Si7223DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-30	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	-6 ^g
		$T_C = 70$ °C	-6 ^g
		$T_A = 25$ °C	-6 ^{a, b, g}
		$T_A = 70$ °C	-6 ^{a, b, g}
Pulsed drain current ($t = 100$ μ s)	I_{DM}	-40	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	6 ^g
		$T_A = 25$ °C	2.2 ^{a, b}
Single pulse avalanche current	I_{AS}	14	
Single pulse avalanche energy	E_{AS}	9.8	mJ
Maximum power dissipation	P_D	$T_C = 25$ °C	23
		$T_C = 70$ °C	14.8
		$T_A = 25$ °C	2.6 ^{a, b}
		$T_A = 70$ °C	1.7 ^{a, b}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{c, d}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, e}	R_{thJA}	38	48	°C/W
Maximum junction-to-case (drain)	R_{thJC}	4.3	5.4	

Notes

- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 94 °C/W
- Based on $T_C = 25$ °C
- Package limited

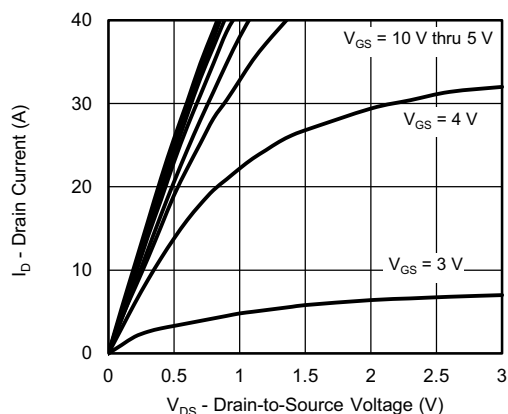
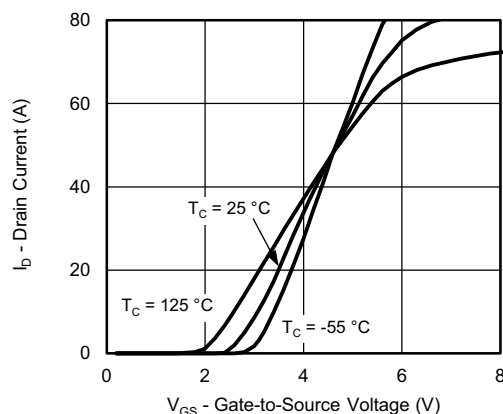
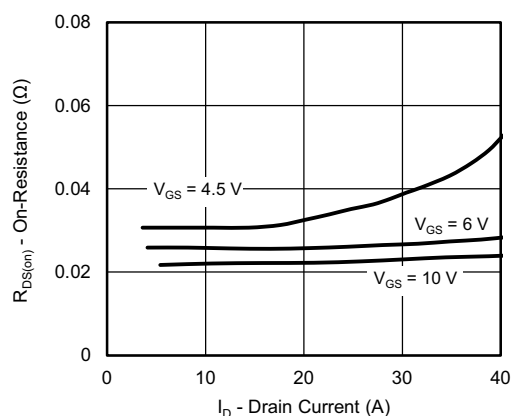
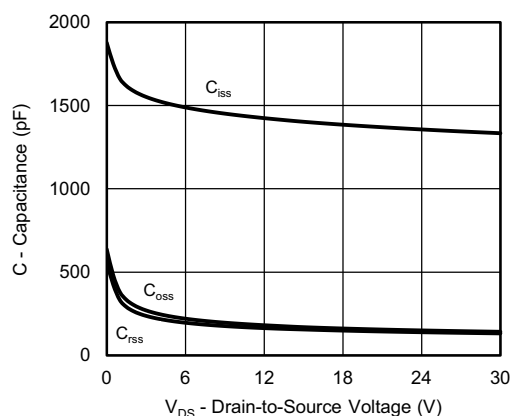
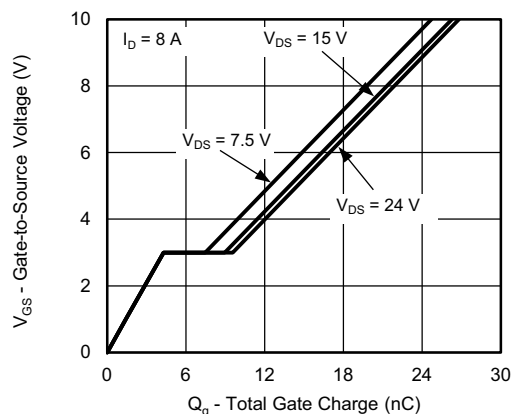
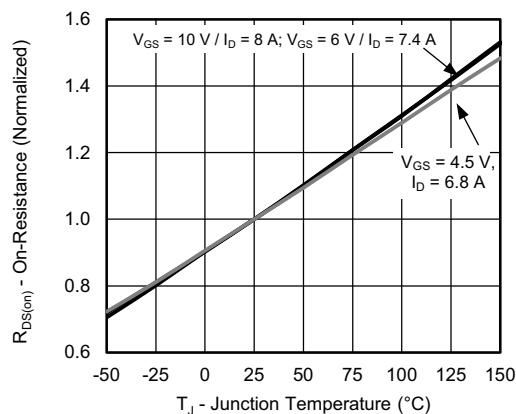


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-30	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -250 μA	-	-24.6	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	-4.5	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1	-	-2.5	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-state drain current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = 10 V	-10	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -8 A	-	0.0220	0.0264	Ω
		V _{GS} = -6 V, I _D = -7.4 A	-	0.0260	0.0312	
		V _{GS} = -4.5 V, I _D = -6.8 A	-	0.0310	0.0372	
Forward transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -6.8 A	-	20	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz	-	1425	-	pF
Output capacitance	C _{oss}		-	172	-	
Reverse transfer capacitance	C _{rss}		-	152	-	
Total gate charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -8 A	-	26.3	40	nC
		V _{DS} = -15 V, V _{GS} = -6 V, I _D = -8 A	-	12.6	19	
Gate-source charge	Q _{gs}		-	4.3	-	
Gate-drain charge	Q _{gd}		-	4.7	-	
Gate resistance	R _g	f = 1 MHz	1.72	8.6	17.2	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = -15 V, R _L = 3.3 Ω I _D ≅ -6.4 A, V _{GEN} = -6 V, R _g = 1 Ω	-	18	36	ns
Rise time	t _r		-	40	60	
Turn-off delay time	t _{d(off)}		-	37	56	
Fall time	t _f		-	36	54	
Turn-on delay time	t _{d(on)}	V _{DD} = -15 V, R _L = 3.3 Ω I _D ≅ -6.4 A, V _{GEN} = -10 V, R _g = 1 Ω	-	12	20	
Rise time	t _r		-	7	14	
Turn-off delay time	t _{d(off)}		-	42	64	
Fall time	t _f		-	8	41	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	6 °	A
Pulse diode forward current	I _{SM}		-	-	40	
Body diode voltage	V _{SD}	I _S = -6.4 A, V _{GS} = 0 V	-	0.8	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = -6.4 A, di/dt = 100 A/μs, T _J = 25 °C	-	20	40	ns
Body diode reverse recovery charge	Q _{rr}		-	12	20	nC
Reverse recovery fall time	t _a		-	11	-	ns
Reverse recovery rise time	t _b		-	9	-	

Notes

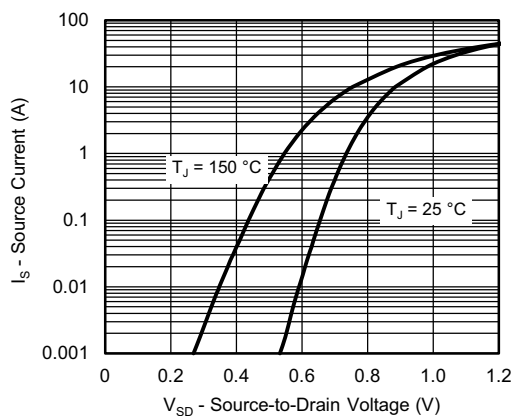
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Package limited

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

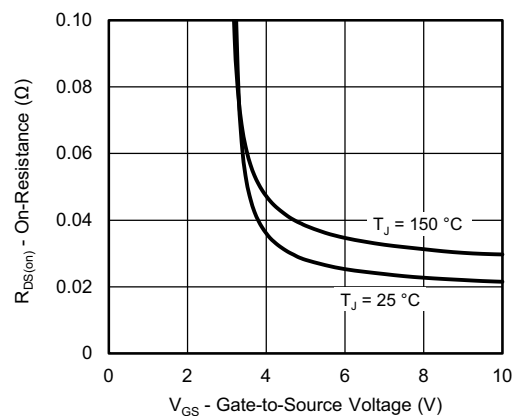
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



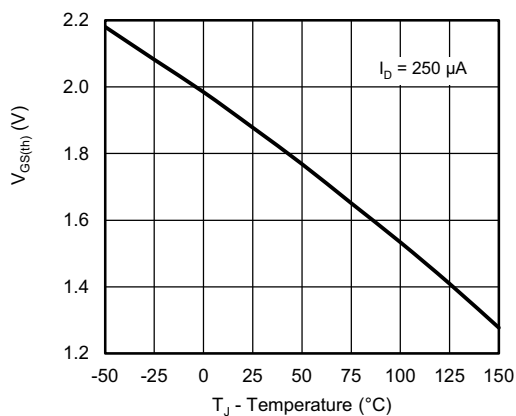
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



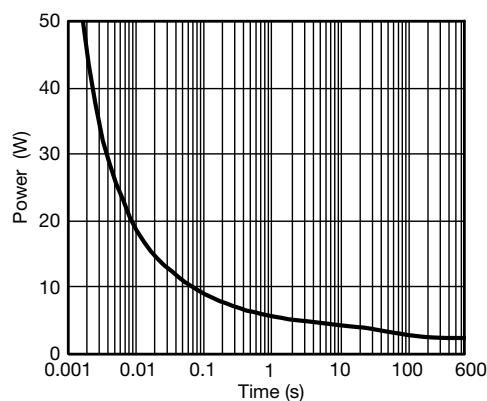
Source-Drain Diode Forward Voltage



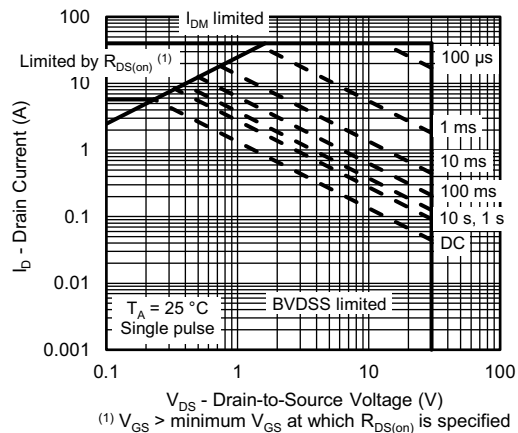
On-Resistance vs. Gate-to-Source Voltage



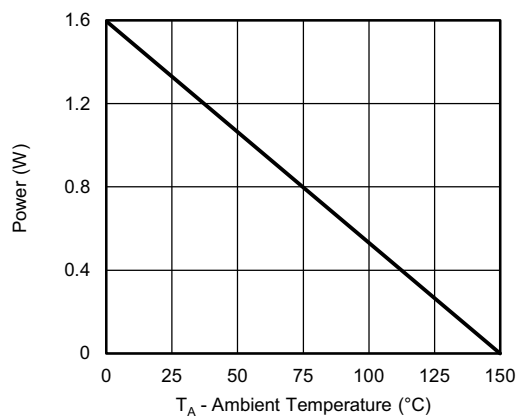
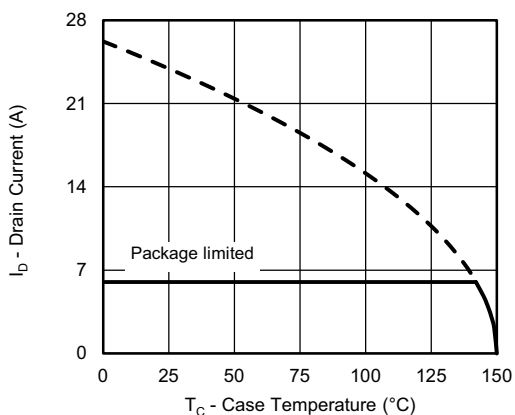
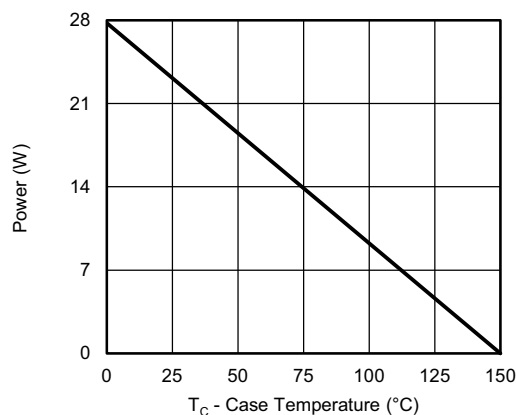
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



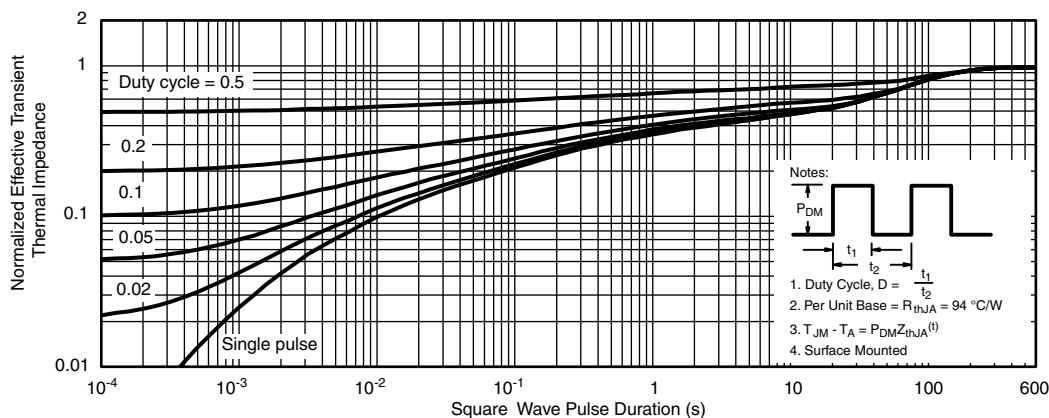
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Power Junction to Ambient

Current Derating ^a

Power Derating
Note

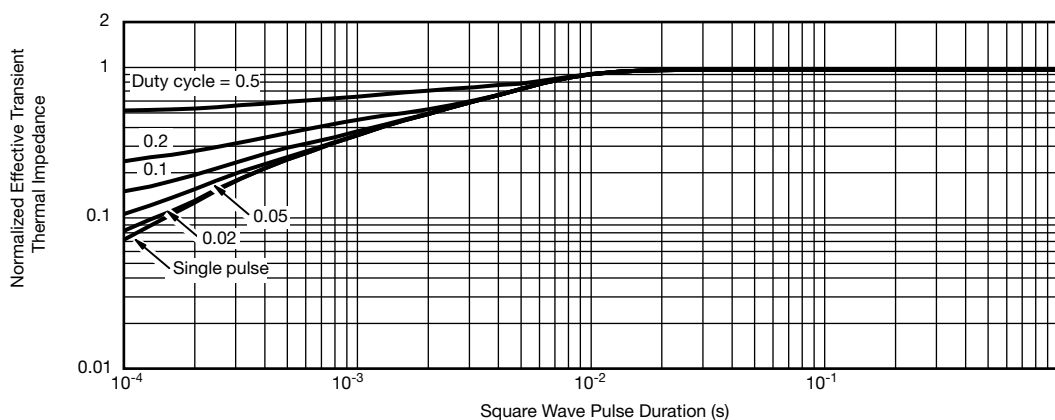
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75609.



PowerPAK® 1212-8, (Single / Dual)



Backside view of single pad



Backside view of dual pad

Notes

1. Inch will govern

[2] Dimensions exclusive of mold gate burrs

3. Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S16-2667-Rev. M, 09-Jan-17						
DWG: 5882						

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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