

P-Channel 150-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 150	0.75 at $V_{GS} = - 10$ V	- 1.4	8 nC
	0.79 at $V_{GS} = - 6$ V	- 1.3	

FEATURES

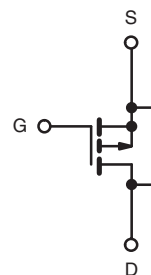
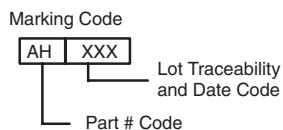
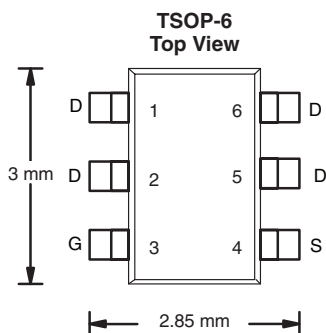
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Active Clamp Circuits in DC/DC Power Supplies



Ordering Information: Si3437DV-T1-E3 (Lead (Pb)-free)
Si3437DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 150	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	- 5	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
Avalanche Current	I_{AS}	5	mJ
Single-Pulse Avalanche Energy	E_{AS}	1.25	
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	W
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	51	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Foot	R_{thJF}	32	39	

Notes:

- $T_C = 25^\circ\text{C}$.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- Maximum under Steady State conditions is 110°C/W .

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 150			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 160		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			5.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 2		- 4	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 150 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 150 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ - 10 V, V _{GS} = - 10 V	- 3			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 1.4 A		0.61	0.75	Ω
		V _{GS} = - 6 V, I _D = - 1 A		0.64	0.79	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 1.4 A		4.5		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 50 V, V _{GS} = 0 V, f = 1 MHz		510		pF
Output Capacitance	C _{oss}			30		
Reverse Transfer Capacitance	C _{rss}			21		
Total Gate Charge	Q _g	V _{DS} = - 75 V, V _{GS} = - 10 V, I _D = - 1 A		12.2	19	nC
Gate-Source Charge	Q _{gs}	V _{DS} = - 75 V, V _{GS} = - 6 V, I _D = - 1 A		8	12	
Gate-Drain Charge	Q _{gd}			2.1		
Gate Resistance	R _g			3.9		
Gate Resistance	R _g	f = 1 MHz		8.5	13	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 75 V, R _L = 75 Ω I _D ≅ - 1 A, V _{GEN} = - 10 V, R _g = 1 Ω		9	15	ns
Rise Time	t _r			11	18	
Turn-Off DelayTime	t _{d(off)}			28	42	
Fall Time	t _f			12	18	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 75 V, R _L = 75 Ω I _D ≅ - 1 A, V _{GEN} = - 6 V, R _g = 1 Ω		14	21	
Rise Time	t _r			29	44	
Turn-Off DelayTime	t _{d(off)}			23	35	
Fall Time	t _f			14	21	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			- 1.4	A
Pulse Diode Forward Current	I _{SM}				- 5	
Body Diode Voltage	V _{SD}	I _S = - 1 A, V _{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 1.2 A, dI/dt = 100 A/μs, T _J = 25 °C		60	90	ns
Body Diode Reverse Recovery Charge	Q _{rr}			120	180	nC
Reverse Recovery Fall Time	t _a			35		ns
Reverse Recovery Rise Time	t _b			25		

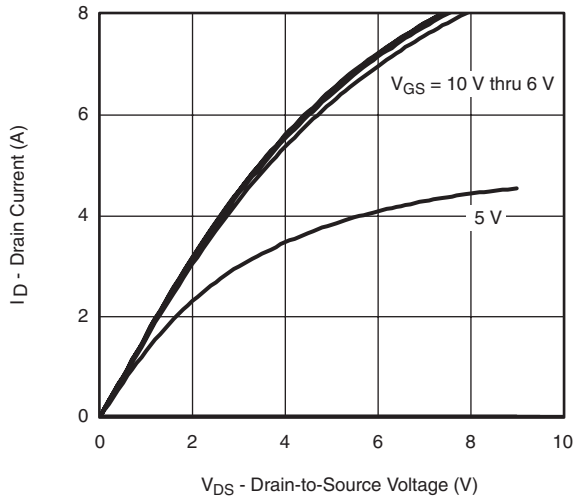
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

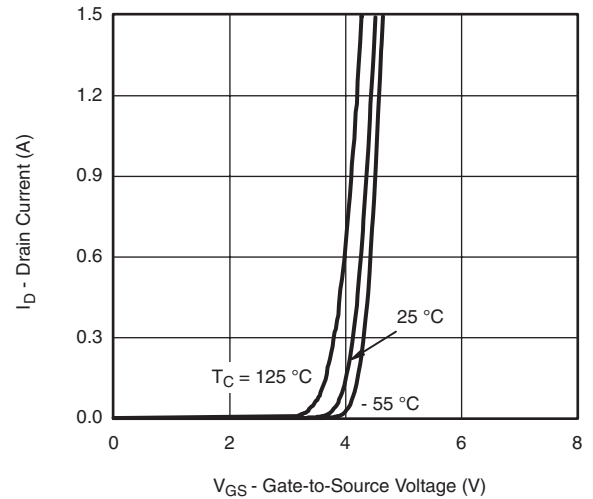
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

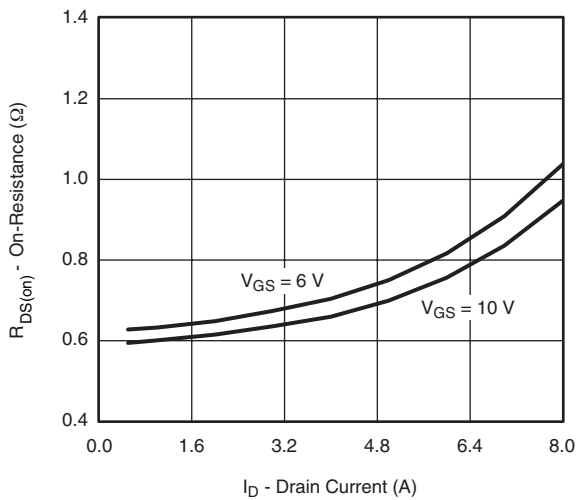
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



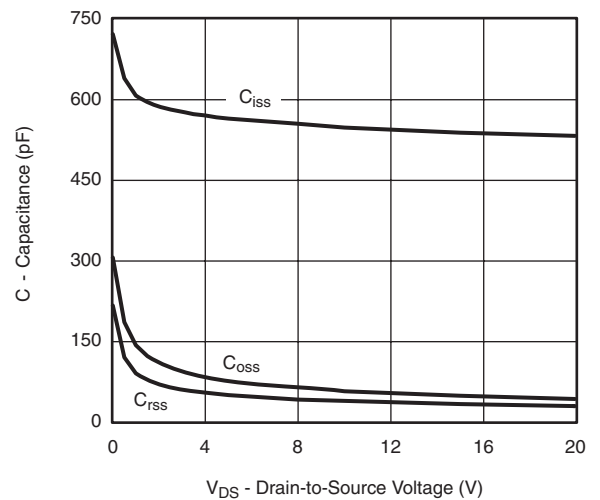
Output Characteristics



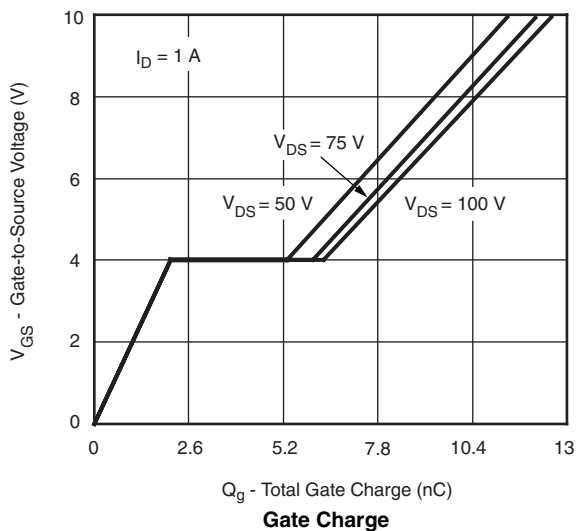
Transfer Characteristics



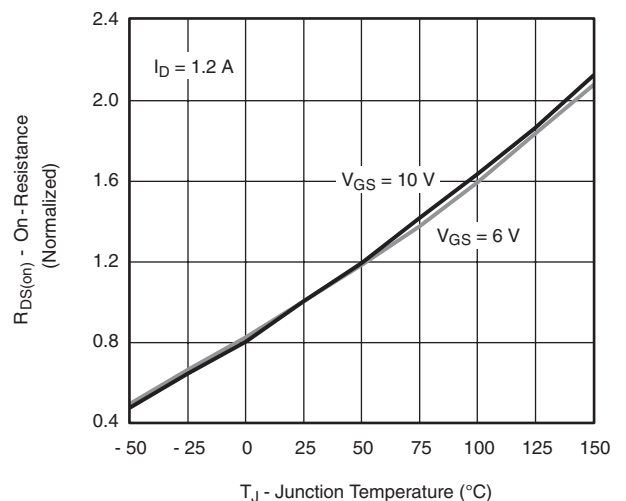
On-Resistance vs. Drain Current and Gate Voltage



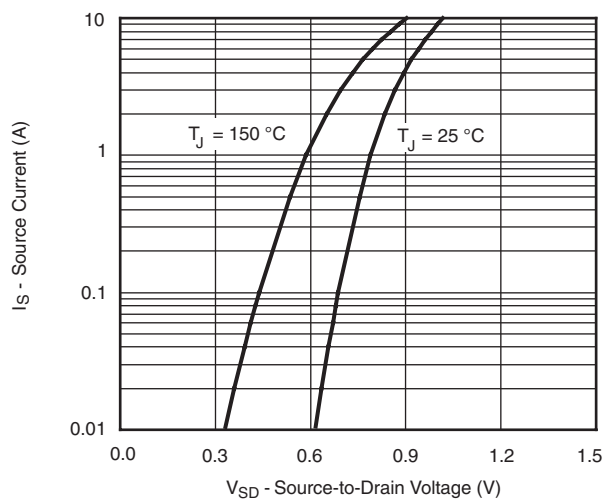
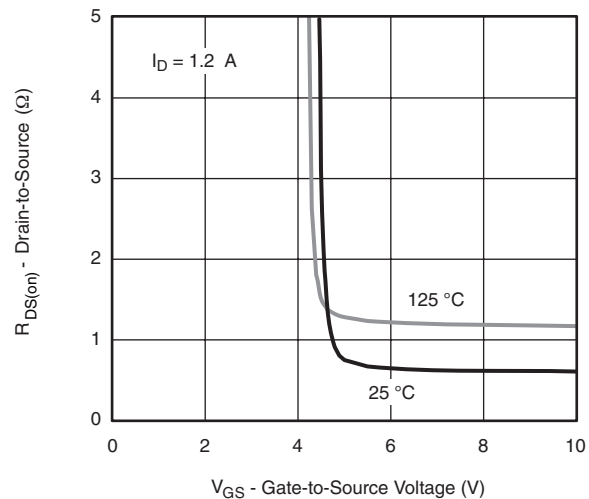
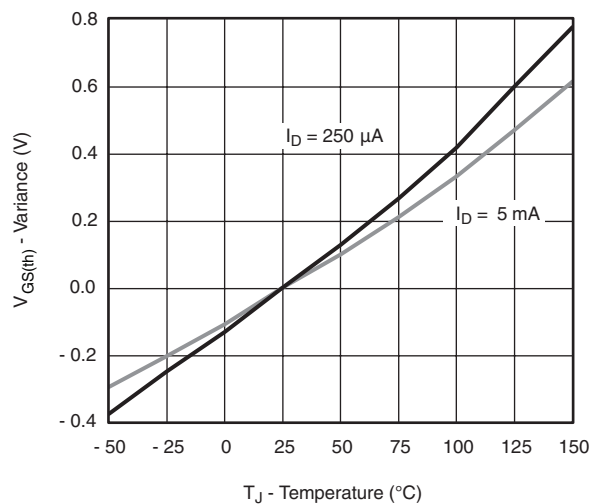
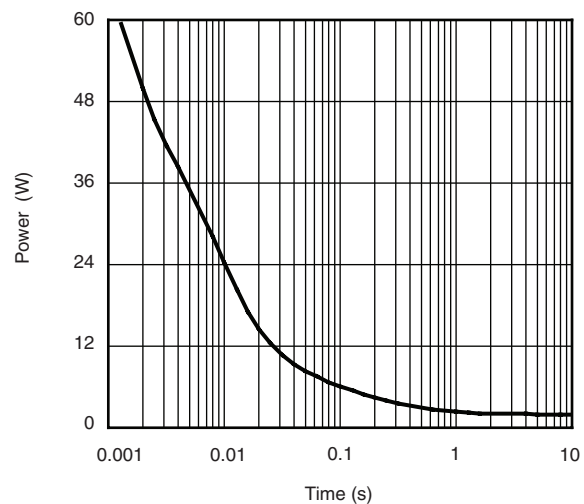
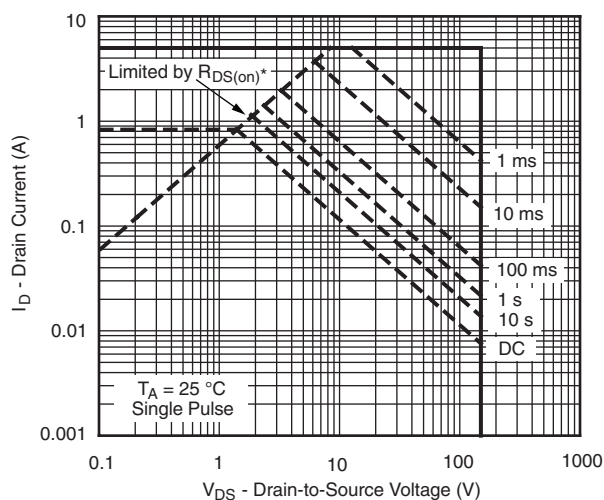
Capacitance



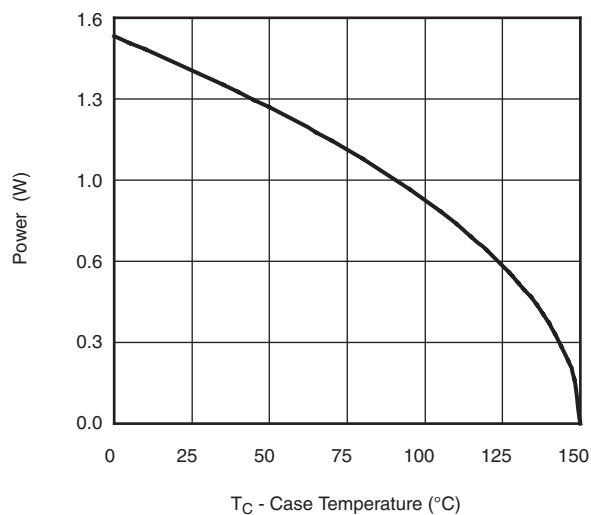
Gate Charge



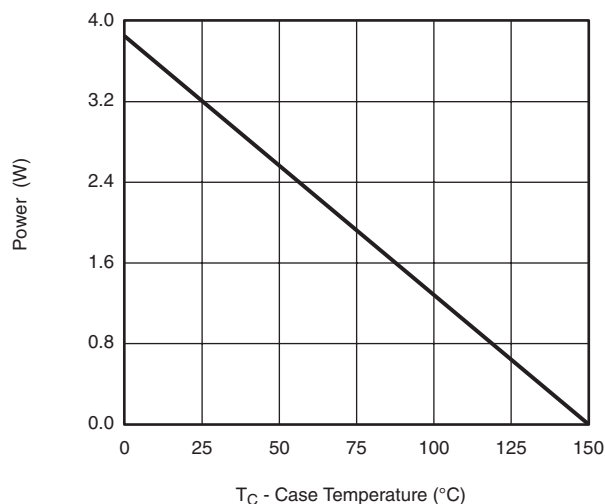
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Temperature****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

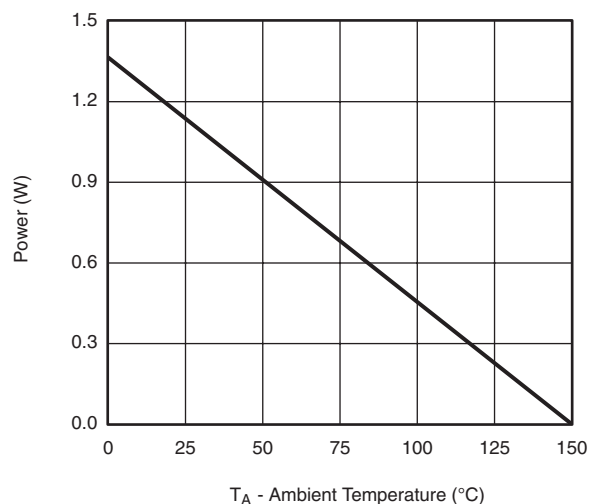
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*

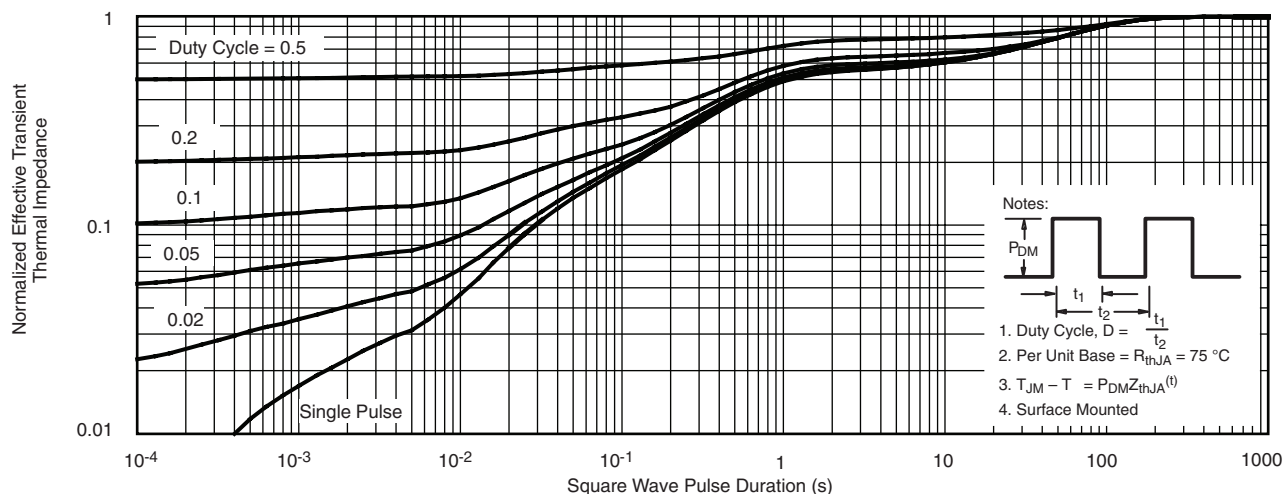
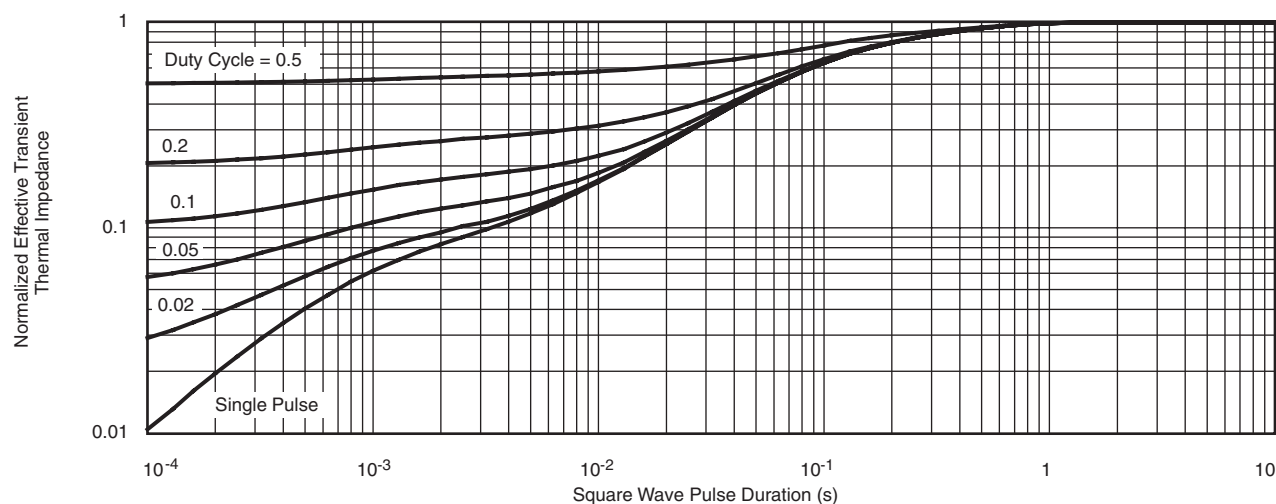


Power, Junction-to-Foot



Power Derating, Junction-to-Ambient

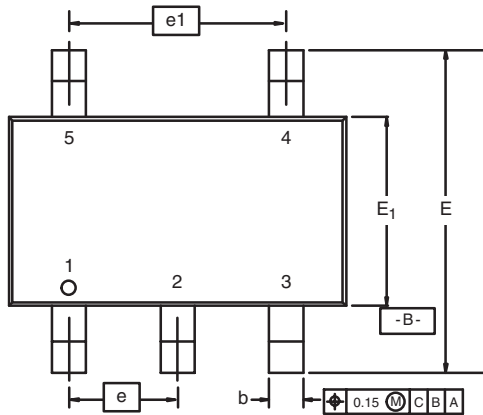
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

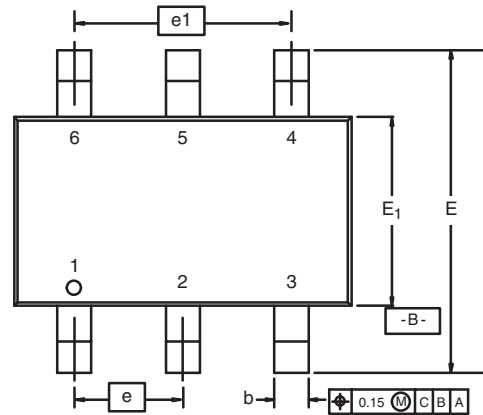
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73899.

TSOP: 5/6-LEAD

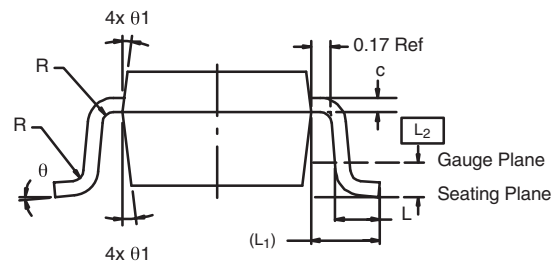
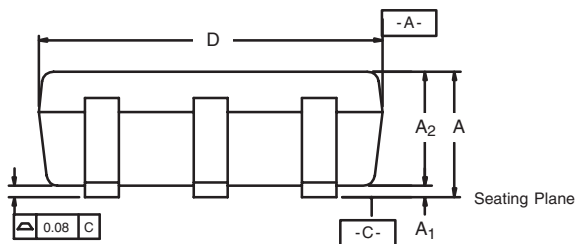
JEDEC Part Number: MO-193C



5-LEAD TSOP

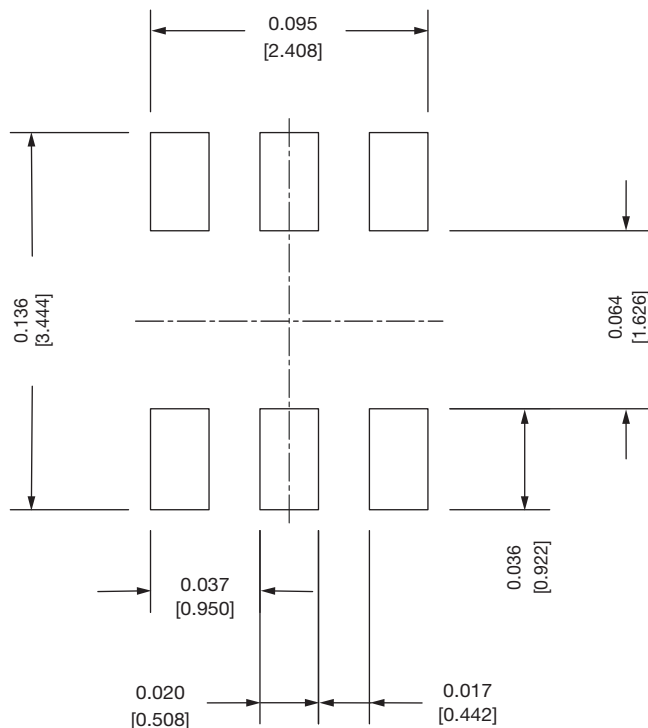
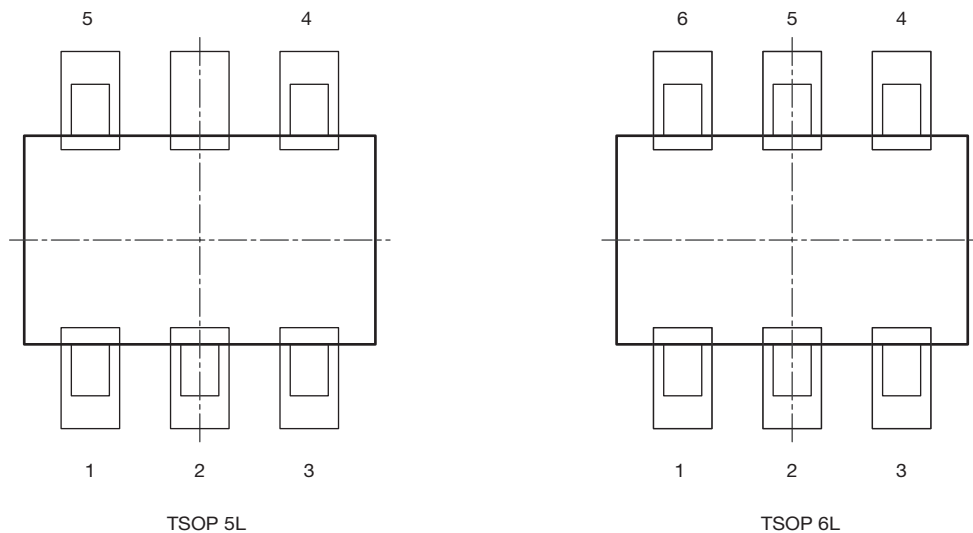


6-LEAD TSOP



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

Recommended Land Pattern For TSOP-5L / TSOP-6L


Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
DWG: 3010



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