

N-Channel, Logic Level Enhancement Mode Field Effect Transistor

NDB5060L

General Description

These logic level N-Channel enhancement mode power field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC-DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 26 A, 60 V
 - ♦ $R_{DS(ON)} = 0.05 \text{ m}\Omega @ V_{GS} = 5 \text{ V}$
 - ♦ $R_{DS(ON)} = 0.035 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
- Critical DC Electrical Parameters Specified at Elevated Temperature
- Rugged Internal Source-Drain Diode Can Eliminate the Need for an External Zener Diode Transient Suppressor
- 175°C Maximum Junction Temperature Rating
- High Density Cell Design for Extremely Low $R_{DS(ON)}$
- D²PAK Package for Both Through Hole and Surface Mount Applications

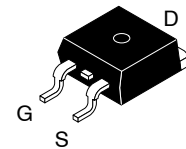
ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Rating	Value	Unit
V_{DSS}	Drain-Source Voltage	60	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1 \text{ M}\Omega$)	60	V
V_{GSS}	Drain-Source Voltage – Continuous – Nonrepetitive ($t_p < 50 \mu\text{s}$)	± 16 ± 25	V
I_D	Drain Current – Continuous – Pulsed	26 78	A
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$ – Derate above 25°C	68 0.45	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	–65 to 175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

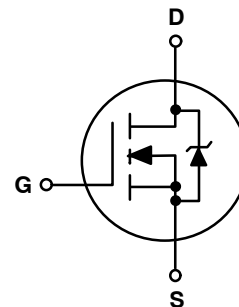
THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$

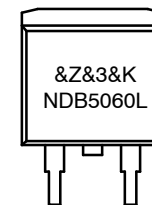


D2PAK-3
(TO-263, 3-LEAD)
CASE 418AJ

N-CHANNEL MOSFET



MARKING DIAGRAM



&Z = Assembly Plan Code
 &3 = 3-Digit Date Code (Year & Week)
 &K = 2-Digits Lot Run Traceability Code
 NDB5060L = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NDB5060L	D2PAK-3 (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NDB5060L

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
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DRAIN-SOURCE AVALANCHE RATINGS (Note 1)

W _{DSS}	Single Pulse Drain-Source Avalanche Energy	V _{DD} = 30 V, I _D = 26 A	–	–	100	mJ
I _{AR}	Maximum Drain-Source Avalanche Current		–	–	26	A

OFF CHARACTERISTICS

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	60	–	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 60 V, V _{GS} = 0 V	–	–	250	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 125°C	–	–	1	mA
I _{GSSF}	Gate-Body Leakage, Forward	V _{GS} = 16 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	V _{GS} = –16 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS (Note 1)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	1.4	2	V
		V _{DS} = V _{GS} , I _D = 250 μA, T _J = 125°C	0.65	1	1.5	
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 5 V, I _D = 13 A	–	0.042	0.05	Ω
		V _{GS} = 5 V, I _D = 13 A, T _J = 125°C	–	0.07	0.08	
		V _{GS} = 10 V, V _{DS} = 13 A	–	0.031	0.035	
I _{D(on)}	On-State Drain Current	V _{GS} = 5 V, V _{DS} = 10 V	26	–	–	A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 13 A	–	16	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 30 V, V _{GS} = 0 V, f = 1.0 MHz	–	840	–	pF
C _{oss}	Output Capacitance		–	230	–	pF
C _{rss}	Reverse Transfer Capacitance		–	75	–	pF

SWITCHING CHARACTERISTICS (Note 1)

t _{D(on)}	Turn – On Delay Time	V _{DD} = 30 V, I _D = 26 A, V _{GS} = 5 V, R _{GEN} = 30 Ω, R _{GS} = 30 Ω	–	13	20	nS
t _r	Turn – On Rise Time		–	200	400	nS
t _{D(off)}	Turn – Off Delay Time		–	45	80	nS
t _f	Turn – Off Fall Time		–	102	200	nS
Q _g	Total Gate Charge	V _{DS} = 24 V, I _D = 26 A, V _{GS} = 5 V	–	17	24	nC
Q _{gs}	Gate-Source Charge		–	4	–	nC
Q _{gd}	Gate-Drain Charge		–	10	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain-Source Diode Forward Current		–	–	26	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		–	–	78	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 13 A (Note 1)	–	0.9	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _F = 26 A,	–	54	120	ns
I _{rr}	Reverse Recovery Current	dI _F /dt = 100 A/μs	–	2.1	8	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

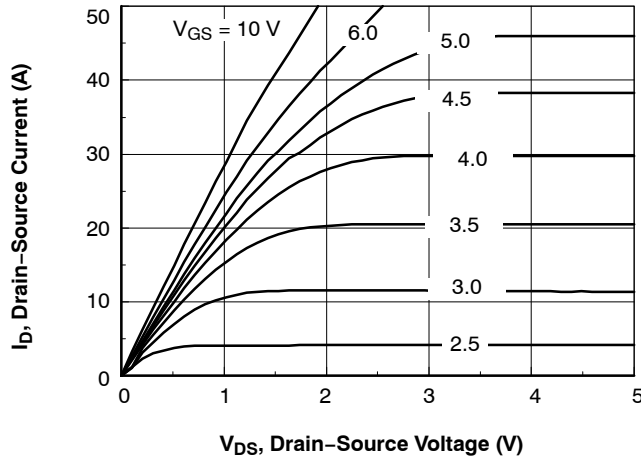


Figure 1. On-Region Characteristics

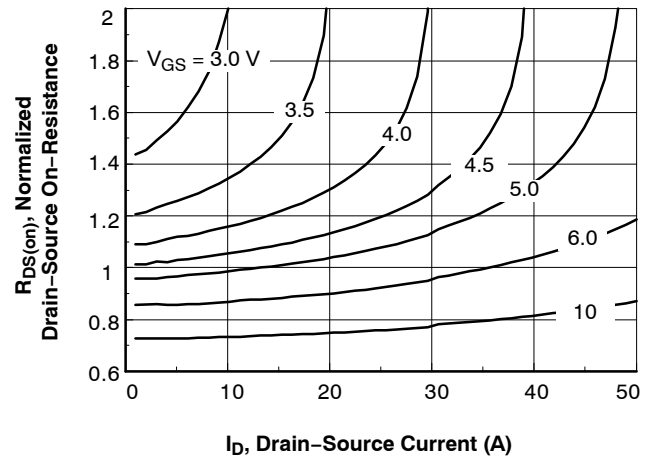


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

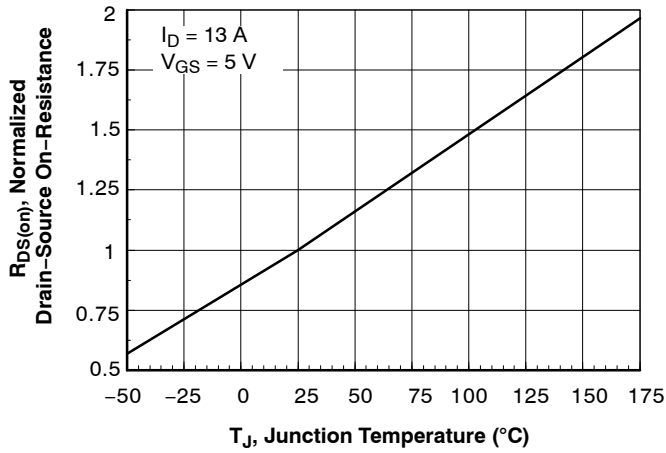


Figure 3. On-Resistance Variation with Temperature

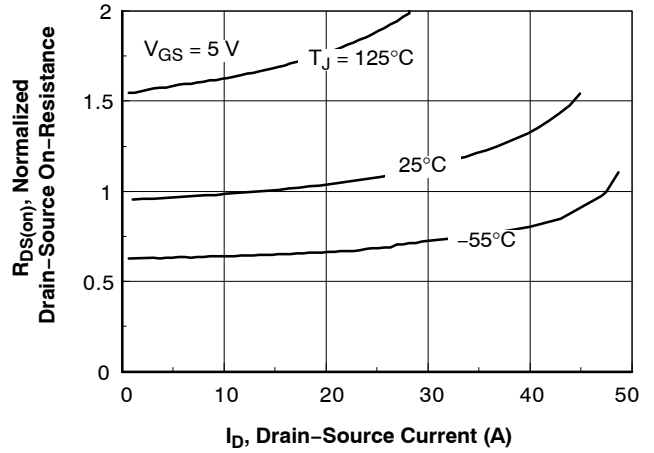


Figure 4. On-Resistance Variation with Drain Current and Temperature

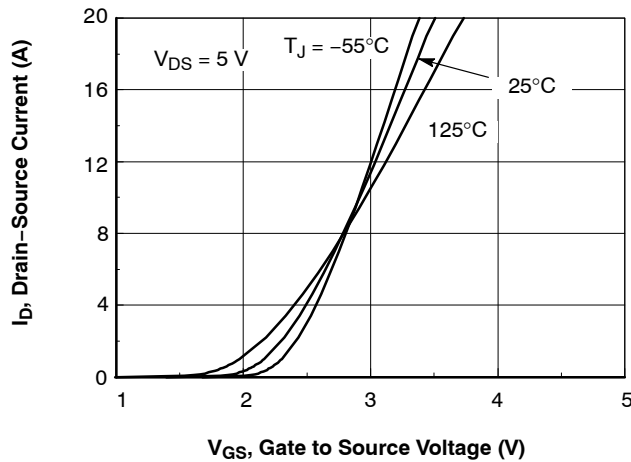


Figure 5. Transfer Characteristics

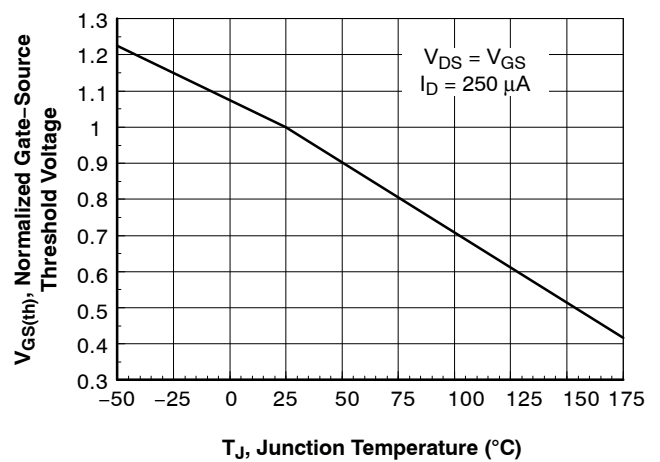


Figure 6. Gate Threshold Variation with Temperature

TYPICAL CHARACTERISTICS (Continued)

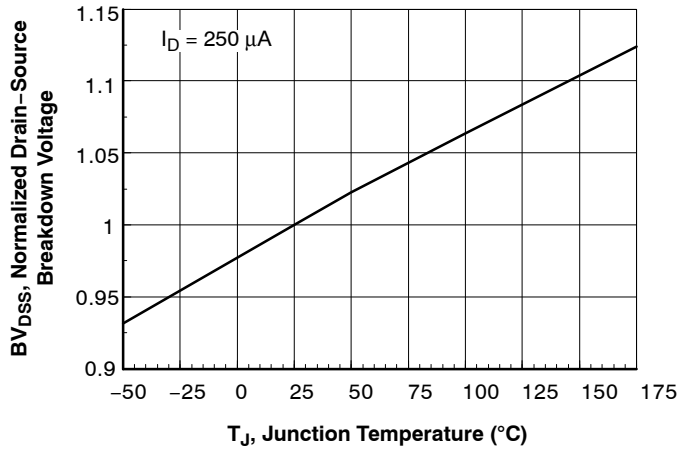


Figure 7. Breakdown Voltage Variation with Temperature

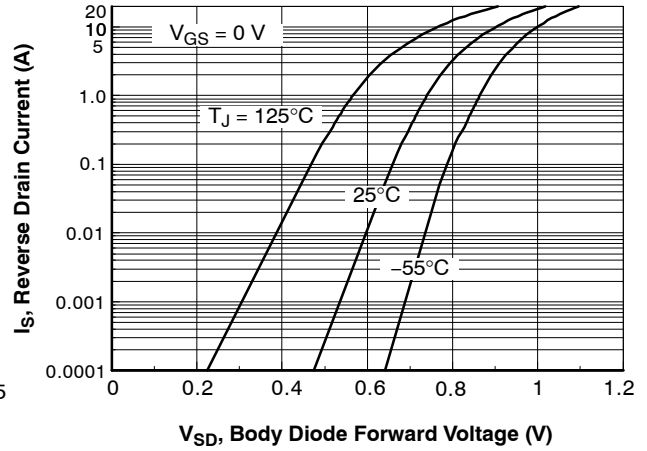


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

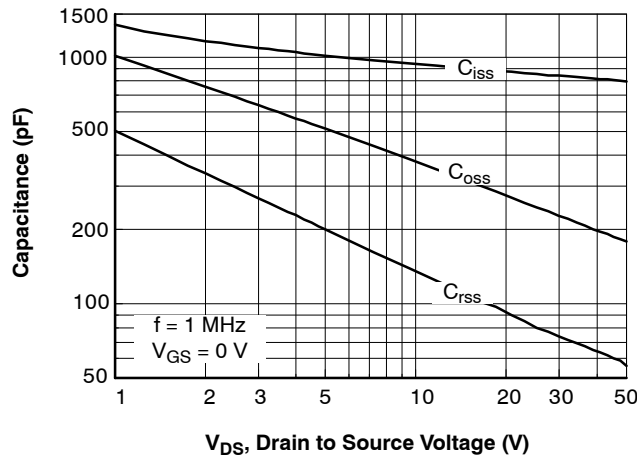


Figure 9. Capacitance Characteristics

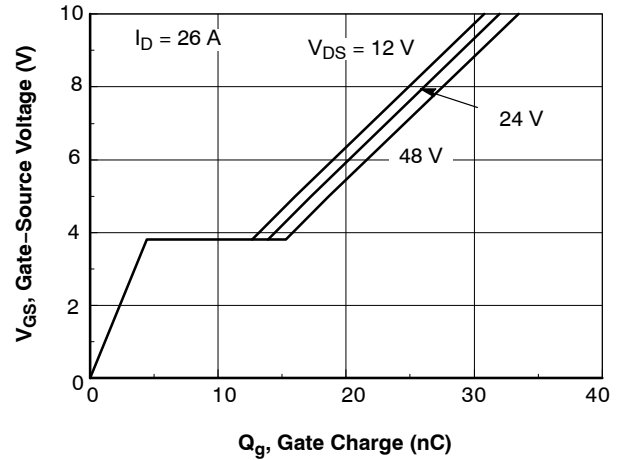


Figure 10. Gate Charge Characteristics

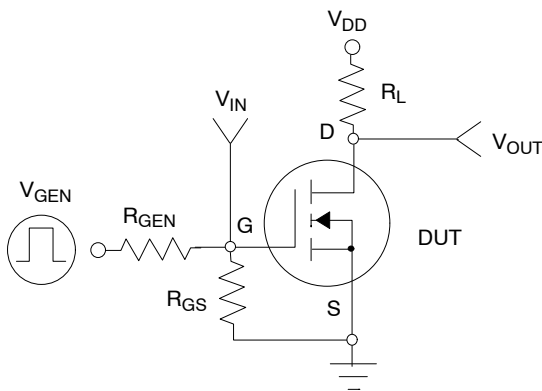


Figure 11. Switching Test Circuit

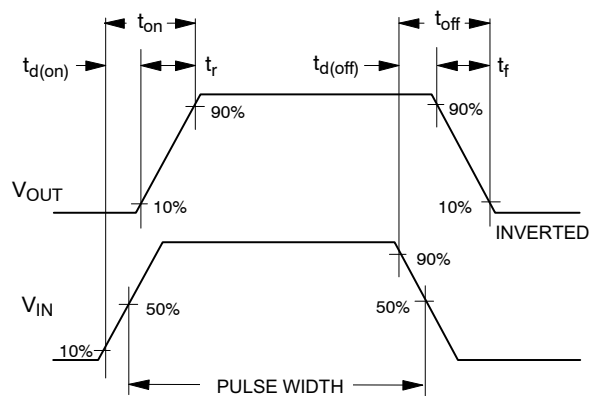


Figure 12. Switching Waveforms

TYPICAL CHARACTERISTICS (Continued)

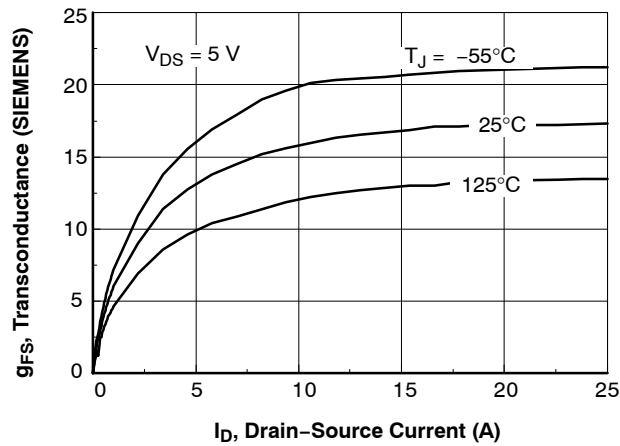


Figure 13. Transconductance Variation with Drain Current and Temperature

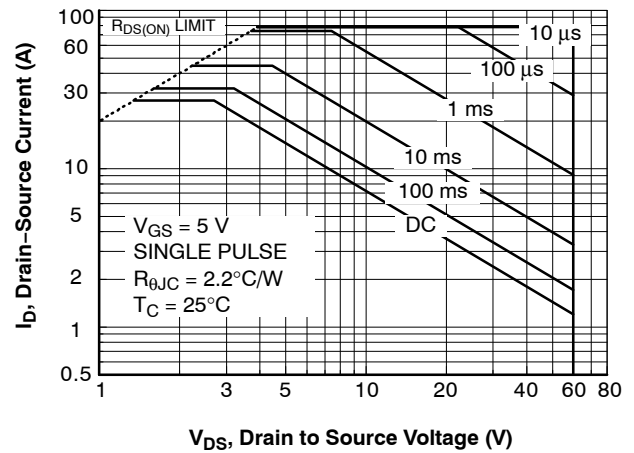


Figure 14. Maximum Safe Operating Area

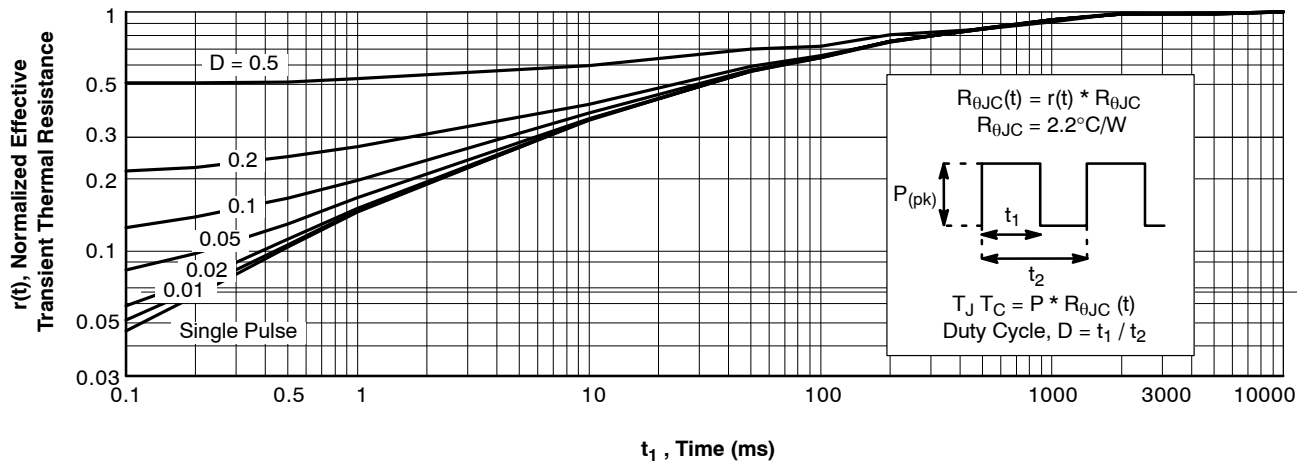
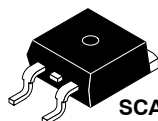


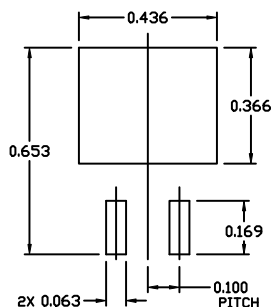
Figure 15. Transient Thermal Response Curve



SCALE 1:1

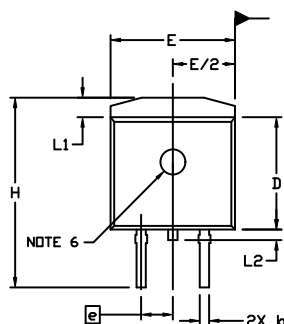
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DATE 11 MAR 2021

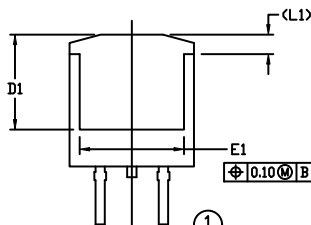


RECOMMENDED
MOUNTING FOOTPRINT

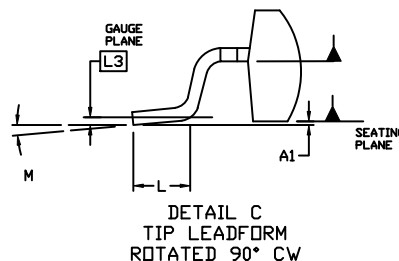
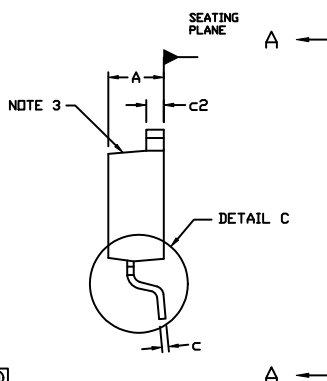
For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM1.



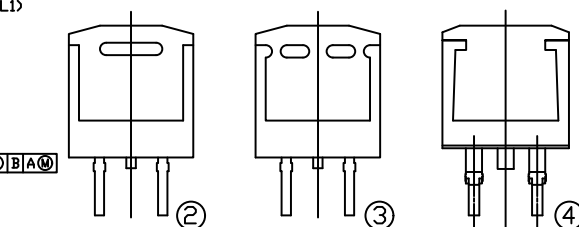
0.100 BSC 0.100 BSC 0.100 BSC



VIEW A-A

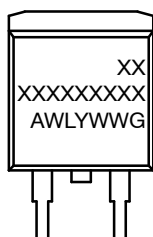


DETAIL C
TIP LEADFORM
ROTATED 90° CW

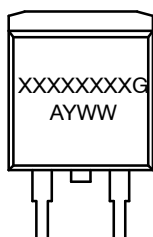


VIEW A-A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



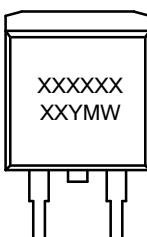
IC



Standard



Rectifier



SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb-Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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