NCP4330

Post Regulation Driver

The NCP4330 houses a dual MOSFET driver intended to be used as a companion chip in AC−DC or DC−DC multi−output post regulated power supplies. Being directly fed by the secondary AC signal, the device keeps power dissipation to the lowest while reducing the surrounding part count. Furthermore, the implementation of a N−channel MOSFET gives NCP4330−based applications a significant advantage in terms of efficiency.

Features

- Undervoltage Lockout
- Thermal Shutdown for Overtemperature Protection
- PWM Operation Synchronized to the Converter Frequency
- High Gate Drive Capability
- Bootstrap for N−MOSFET High−Side Drive
- Over−Lap Management for Soft Switching
- High Efficiency Post−Regulation
- Ideal for Frequencies up to 400 kHz
- This is a Pb−Free Device

Typical Applications

- ATX 3V3 Post−Regulation
- Offline SMPS with MAGAMP Post−Regulation
- Multi−Outputs DC−DC Converters

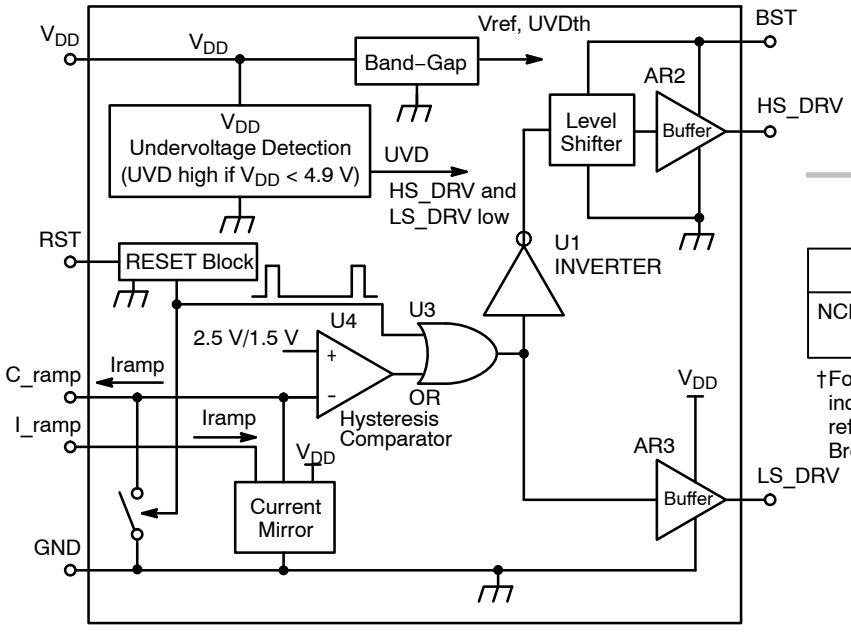

Figure 1. Block Diagram

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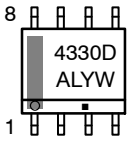
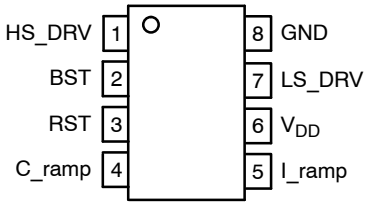
MARKING DIAGRAM

SO−8
D SUFFIX
CASE 751



4330D	= Device Number
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP4330DR2G	SO−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

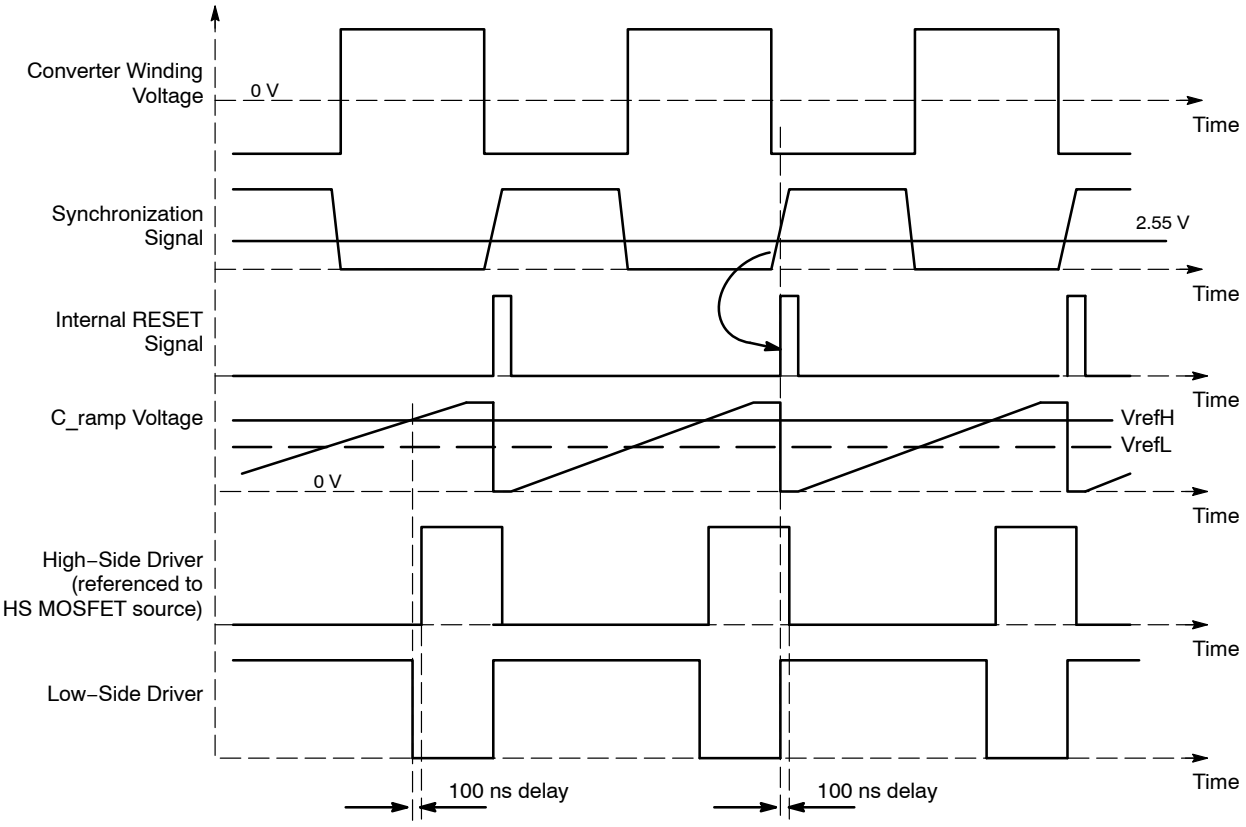


Figure 2. Timing Diagram(s)

DETAILED PIN DESCRIPTION(S)

Pin Number	Name	Function
1	HS_DRV	"HS_DRV" is the gate driver of the high−side MOSFET.
2	BST	"BST" is the bootstrap pin. A 0.1 μF to 1.0 μF ceramic capacitor should be connected between this pin and the node that is common to the coil and the two MOSFET. The "BST" voltage feeds the high−side driver ("HS_DRV").
3	RST	The "RST" pin resets the C_ramp voltage in order to synchronize the post−regulator free−wheeling sequence to the forward converter demagnetization phase.
4	C_ramp	The capacitor connected to the C_ramp pin enables to adjust the delay in turning on the high−side MOSFET (in conjunction with "I_ramp" current).
5	I_ramp	The "I_ramp" pin receives a current supplied by a regulation means. This current adjusts the delay after which the high−side MOSFET is turned on. By this way, it modules the high−side MOSFET on time in order to regulate the output voltage.
6	V_{DD}	"V_{DD}" is the power supply input. A 0.1 μF to 1.0 μF ceramic capacitor should be connected from this pin to ground for decoupling.
7	LS_DRV	"LS_DRV" is the driver output of the low−side MOSFET gate.
8	GND	Ground.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
BST	Bootstrap Input	−0.3, +40	V
RST	Reset Input	−0.3, +5.0	V
C_ramp	Timing Capacitor Node (Note 1)	−0.3, V_{rampHL}	V
I_ramp	Regulation Current Input (Note 1)	−0.3, Vcl	V
V_{DD}	Supply Voltage	−0.3, +20	V
$R_{\theta JA}$	Thermal Resistance	180	°C/W
T_J	Operating Junction Temperature Range (Note 2)	−40, +125	°C
T_{Jmax}	Maximum Junction Temperature	150	°C
T_{Smax}	Storage Temperature Range	−65 to +150	°C
T_{Lmax}	Lead Temperature (Soldering, 10 s)	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{rampHL} and Vcl are the internal clamp levels of pins 4 and 5 respectively.
2. The maximum junction temperature should not be exceeded.

ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{BST} = 25 V, T_J from −25°C to +125°C, unless otherwise specified.)

Symbol	Characteristic	Min	Typ	Max	Unit
High−Side Output Stage					
V_{HS_H}	High−Side Output Voltage in High State @ Isource = −100 mA	22.5	23.5	–	V
V_{HS_L}	High−Side Output Voltage in Low State @ Isink = 100 mA	–	0.9	1.5	V
I_{source_HS}	Current Capability of the High−Side Drive Output in High State	–	0.5	–	A
I_{sink_HS}	Current Capability of the High−Side Drive Output in Low State	–	0.75	–	A
t_{r-HS}	High−Side Output Voltage Rise Time from 0.5 V to 12 V (C_L = 1.0 nF)	–	25	–	ns
t_{f-HS}	High−Side Output Voltage Fall Time from 20 V to 0.5 V (C_L = 1.0 nF)	–	25	–	ns
T_{LS-HS}	Delay from Low−Side Gate Drive Low (High) to High−Side Drive High (Low)	–	100	–	ns
Low−Side Output Stage					
V_{LS_H}	Low−Side Output Voltage in High State @ Isource = −500 mA	7.4	8.2	–	V
V_{LS_L}	Low−Side Output Voltage in Low State @ Isink = 750 mA	–	1.3	1.7	V
I_{source_LS}	Current Capability of the Low−Side Drive Output in High State	–	0.5	–	A
I_{sink_LS}	Current Capability of the Low−Side Drive Output in Low State	–	0.75	–	A
t_{r-LS}	Low−Side Output Voltage Rise Time from 0.5 V to 7.0 V (C_L = 2.0 nF)	–	25	–	ns
t_{f-LS}	Low−Side Output Voltage Fall Time from 9.5 V to 0.5 V (C_L = 2.0 nF)	–	25	–	ns
Ramp Control					
I_{charge}	C_ramp Current @ Ipin5 = 100 μA @ Ipin5 = 1.5 mA	 90 1400	 102 1590	 110 1800	μA
Vcl	Pin5 Clamp Voltage @ Ipin5 = 1.5 mA	0.7	1.4	2.1	V
$Vref_L$	Ramp Control Reference Voltage, Vpin4 Falling	1.3	1. 5	1.7	V
$Vref_H$	Ramp Control Reference Voltage, Vpin4 Rising	2.25	2.5	2.75	V
V_{rampHL}	Ramp Voltage Maximum Value @ Ipin5 = 1.5 mA	3.2	3.6	4.2	V
V_{rampLL}	Ramp Voltage Low Voltage @ Ipin5 = 1.5 mA	–	–	100	mV

ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 10 V, V_{BST} = 25 V, T_J from −25°C to +125°C, unless otherwise specified.)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD} Management					
UVD_H	Undervoltage Lockout Threshold (V_{DD} Rising)	5.2	5.8	6.4	V
UVD_L	Undervoltage Lockout Threshold (V_{DD} Falling)	4.9	5.2	5.5	V
H_{UVD}	Undervoltage Lockout Hysteresis	400	600	–	mV
	Consumption:				mA
I_{DD1}	@ Vpin4 = 3.0 V and Ipin5 = 500 μA	–	13	20	
I_{DD2}	@ Vpin4 = 0 V and Ipin5 = 500 μA	–	7.0	12	
I_{DD3}	@ Vpin4 Oscillating 0 to 3.0 V at 200 kHz, Ipin5 = 500 μA	–	10	15	
Reset Block					
V_{rst_th}	Reset Block Threshold	2.2	2.5	2.8	V
H_{rst}	Reset Comparator Hysteresis	0.8	1.0	–	V
T_{reset}	Reset Pulse Duration	–	250	500	ns
I_{reset}	C_ramp Pin Average Current, a 200 kHz, 50% duty cycle Pulse Generator being applied to reset pin and 1.0 V to pin 4 (C_ramp) and @ Iramp = 0	0.3	0.7	–	mA
V_{cl-neg}	Negative Clamp Level @ Ipin3 = −2.0 mA	−0.5	−0.3	0	V
BST Leakage					
$BST_{leakage}$	BST Leakage Current (BST = 10 V, V_{DD} = 1.5 V, other pins grounded, T_J = 25°C)	–	8.0	15	μA
Temperature Protection					
T_{limit}	Thermal Shutdown Threshold	–	150	–	°C
H_{temp}	Thermal Shutdown Hysteresis	–	50	–	°C

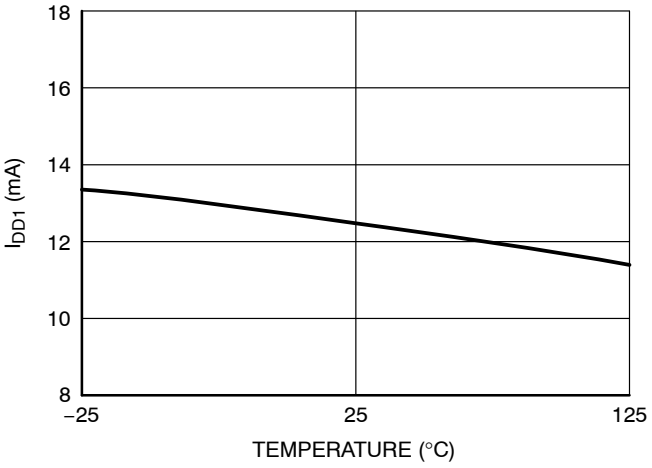


Figure 3. I_{DD1} Consumption vs. Temperature

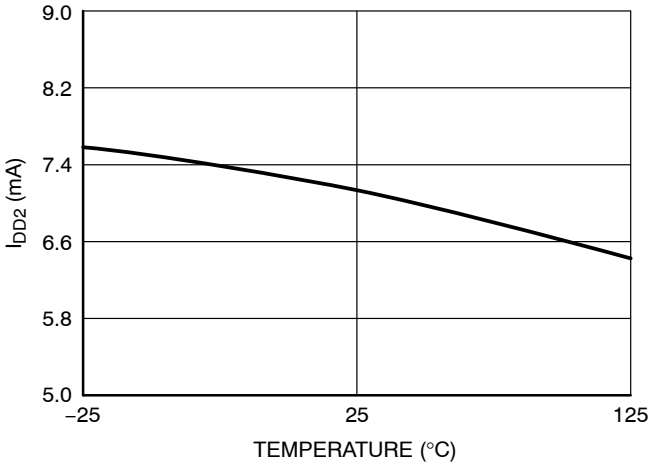


Figure 4. I_{DD2} Consumption vs. Temperature

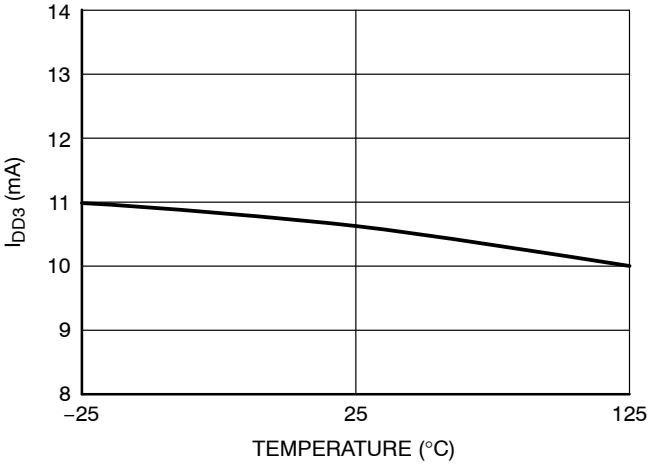


Figure 5. I_{DD3} Consumption vs. Temperature

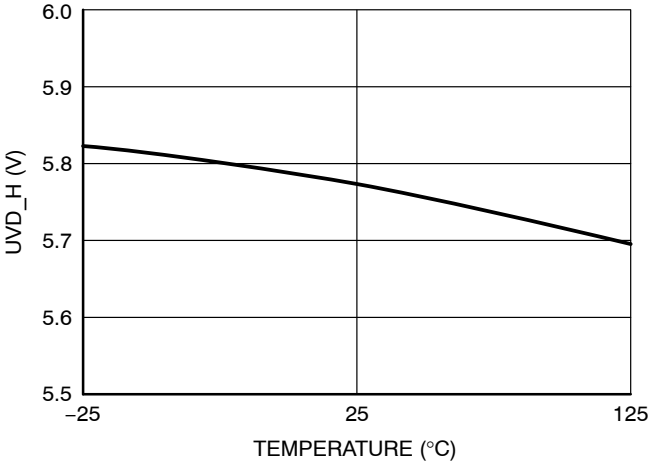


Figure 6. Undervoltage Lockout Upper Threshold vs. Temperature

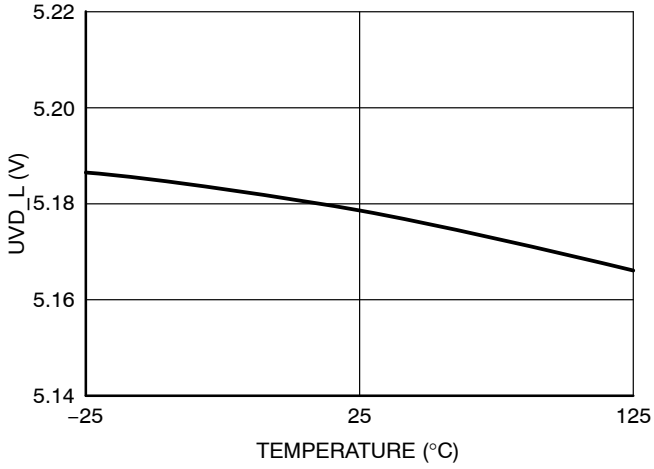


Figure 7. Undervoltage Lockout Lower Threshold vs. Temperature

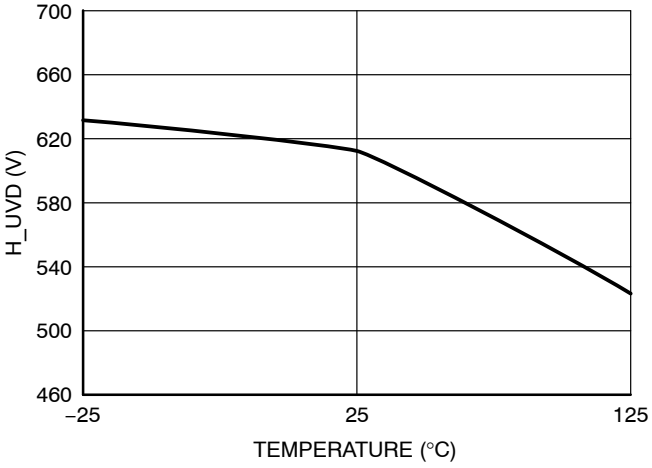


Figure 8. Undervoltage Lockout Hysteresis vs. Temperature

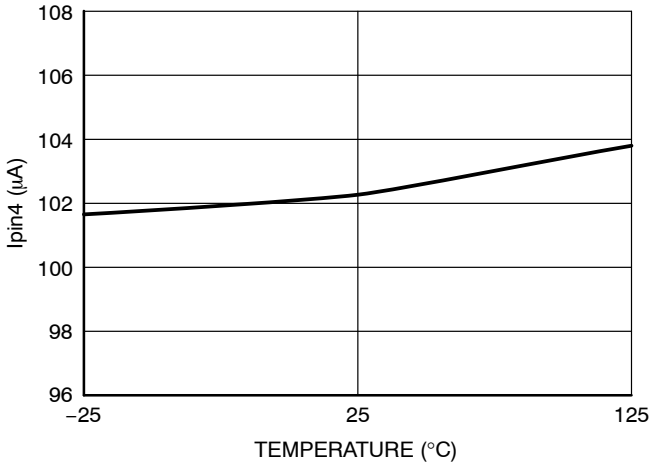


Figure 9. Pin4 Charge Current vs. Temperature (@ Ipin5 = 100 μA)

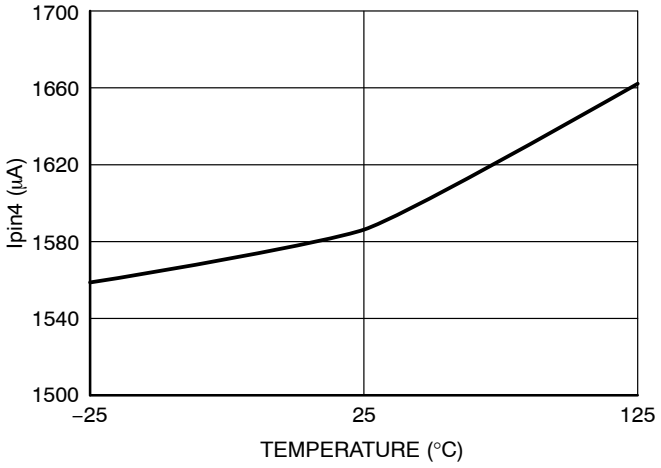


Figure 10. Pin4 Charge Current vs. Temperature (@ Ipin5 = 1.5 mA)

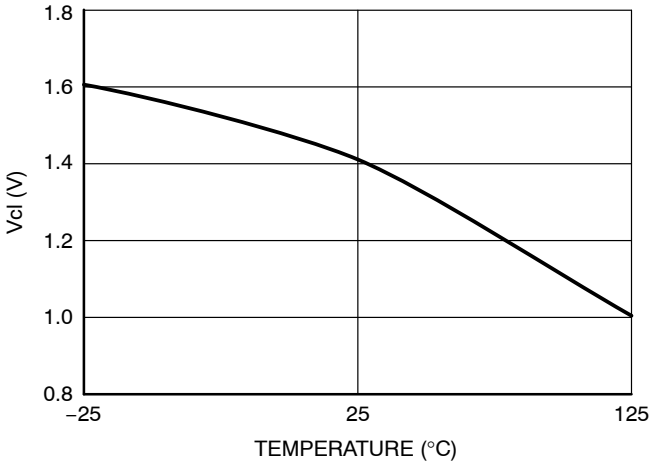


Figure 11. Pin5 Clamp Voltage vs. Temperature

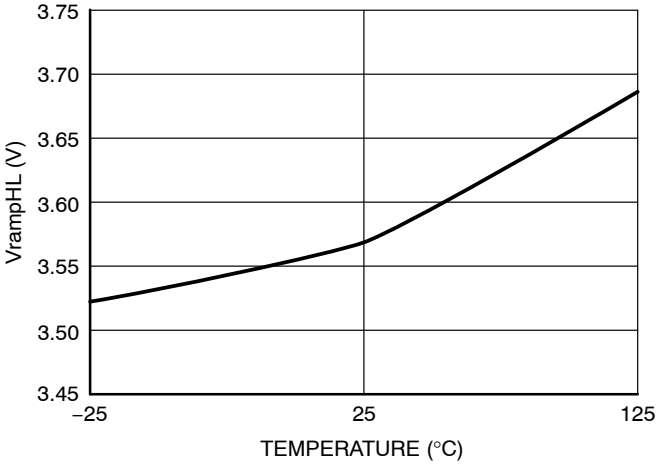


Figure 12. Pin4 Clamp Voltage vs. Temperature

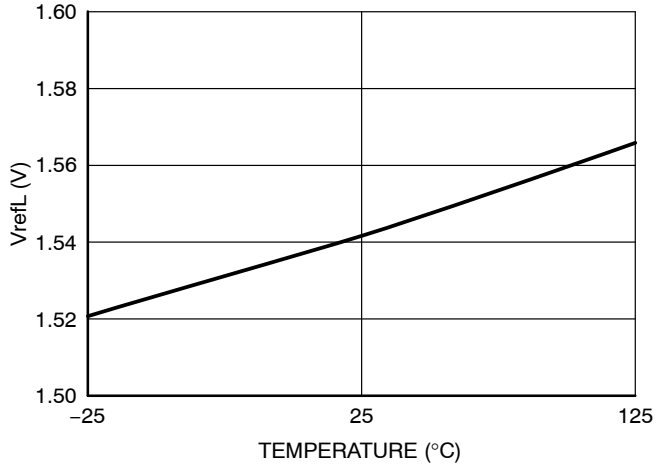


Figure 13. Ramp Control Reference Voltage vs. Temperature (Vpin4 falling)

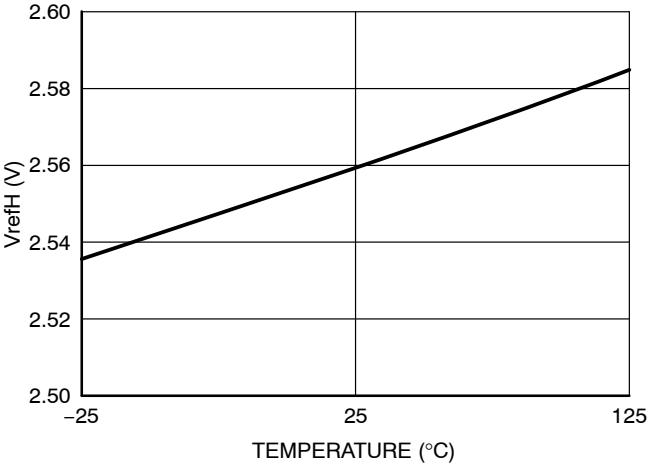


Figure 14. Ramp Control Reference Voltage vs. Temperature (Vpin4 rising)

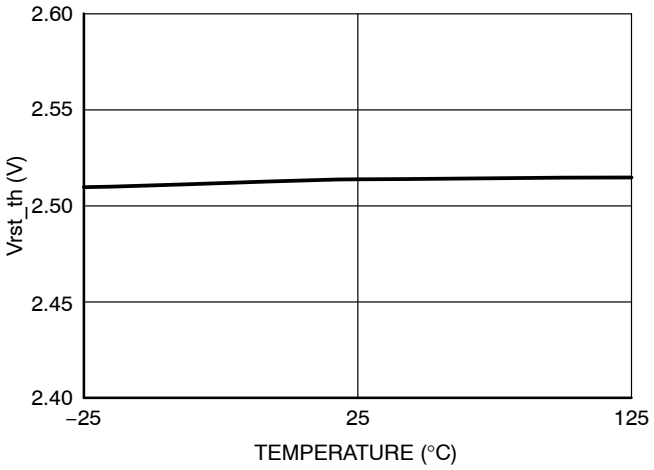


Figure 15. Reset Threshold vs. Temperature (Vpin3 rising)

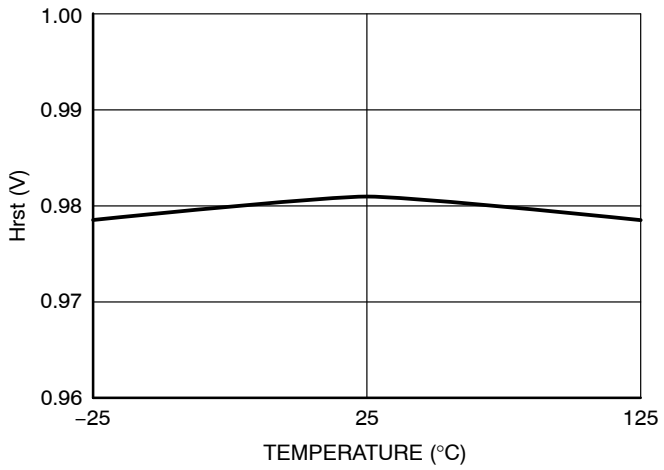


Figure 16. Reset Comparator Hysteresis vs. Temperature

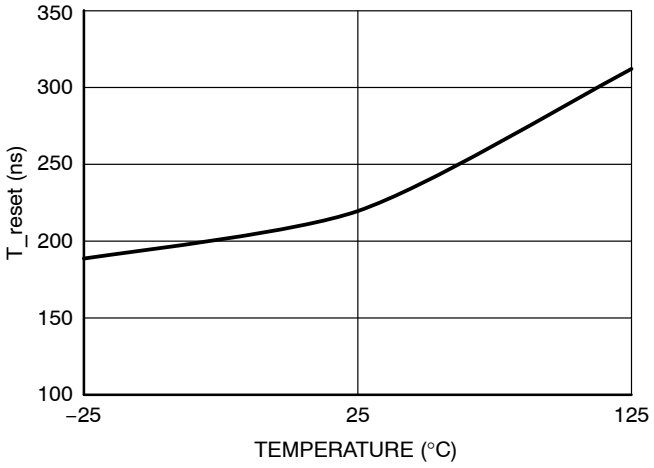


Figure 17. Reset Time vs. Temperature

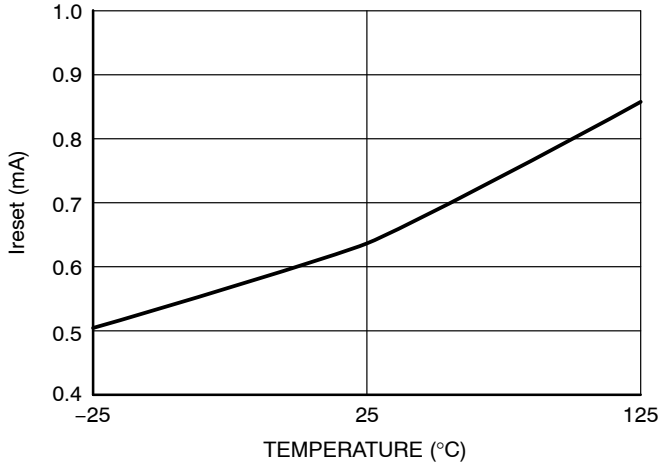


Figure 18. Pin4 Average Sink Current vs. Temperature (@ f = 200 kHz, Vpin4 = 1 V and Iramp = 0 A)

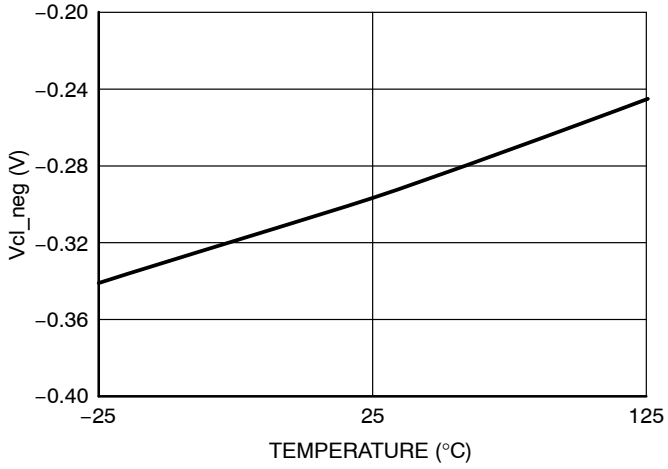


Figure 19. Pin3 Negative Clamp Voltage vs. Temperature (@ Ipin3 = −2 mA)

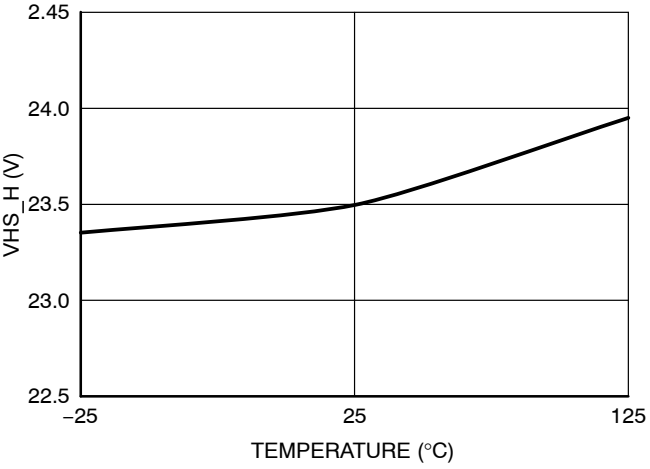


Figure 20. High−Side Drive Voltage vs. Temperature (high state, Isource = −100 mA, @ Vbst = 25 V)

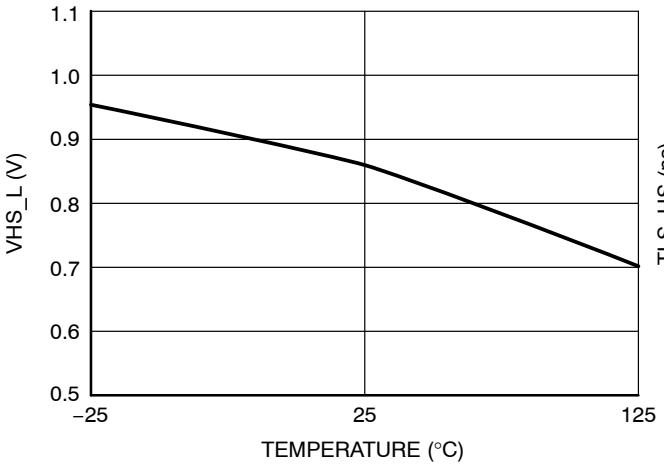


Figure 21. High−Side Drive Voltage vs. Temperature (low state, Isink = 100 mA, @ Vbst = 25 V)

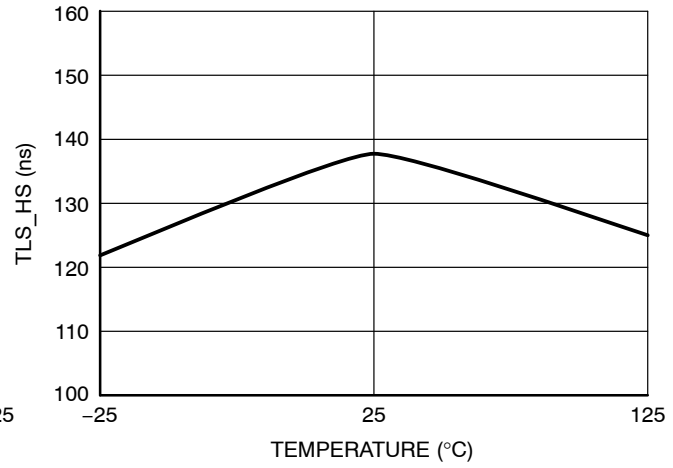


Figure 22. Low Side to High Side Delay vs. Temperature

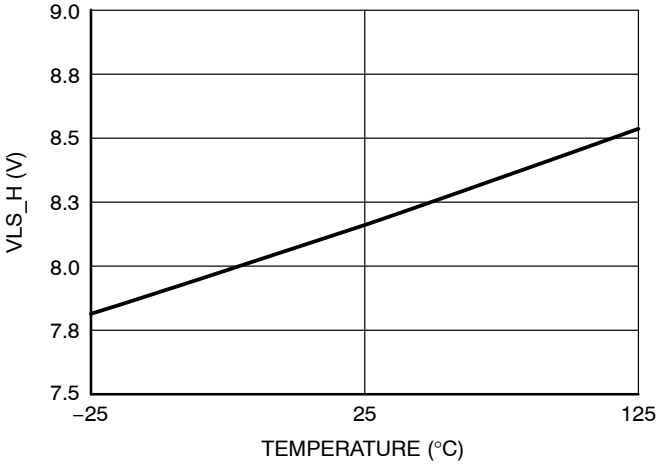


Figure 23. Low−Side Drive Voltage vs. Temperature (high state, Isource = −500 mA, @ V_{DD} = 10 V)

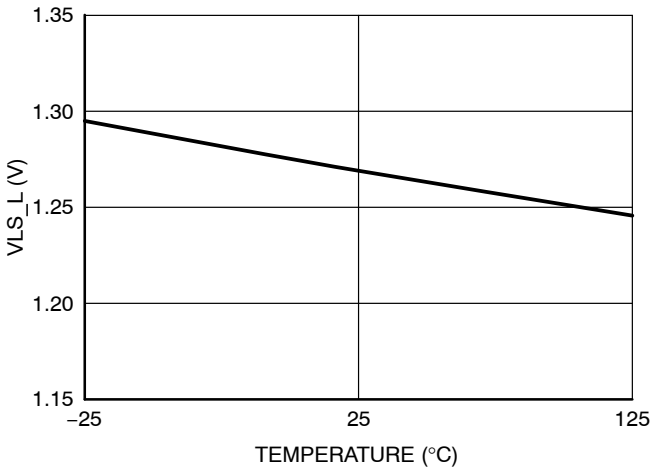


Figure 24. Low−Side Drive Voltage vs. Temperature (low state, Isink = 750 mA, @ V_{DD} = 10 V)

DETAILED OPERATING DESCRIPTION

Introduction

The NCP4330 is designed for forward, multiple output power supplies using synchronous rectification. One output is traditionally regulated thanks to a regulation arrangement that modulates the forward converter duty cycle. The other outputs are regulated by a dual MOSFET arrangement driven by the NCP4330. The high−side MOSFET turns on during one part of the forward converter on−time, while the low−side power switch is ON for the rest of the period (free wheeling).

The sequencing of the switching phases, includes over−laps that result in only one hard switching (high−side turn on). The three other transitions are soft for an optimum efficiency.

The synchronous rectification enables to keep a Continuous Conduction Mode (CCM) operation whatever the load is, as this technique allows to send back some energy towards the input (light load conditions). In Continuous Conduction Mode (CCM), the forward duty cycle is simply given by the following equation:

$$d_f = \frac{Vout1}{(n_s / n_p) * Vin}$$

where: – d_f is the forward duty cycle,
– n_s/n_p is the transformer turn ratio (n_p: primary number of turns, n_s: secondary number of turns),
– Vin is the forward converter input voltage,
– Vout1 is the main output voltage of the forward converter.

The post−regulated output voltages are given by the following equation:

$$Vout_n = d_n * \frac{n_s}{n_p} * Vin,$$

where d_n is the duty cycle of the post−regulator n, with $d_n < d_f$ since (n_s*Vin/n_p) is available only during the forward converter on−time.

Post−regulated output voltages are then necessarily lower than the main regulated one.

Sequencing and Regulation Block

The timing diagram of page 2 portrays the phases sequencing.

Typically, a regulation arrangement injects a current into pin 5, in order to adjust the high−side MOSFET duty cycle. Pin 5 current is internally mirrored in order to charge the C_{ramp} capacitor. An internal comparator (1.0 V hysteresis) detects when the capacitor voltage exceeds the 2.5 V internal reference. At that moment, the low−side MOSFET turns off. 100 ns later (typically), the high–side MOSFET switches on and keeps on until (following the turn off of the forward converter power switch) a RESET signal is applied to pin 3. At that time, an internal switch grounds the C_{ramp} pin and abruptly discharges the C_{ramp} capacitor. As a consequence, the internal comparator turns low and forces the low−side MOSFET on. The high−side MOSFET turns off 100 ns later.

During the 100 ns during which both high and low side MOSFETs are on, the MOSFET Q1 of the application schematic is off and no energy can then be drawn from the converter transformer. Therefore, these 100 ns should not be considered as a part of the high−side MOSFET conduction time which can be computed as follows:

$$t_{on\_HS} = T_{sw} - t_{RST} - t_{LS,HS} - t_{charge}$$

where: – T_{sw} is the forward switching period,
– t_{RST} is the C_{ramp} reset time during which the capacitor is kept grounded,
– $t_{LS,HS}$ is the delay between the low−side turn off and the high−side switch on. During this time, 100 ns typically, the two drivers are in low state,
– t_{charge} is the time necessary to charge the C_ramp capacitor up to the 2.5 V reference voltage.

Given that:

$$t_{charge} = \frac{C_{ramp} * Vref}{I_{ramp}}$$

where: – C_{ramp} is the capacitor connected to the C_ramp pin,
– I_{ramp} is the current injected into the I_ramp pin,
– Vref is the 2.5 V reference voltage,

the following equation dictates the high−side MOSFET duty cycle:

$$d_{on\_HS} = 1 - \frac{t_{RST} + t_{LS,HS} + \frac{C_{ramp}*Vref}{I_{ramp}}}{T_{sw}}$$

The following curve gives d_{on_HS} versus the current I_{ramp} in the following conditions: 400 kHz switching frequency, 250 ns reset pulse duration, 100 ns switching delay (between LS and HS), 100 pF C_{ramp} capacitor.

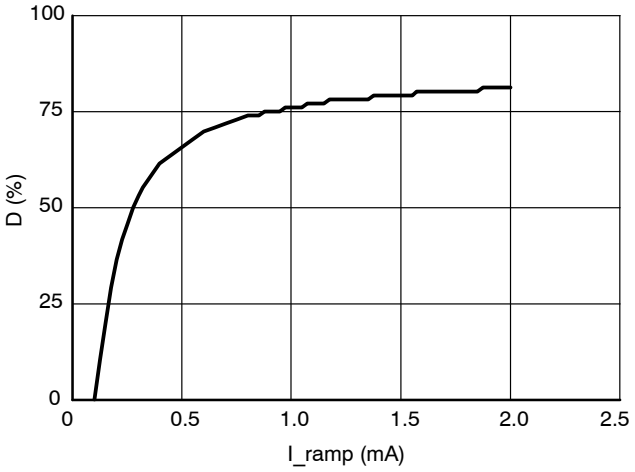


Figure 25. High−Side MOSFET Duty Cycle vs. I_ramp
Conditions: Switching Frequency: 400 kHz, Reset Pulse Duration: 250 ns, Switching Delay (between LS and HS): 100 ns, Cramp = 100 pF.

One can note that the duty cycle increases when the I_ramp current increases. The duty cycle is zero if the I_ramp current is below about 110 μA.

The duty cycle is limited to about 81% mainly by the reset time and the 100 ns delay that all together represent 14% of the period. In a 100 kHz application, the relative impact of these times would be reduced and the maximum duty cycle would be higher (in the range of 92%).

In fact, the high−side on−times are useful only during the forward on−times. ***Finally, if the duty cycle of the forward converter is less than 80%, one can consider that the useful post regulator duty cycle can vary between 0 and 100%.***

It can also be noted that the HS MOSFET can be turned on while the forward power switch is off, the forward free−wheeling MOSFET (Q2) is on and then no voltage is applied to the post−regulator. This is not an issue since the MOSFETs Q2 and Q3 derive the L2 coil current so that the free wheeling operation continues (refer to application schematic).

However, such a situation should occur only during transient phases. Should this state occur too frequently, an excessive heating of the Q2 switch could be produced.

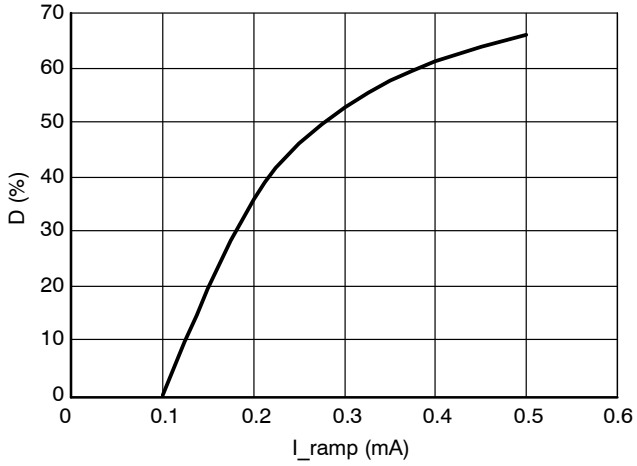


Figure 26. HS MOSFET Duty Cycle vs. I_ramp (zoom)

RESET Block

The “reset” pin should receive the free−wheeling drive signal of the forward (refer to application schematic). When this voltage exceeds the reset block threshold (2.55 V typically), the C_ramp capacitor is grounded by an internal switch for about 250 ns and the low−side MOSFET is turned on. The circuit is then initialized for a new cycle.

The voltage that is applied to the “reset” pin, may be negative during one part of the period. The NCP4330 incorporates a negative clamp system to avoid that too negative voltages on the pin may cause carriers injection within the die. The negative clamp acts to force a minimum voltage of about –0.3 V in conjunction with the external resistor R3. It features a current capability of about 2.0 mA.

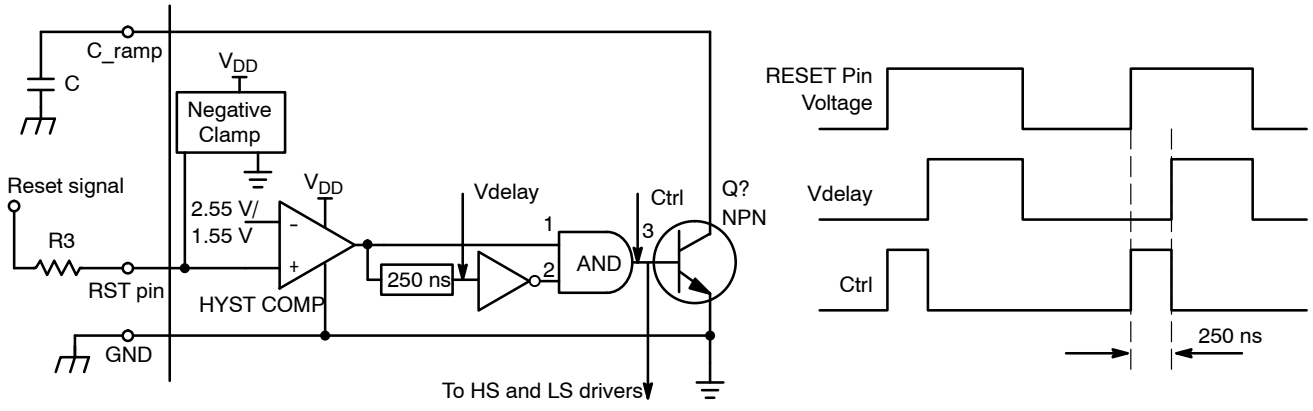


Figure 27. Reset Block

Low−Side Driver Stage

The timing diagram of page 2 portrays the sequencing driven by the NCP4330.

The low−side drive is controlled by an internal comparator that compares the C_ramp voltage to the internal reference 2.5 V (1.0 V hysteresis). When the C_ramp exceeds the 2.5 V reference, the comparator turns high forcing the low−side MOSFET off. 100 ns later, the high−side MOSFET switches on.

When a reset signal is applied to the reset pin, the C_ramp capacitor is grounded. As a consequence, the internal comparator turns low and forces the low−side MOSFET on. 100 ns later, the high−side MOSFET switches off.

The low−side drive is designed to drive on and off a 25 nC gate charge power MOSFET, in 25 ns typical.

1. Low−Side MOSFET Turn On:

In nominal operation, the body diode is already ON when the low−side MOSFET turns on. The energy Qg to be supplied is then approximately half the energy necessary if the drain source voltage was high.

The necessary current capability is then:

$$I_{ls\ -\ on} = \frac{1}{2} * \frac{25\ nC}{25\ ns}$$, that is 500 mA.

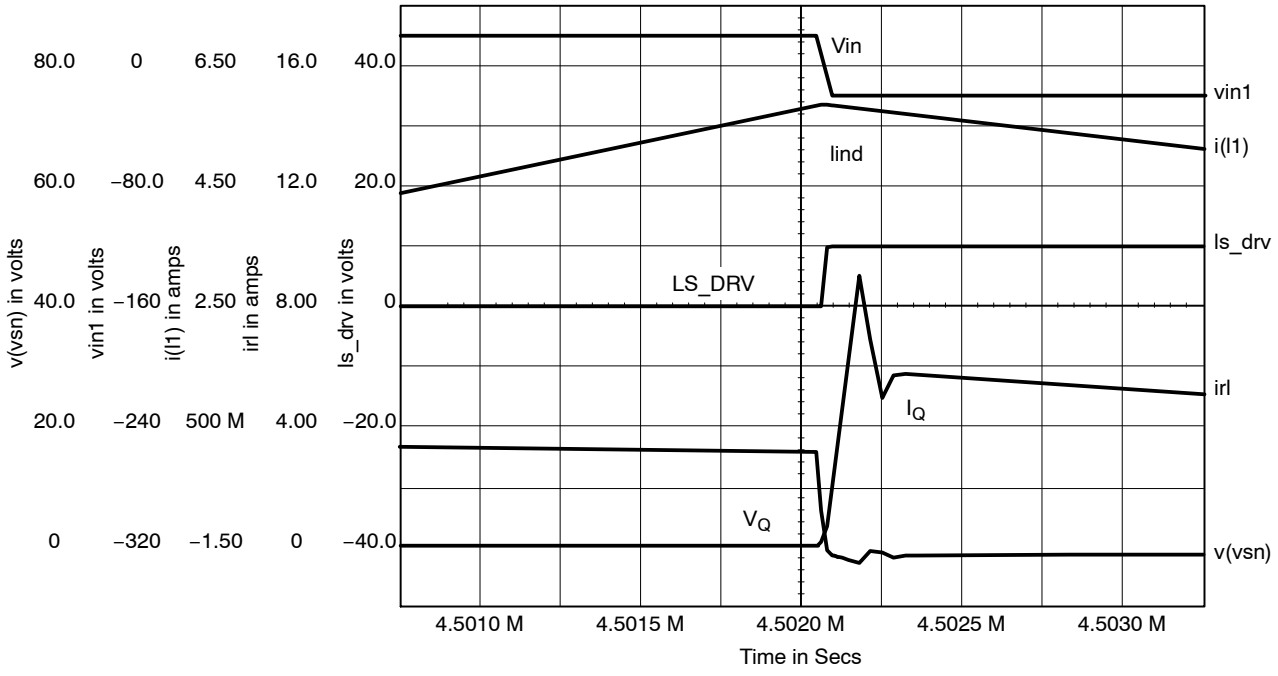


Figure 28. Low−Side MOSFET Turn ON

2. Low−Side MOSFET Turn Off:

The high−side MOSFET turns on about 100 ns after the low−side one is switched off. During this time when both switches are off, the body diode of the low−side MOSFET derives the inductor current (in nominal load condition, when the coil current is positive, i.e., it flows toward the output). As a result, the LS MOSFET turns off while its drain−source voltage keeps around zero due to its body diode activation.

Again, the energy Qg to be supplied is then approximately half its value if the drain source voltage was high.

The necessary current capability is then:

$$I_{ls\ -\ off} = \frac{1}{2} * \frac{25\ nC}{25\ ns}$$, that is 500 mA.

High dV/dt occur in the application. When the high−side MOSFET turns on, the drain−source voltage of the low−side MOSFET sharply increases, producing a huge current through the Crss capacitor. This current may produce some parasitic turn on of the LS MOSFET if the driver impedance is not low enough to absorb this current without significant increase of the driver voltage. The driver current capability has then been increased to 750 mA so that it can effectively face a 30 V variation in 10 ns with a MOSFET exhibiting a 250 pF Crss.

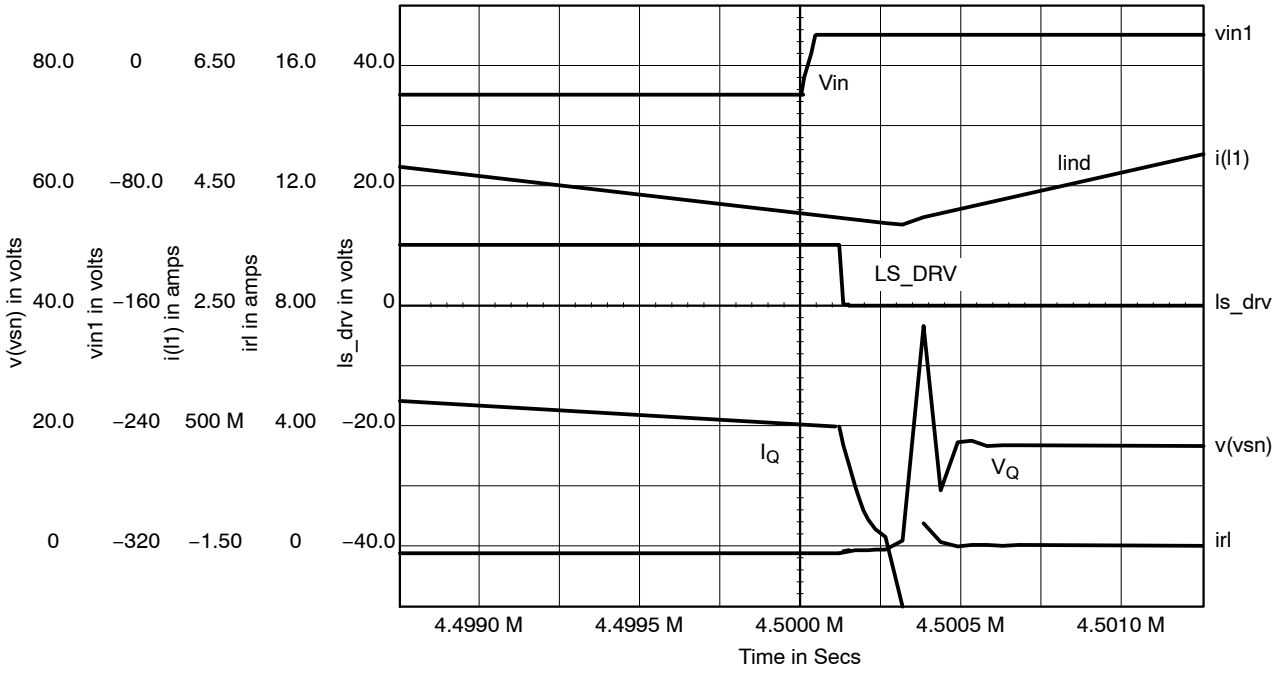


Figure 29. Low−Side MOSFET Turn Off

High−Side Driver Stage

The high−side turn on (turn off) is 100 ns delayed behind the low−side turn off (turn on).

The high−side drive is designed to drive on and off 12.5 nC gate charge power MOSFET, in 25 ns typical.

1. High−Side Turn On:

As portrayed by in figure 30, the high−side turn on is a “hard” switching (large dV/dt and dI/dt).

The necessary current capability is then:

$I_{hs\ -\ on} = \frac{12.5\ nC}{25\ ns}$, that is 500 mA.

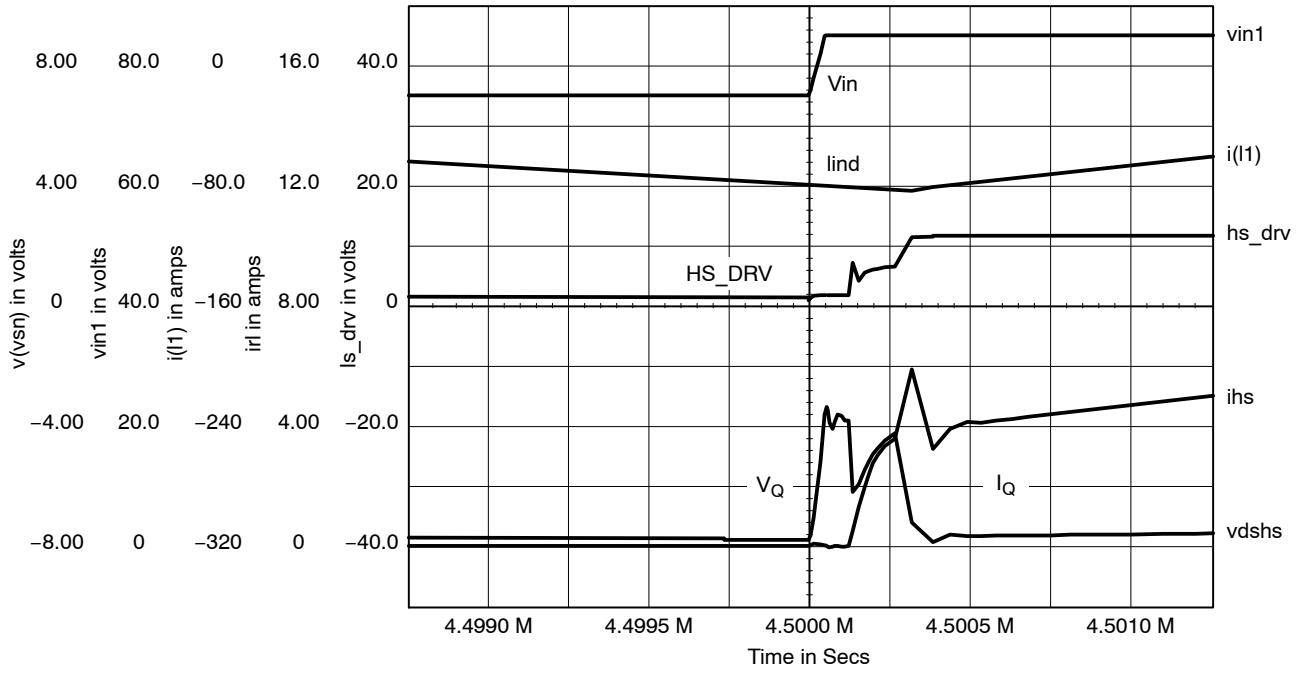


Figure 30. High−Side MOSFET Turn On

2. High−Side Turn Off:

The high−side MOSFET turns in a very soft way (no current, no voltage). The turn off drive is in fact designed to face the high dV/dt that occurs when the MOSFET Q1 abruptly turns on. The current capability has been set to 750 mA so that a 30 V variation in 10 ns cannot parasitically switch on a high−side MOSFET exhibiting a 250 pF Crss.

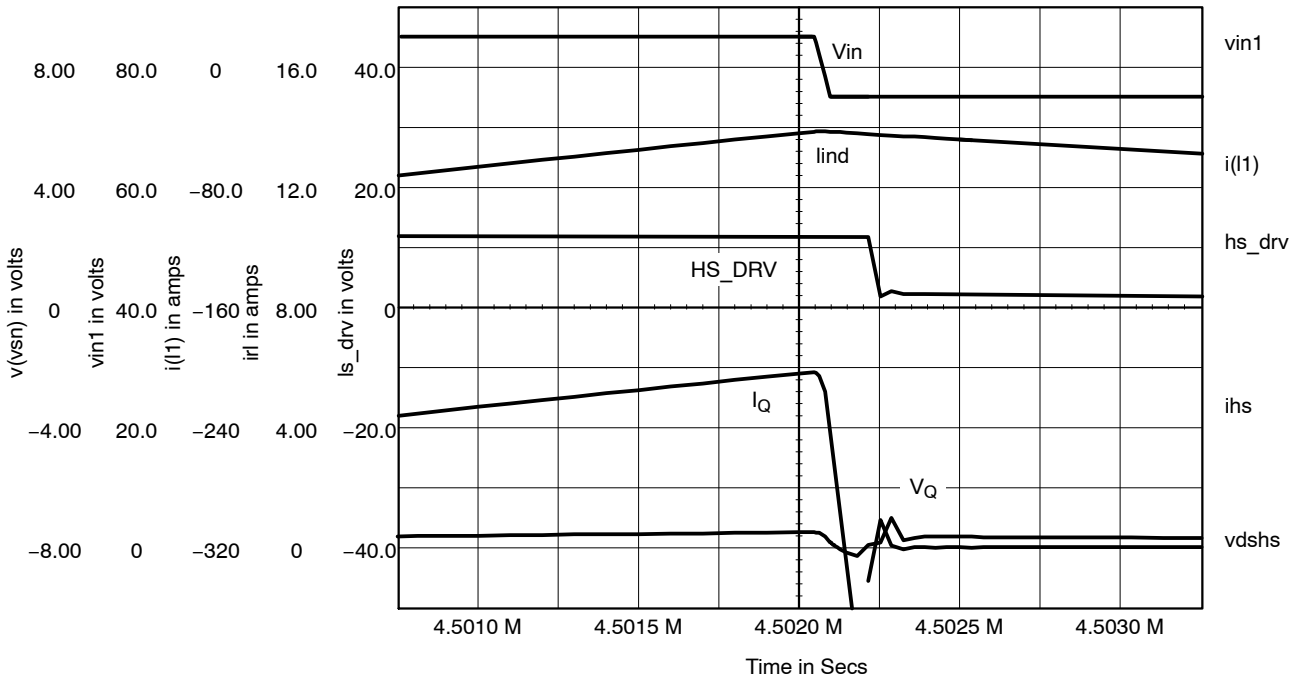


Figure 31. High−Side MOSFET Turn Off

3. Input Voltage Limitation:

Traditional high−side drivers turn off the MOSFET they control, by forcing nearly 0 V between gate and source. The NCP4330 high−side stage is not referenced to the MOSFET source but to ground, and the HS MOSFET is forced off by grounding its gate. This technique that saves the pin that is traditionally connected to the MOSFET source, allows a robust turn off of the power switch. In effect, the low−side MOSFET that is ON when the high−side is off, forces the High−side MOSFET source to approximately 0 V.

However the high−side MOSFET turn on is preceded by a 100 ns phase during which both the low−side and high−side power switches are off. During this 100 ns phase, the drain source voltage of the low−side MOSFET may get high, given that in light load operation, the L2 coil current may get negative and flow from the load toward the input through the HS MOSFET body diode. In this case, the gate source voltage of the high−side MOSFET becomes negative and substantially equal to the input voltage amplitude of the post−regulator in absolute value.

Therefore, the maximum value of the pulsed input voltage should be chosen lower than the maximum source−gate voltage the HS MOSFET can sustain. Traditional MOSFET Vgs maximum ratings are generally +/−20 V. Therefore, with this kind of MOSFETs, the input voltage must keep below 20 V (possible spikes being included).

Undervoltage Lockout

An undervoltage lockout comparator is incorporated to guarantee that the device is fully functional before enabling the output stages. The NCP4330 starts to operate when the power supply V_{DD} exceeds 5.8 V. A 600 mV hysteresis avoids that some noise on the V_{DD} might produce some erratic turns on and off of the device. When the NCP4330 detects an undervoltage lockout condition, it keeps both the high−side and low−side drivers in low state.

The undervoltage lockout has a 4.9 V minimum threshold (falling). As a consequence, around 3.4 V are available on the driver outputs to force on the MOSFET. Such a level allows to properly drive most MOSFETs.

APPLICATIONS INFORMATION

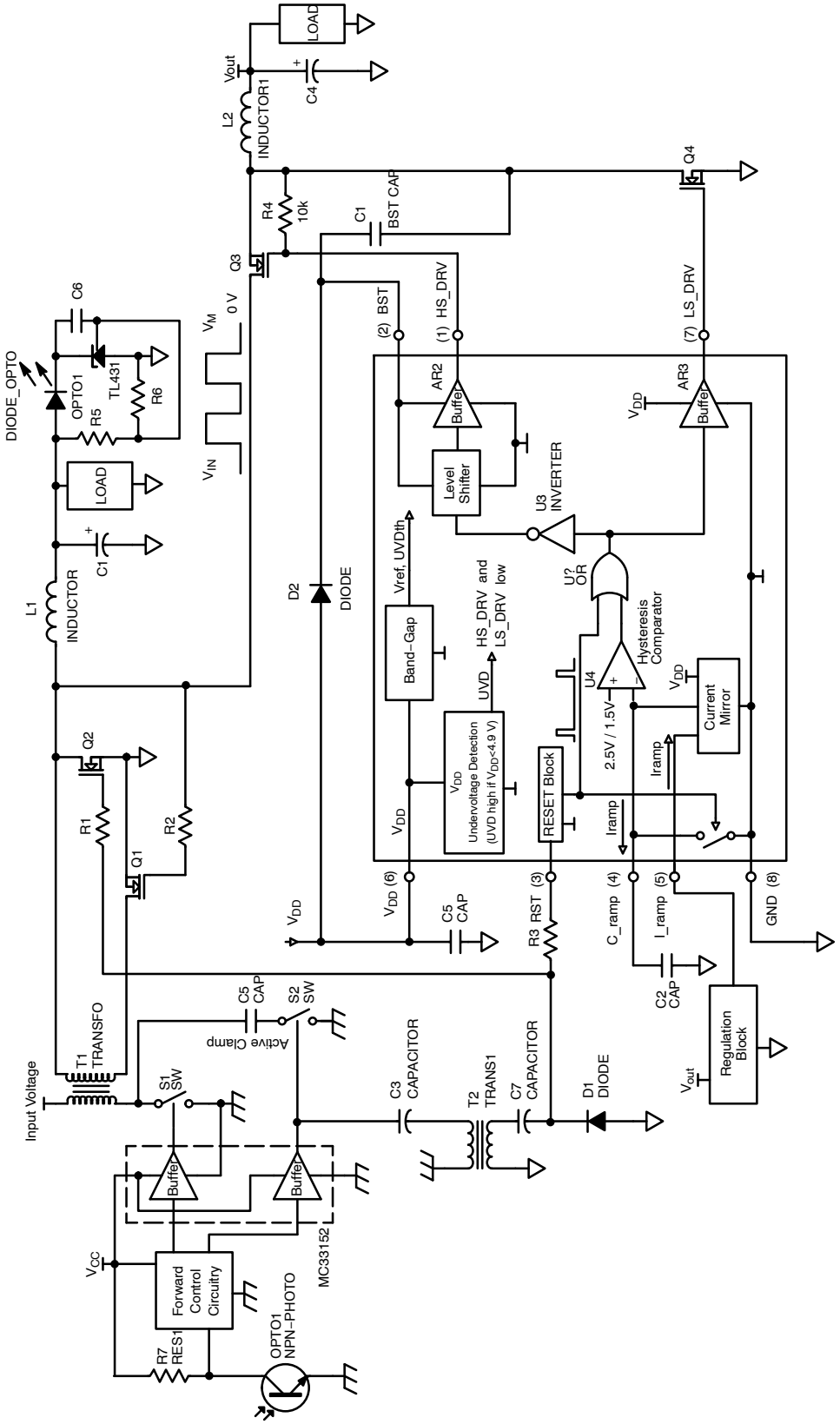


Figure 32. Typical Application

The maximum value (V_M) of the pulsed input voltage (V_{IN}) must be kept lower than the maximum source−gate voltage the HS MOSFET can sustain

If the input voltage may exceed the maximum source−gate voltage the HS MOSFET can sustain, an intermediary stage should be inserted between the NCP4330 and the HS MOSFET. Figure 33 presents a solution consisting of a diode, a PNP and a resistor (in the range of 500 Ω). The HS MOSFET is normally turned on through the diode while the PNP Q2 enables to drive the MOSFET between gate and source at turn off.

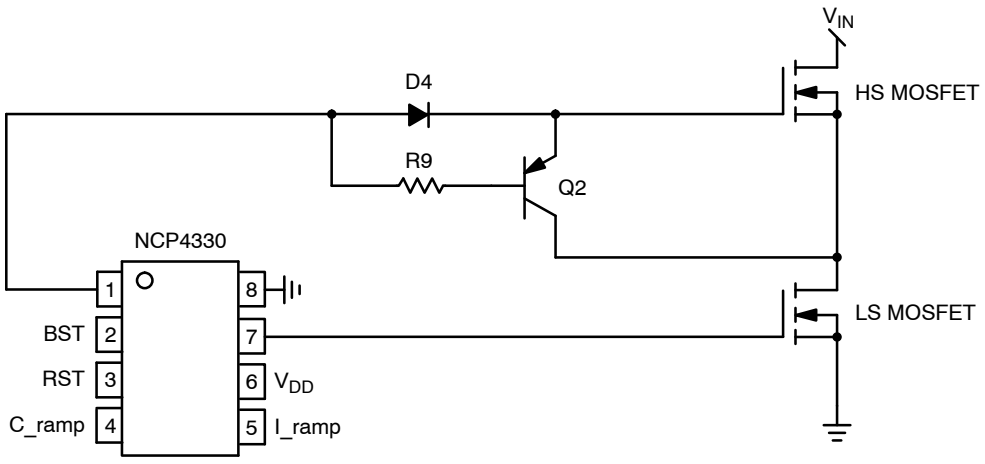
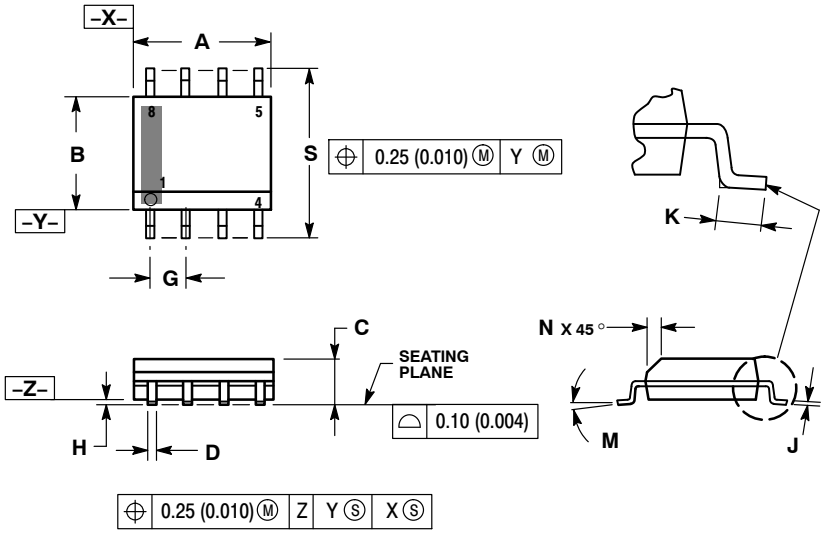


Figure 33.

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

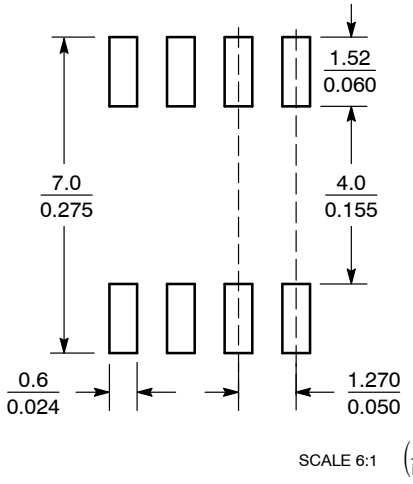
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

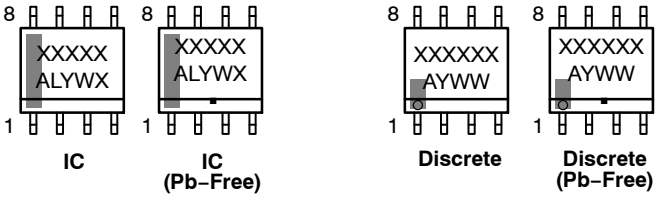
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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