

# MTD6N15

## Power Field Effect Transistor DPAK for Surface Mount N-Channel Enhancement-Mode Silicon Gate

This Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

### Features

- Silicon Gate for Fast Switching Speeds
- Low  $R_{DS(on)}$  — 0.3  $\Omega$  Max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement —  $V_{GS(th)} = 4.0$  V Max
- Surface Mount Package on 16 mm Tape
- Pb-Free Package is Available

### MAXIMUM RATINGS

| Rating                                                                                                                                                 | Symbol                | Value                | Unit                     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|----------------------|--------------------------|
| Drain-Source Voltage                                                                                                                                   | $V_{DS}$              | 150                  | Vdc                      |
| Drain-Gate Voltage ( $R_{GS} = 1.0$ M $\Omega$ )                                                                                                       | $V_{DGR}$             | 150                  | Vdc                      |
| Gate-Source Voltage <ul style="list-style-type: none"><li>– Continuous</li><li>– Non-Repetitive (<math>t_p \leq 50</math> <math>\mu</math>s)</li></ul> | $V_{GS}$<br>$V_{GSM}$ | $\pm 20$<br>$\pm 40$ | Vdc<br>Vpk               |
| Drain Current – Continuous <ul style="list-style-type: none"><li>– Pulsed</li></ul>                                                                    | $I_D$<br>$I_{DM}$     | 6.0<br>20            | Adc                      |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$                                                                  | $P_D$                 | 20<br>0.16           | W<br>W/ $^\circ\text{C}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ (Note 1)                                                         | $P_D$                 | 1.25<br>0.01         | W<br>W/ $^\circ\text{C}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$<br>(Note 1)<br>Derate above $25^\circ\text{C}$ (Note 2)                                             | $P_D$                 | 1.75<br>0.014        | W<br>W/ $^\circ\text{C}$ |
| Operating and Storage Junction<br>Temperature Range                                                                                                    | $T_J, T_{stg}$        | –65 to +150          | $^\circ\text{C}$         |

### THERMAL CHARACTERISTICS

| Characteristic                                                                                                                                                      | Symbol                                                | Value               | Unit               |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|---------------------|--------------------|
| Thermal Resistance <ul style="list-style-type: none"><li>– Junction-to-Case</li><li>– Junction-to-Ambient (Note 1)</li><li>– Junction-to-Ambient (Note 2)</li></ul> | $R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | 6.25<br>100<br>71.4 | $^\circ\text{C/W}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. When surface mounted to an FR4 board using 0.5 sq. in. drain pad size.

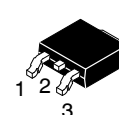
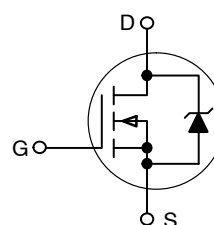


ON Semiconductor®

<http://onsemi.com>

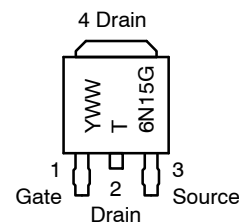
| $V_{(BR)DS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|--------------|------------------|-----------|
| 150 V        | 0.3 $\Omega$     | 6.0 A     |

### N-CHANNEL



CASE 369C  
DPAK  
(Surface Mount)  
STYLE 2

### MARKING DIAGRAM & PIN ASSIGNMENTS



Y = Year  
WW = Work Week  
6N15 = Device Code  
G = Pb-Free Package

### ORDERING INFORMATION

| Device     | Package           | Shipping†        |
|------------|-------------------|------------------|
| MTD6N15T4  | DPAK              | 2500/Tape & Reel |
| MTD6N15T4G | DPAK<br>(Pb-Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# MTD6N15

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|----------------|--------|-----|-----|------|
|----------------|--------|-----|-----|------|

### OFF CHARACTERISTICS

|                                                                                                                                |               |     |           |                 |
|--------------------------------------------------------------------------------------------------------------------------------|---------------|-----|-----------|-----------------|
| Drain-Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 0.25\text{ mAdc}$ )                                          | $V_{(BR)DSS}$ | 150 | –         | Vdc             |
| Zero Gate Voltage Drain Current<br>( $V_{DS} = \text{Rated } V_{DSS}$ , $V_{GS} = 0\text{ Vdc}$ )<br>$T_J = 125^\circ\text{C}$ | $I_{DSS}$     | –   | 10<br>100 | $\mu\text{Adc}$ |
| Gate-Body Leakage Current, Forward ( $V_{GSF} = 20\text{ Vdc}$ , $V_{DS} = 0$ )                                                | $I_{GSSF}$    | –   | 100       | nAdc            |
| Gate-Body Leakage Current, Reverse ( $V_{GSR} = 20\text{ Vdc}$ , $V_{DS} = 0$ )                                                | $I_{GSSR}$    | –   | 100       | nAdc            |

### ON CHARACTERISTICS (Note 3)

|                                                                                                                                              |              |            |            |          |
|----------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------|------------|----------|
| Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = 1.0\text{ mAdc}$ )<br>$T_J = 100^\circ\text{C}$                                          | $V_{GS(th)}$ | 2.0<br>1.5 | 4.5<br>4.0 | Vdc      |
| Static Drain-Source On-Resistance ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 3.0\text{ Adc}$ )                                                      | $R_{DS(on)}$ | –          | 0.3        | $\Omega$ |
| Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ )<br>( $I_D = 6.0\text{ Adc}$ )<br>( $I_D = 3.0\text{ Adc}$ , $T_J = 100^\circ\text{C}$ ) | $V_{DS(on)}$ | –<br>–     | 1.8<br>1.5 | Vdc      |
| Forward Transconductance ( $V_{DS} = 15\text{ Vdc}$ , $I_D = 3.0\text{ Adc}$ )                                                               | $g_{FS}$     | 2.5        | –          | mhos     |

### DYNAMIC CHARACTERISTICS

|                              |                                                                                                 |           |   |      |    |
|------------------------------|-------------------------------------------------------------------------------------------------|-----------|---|------|----|
| Input Capacitance            | $(V_{DS} = 25\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )<br>(See Figure 11) | $C_{iss}$ | – | 1200 | pF |
| Output Capacitance           |                                                                                                 | $C_{oss}$ | – | 500  |    |
| Reverse Transfer Capacitance |                                                                                                 | $C_{rss}$ | – | 120  |    |

### SWITCHING CHARACTERISTICS\* ( $T_J = 100^\circ\text{C}$ )

|                     |                                                                                                                      |              |           |     |    |
|---------------------|----------------------------------------------------------------------------------------------------------------------|--------------|-----------|-----|----|
| Turn-On Delay Time  | $(V_{DD} = 25\text{ Vdc}$ , $I_D = 3.0\text{ Adc}$ , $R_G = 50\ \Omega$ )<br>(See Figures 13 and 14)                 | $t_{d(on)}$  | –         | 50  | ns |
| Rise Time           |                                                                                                                      | $t_r$        | –         | 180 |    |
| Turn-Off Delay Time |                                                                                                                      | $t_{d(off)}$ | –         | 200 |    |
| Fall Time           |                                                                                                                      | $t_f$        | –         | 100 |    |
| Total Gate Charge   | $(V_{DS} = 0.8\text{ Rated } V_{DSS}$ ,<br>$I_D = \text{Rated } I_D$ , $V_{GS} = 10\text{ Vdc}$ )<br>(See Figure 12) | $Q_g$        | 15 (Typ)  | 30  | nC |
| Gate-Source Charge  |                                                                                                                      | $Q_{gs}$     | 8.0 (Typ) | –   |    |
| Gate-Drain Charge   |                                                                                                                      | $Q_{gd}$     | 7.0 (Typ) | –   |    |

### SOURCE-DRAIN DIODE CHARACTERISTICS\*

|                       |                                                                                         |          |                             |     |     |
|-----------------------|-----------------------------------------------------------------------------------------|----------|-----------------------------|-----|-----|
| Forward On-Voltage    | $(I_S = 6.0\text{ Adc}$ , $di/dt = 25\text{ A}/\mu\text{s}$ , $V_{GS} = 0\text{ Vdc}$ ) | $V_{SD}$ | 1.3 (Typ)                   | 2.0 | Vdc |
| Forward Turn-On Time  |                                                                                         | $t_{on}$ | Limited by stray inductance |     |     |
| Reverse Recovery Time |                                                                                         | $t_{rr}$ | 325 (Typ)                   | –   | ns  |

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

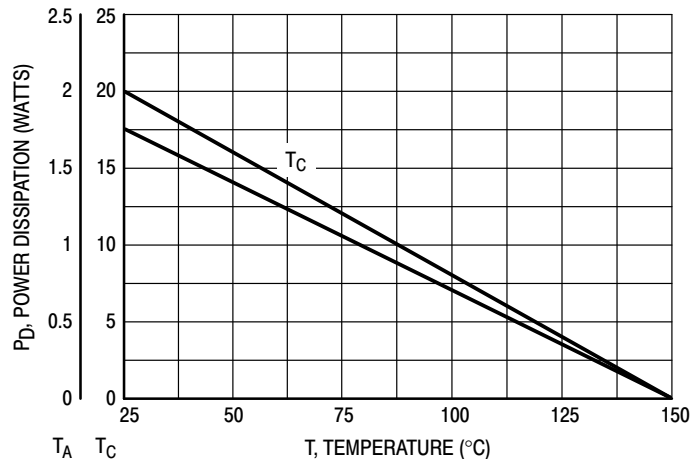


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

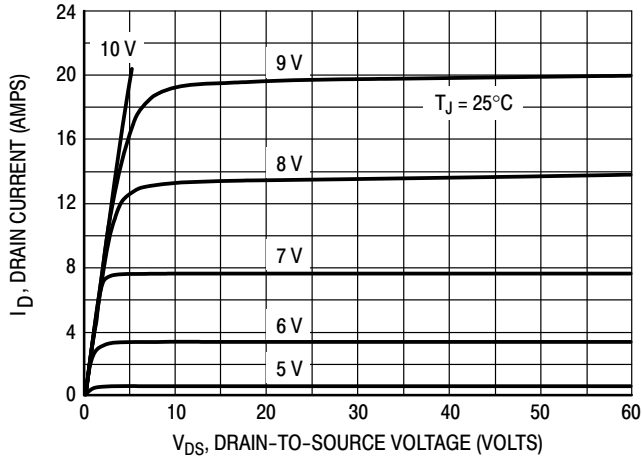


Figure 2. On-Region Characteristics

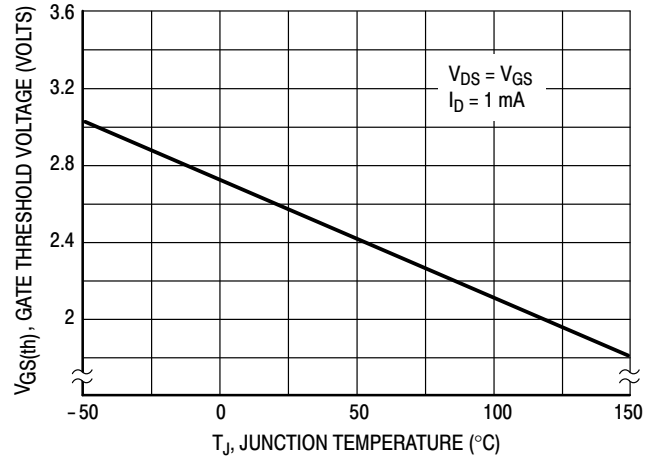


Figure 3. Gate-Threshold Voltage Variation With Temperature

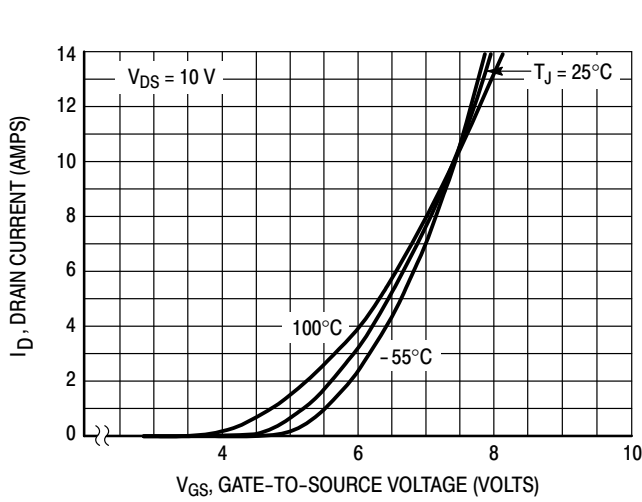


Figure 4. Transfer Characteristics

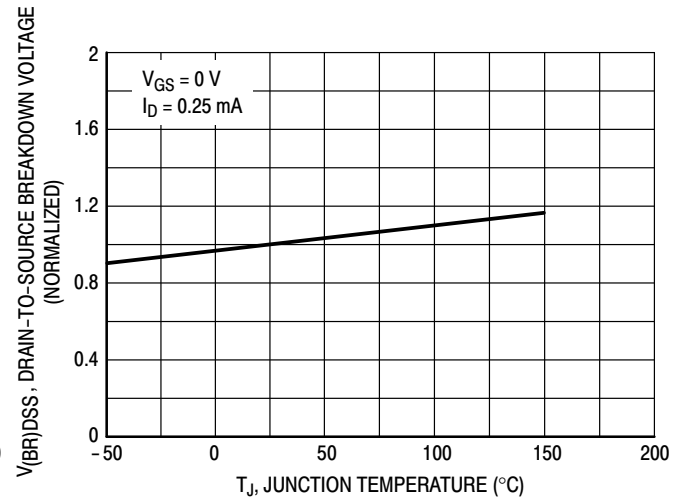


Figure 5. Breakdown Voltage Variation With Temperature

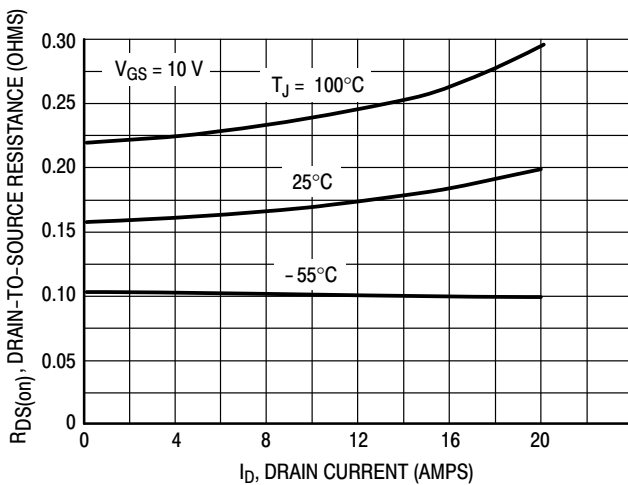


Figure 6. On-Resistance versus Drain Current

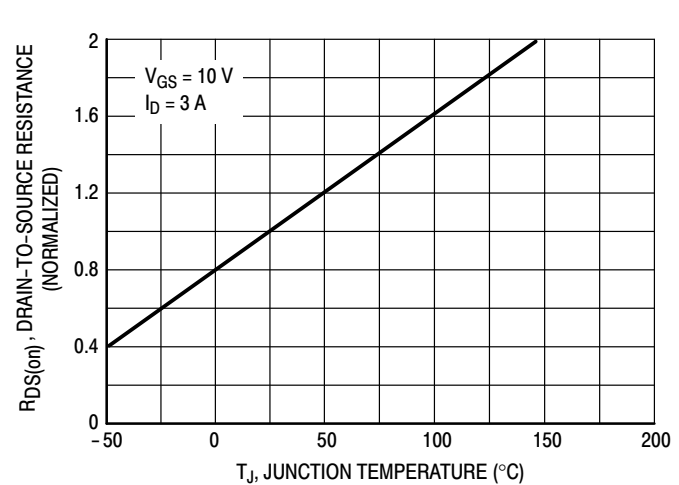


Figure 7. On-Resistance Variation With Temperature

# SAFE OPERATING AREA

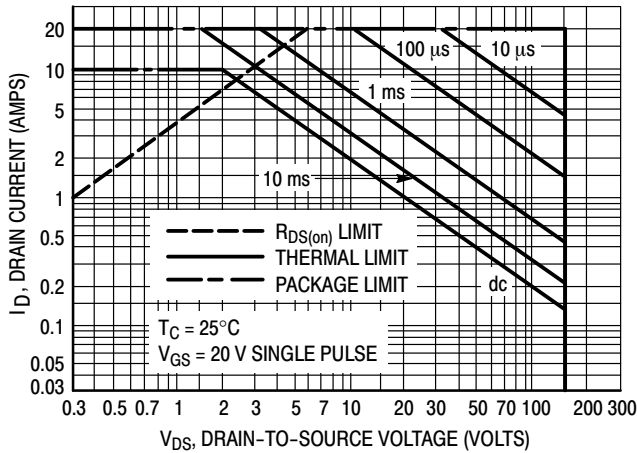


Figure 8. Maximum Rated Forward Biased Safe Operating Area

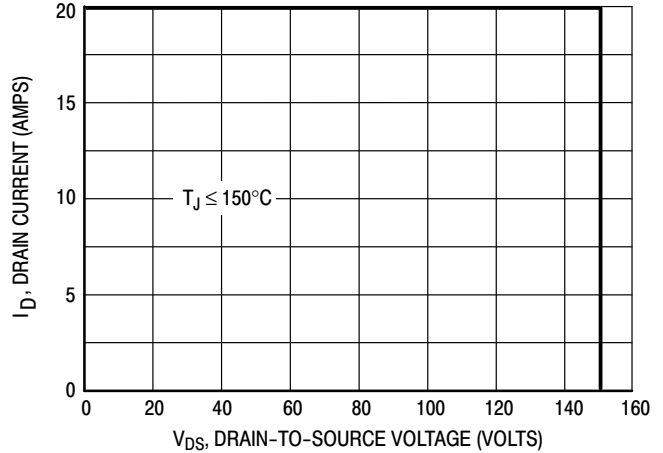


Figure 9. Maximum Rated Switching Safe Operating Area

## FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

## SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current,  $I_{DM}$  and the breakdown voltage,  $V_{(BR)DSS}$ . The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

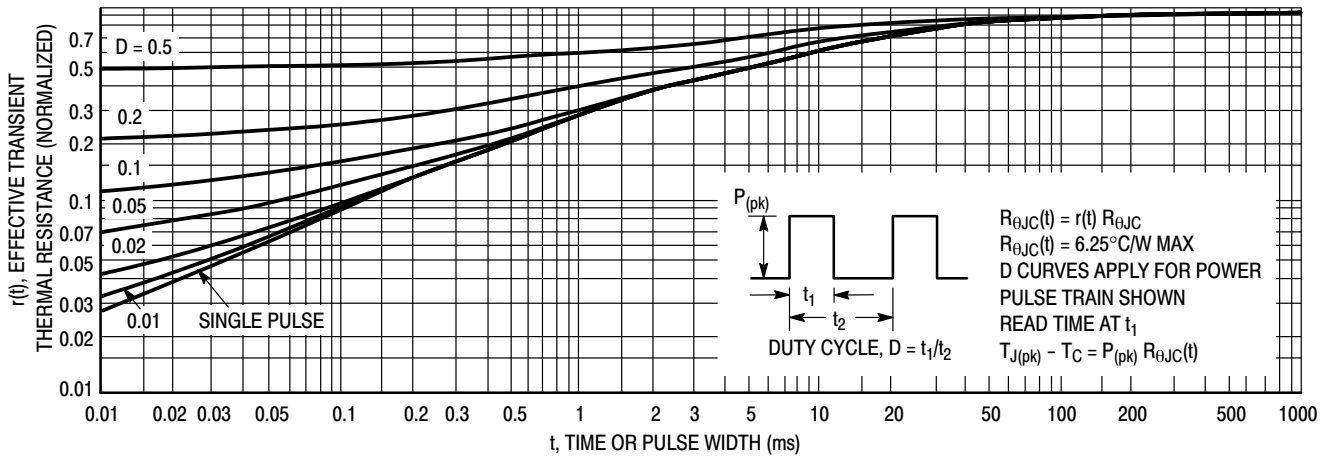


Figure 10. Thermal Response

# MTD6N15

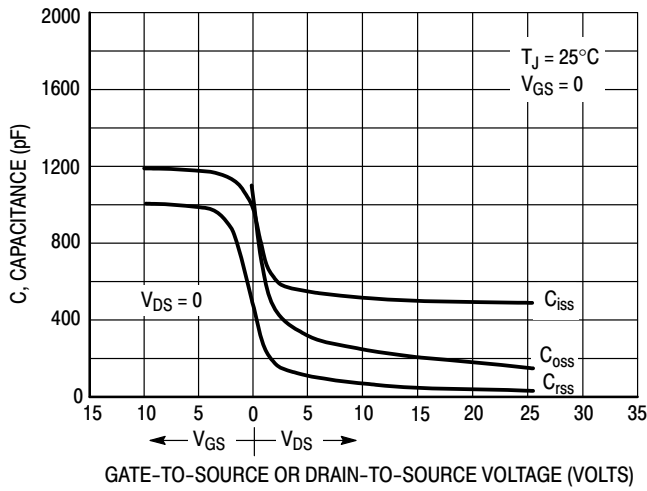


Figure 11. Capacitance Variation

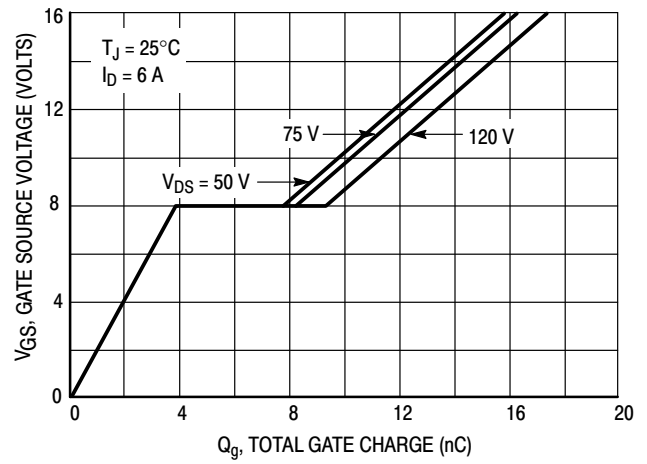


Figure 12. Gate Charge versus Gate-To-Source Voltage

## RESISTIVE SWITCHING

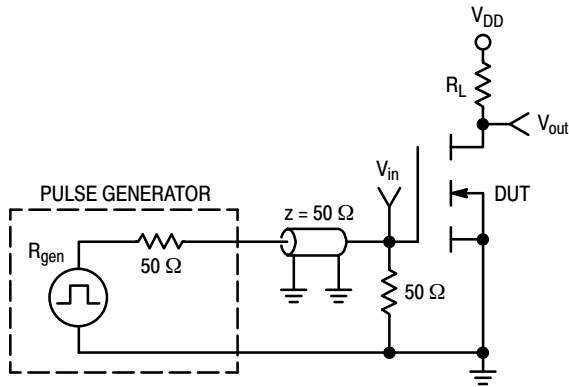


Figure 13. Switching Test Circuit

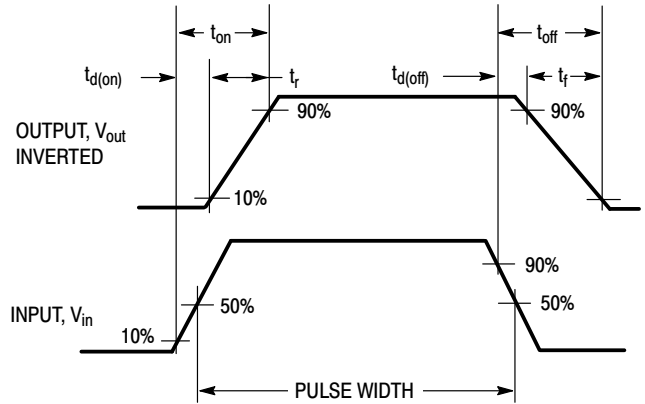


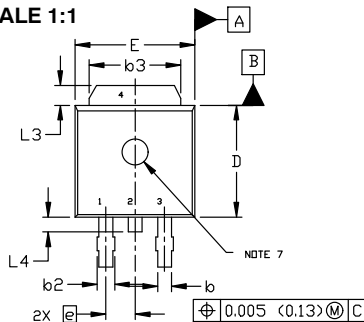
Figure 14. Switching Waveforms



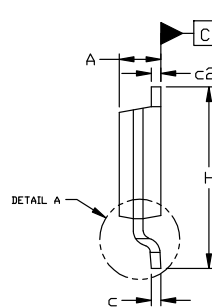
DPAK (SINGLE GAUGE)  
CASE 369C  
ISSUE G

DATE 31 MAY 2023

SCALE 1:1



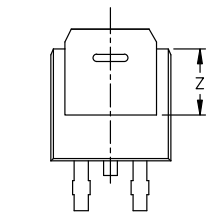
TOP VIEW



SIDE VIEW

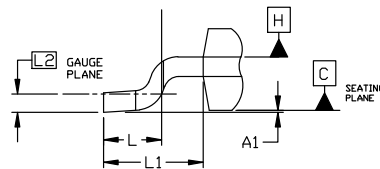
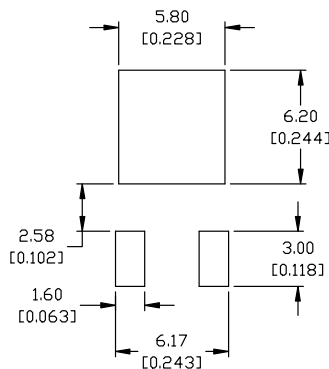


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE  
CONSTRUCTIONS



DETAIL A  
ROTATED 90° CW

NOTES:

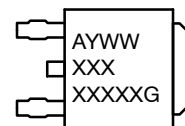
1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

| DIM | INCHES |       | MILLIMETERS |       |
|-----|--------|-------|-------------|-------|
|     | MIN.   | MAX.  | MIN.        | MAX.  |
| A   | 0.086  | 0.094 | 2.18        | 2.38  |
| A1  | 0.000  | 0.005 | 0.00        | 0.13  |
| b   | 0.025  | 0.035 | 0.63        | 0.89  |
| b2  | 0.028  | 0.045 | 0.72        | 1.14  |
| b3  | 0.180  | 0.215 | 4.57        | 5.46  |
| c   | 0.018  | 0.024 | 0.46        | 0.61  |
| c2  | 0.018  | 0.024 | 0.46        | 0.61  |
| D   | 0.235  | 0.245 | 5.97        | 6.22  |
| E   | 0.250  | 0.265 | 6.35        | 6.73  |
| e   | 0.090  | BSC   | 2.29        | BSC   |
| H   | 0.370  | 0.410 | 9.40        | 10.41 |
| L   | 0.055  | 0.070 | 1.40        | 1.78  |
| L1  | 0.114  | REF   | 2.90        | REF   |
| L2  | 0.020  | BSC   | 0.51        | BSC   |
| L3  | 0.035  | 0.050 | 0.89        | 1.27  |
| L4  | ----   | 0.040 | ---         | 1.01  |
| Z   | 0.155  | ----  | 3.93        | ---   |

GENERIC  
MARKING DIAGRAM\*



IC



Discrete

XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

|                                                                       |                                                                       |                                                                  |                                                                            |                                                                   |
|-----------------------------------------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------|----------------------------------------------------------------------------|-------------------------------------------------------------------|
| STYLE 1:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 2:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN          | STYLE 3:<br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | STYLE 4:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE              | STYLE 5:<br>PIN 1. GATE<br>2. ANODE<br>3. CATHODE<br>4. ANODE     |
| STYLE 6:<br>PIN 1. MT1<br>2. MT2<br>3. GATE<br>4. MT2                 | STYLE 7:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 8:<br>PIN 1. N/C<br>2. CATHODE<br>3. ANODE<br>4. CATHODE   | STYLE 9:<br>PIN 1. ANODE<br>2. CATHODE<br>3. RESISTOR ADJUST<br>4. CATHODE | STYLE 10:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE |

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

|                  |                     |                                                                                                                                                                                  |
|------------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98AON10527D         | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | DPAK (SINGLE GAUGE) | PAGE 1 OF 1                                                                                                                                                                      |

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)