

Low-Power, Two-Port, High-Speed, USB2.0 (480 Mbps) Switch

FSUSB43

Description

The FSUSB43 is a bi-directional, low-power, two-port, high-speed, USB2.0 switch. Configured as a double-pole, double-throw (DPDT) switch, it is optimized for switching between two high-speed (480 Mbps) sources or a high-speed and full-speed (12 Mbps) source.

The FSUSB43 is compatible with the requirements of USB2.0 and features an extremely low on capacitance (C_{ON}) of 5.7 pF. The wide bandwidth of this device (720 MHz) exceeds the bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

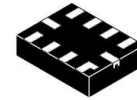
The FSUSB43 contains special circuitry on the switch I/O pins for applications where the V_{CC} supply is powered-off ($V_{CC} = 0$), which allows the device to withstand an over-voltage condition. This minimizes current consumption even when the control voltage applied to the SEL pin is lower than the supply voltage (V_{CC}). This feature is especially valuable to mobile applications, such as cell phones, allowing for direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

Features

- Over-Voltage Tolerance (OVT) on all USB Ports up to 5.25 V without External Components
- Low On Capacitance: 5.7 pF Typical
- Low On Resistance: 3.9 Ω Typical
- Low Power Consumption: 1 μ A Maximum
 - ♦ 20 μ A Maximum ICCT over an Expanded Voltage Range ($V_{IN} = 1.8$ V, $V_{CC} = 4.3$ V)
- Wide -3 db Bandwidth: > 720 MHz
- Packaged in 10-Lead MicroPak™ (1.6 mm x 2.1 mm)
- 8 kV ESD Rating, > 16 kV Power/GND ESD Rating
- Power-Off Protection on All Ports when $V_{CC} = 0$ V
 - ♦ D+/D- Pins Tolerate up to 5.25 V

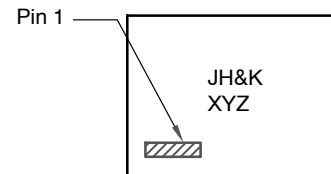
Typical Applications

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box



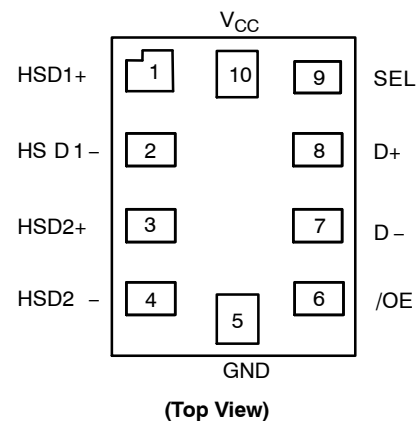
UQFN10 1.6 × 2.1
CASE 523AZ

MARKING DIAGRAM

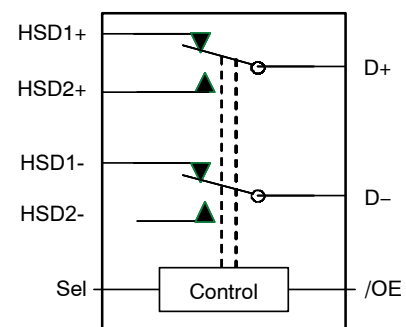


JH = Specific Device Code
 &K = 2 Digit Lot Run Code
 X = Year
 Y = 2 Week Data Code
 Z = Plant Code

PIN CONNECTION



ANALOG SYMBOL



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

FSUSB43

Table 1. PIN DESCRIPTION

Pin #	Name	Description
1	HSD1+	Multiplexed Source Inputs
2	HSD1–	Multiplexed Source Inputs
3	HSD2+	Multiplexed Source Inputs
4	HSD2–	Multiplexed Source Inputs
5	GND	Ground
6	OE	Switch Enable
7	D–	USB Data Bus
8	D+	USB Data Bus
9	SEL	Switch Select
10	V _{CC}	Supply Voltage

Table 2. TRUTH TABLE

SEL	OE	Function
X	HIGH	Disconnect
LOW	LOW	D+, D– = HSD1+, HSD1–
HIGH	LOW	D+, D– = HSD2+, HSD2–

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	–0.5	+5.5	V
V _{CNTRL}	DC Input Voltage (SEL, OE) (Note 1)	–0.5	V _{CC}	V
W _{SW}	ALL PINS for V _{CC} 0 to 5.5 V	–0.5	5.5	V
I _{IK}	DC Input Diode Current	–50		mA
I _{OUT}	DC Output Current		100	mA
T _{STG}	Storage Temperature	–65	+150	°C
ESD	Human Body Model: JEDEC JESD22–A114	All Pins	8	kV
		I/O to GND	9	
		Power to GND	16	
	Charged Device Model: JEDEC JESD22–C101		2	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Table 4. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	2.4	4.4	V
V _{CNTRL}	Control Input Voltage (SEL, OE) (Note 2)	0	V _{CC}	V
V _{SW}	Switch I/O Voltage	–0.5	4.5	V
T _A	Operating Temperature	–40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. The control input must be held HIGH or LOW; it must not float.

Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A (Note 3)			Unit
				Min	Typ	Max	
V _{IK}	Clamp Diode Voltage	I _{IN} = -18 mA	3.0			-1.2	V
V _{IH}	Input Voltage High		2.4 to 3.6	1.3			V
			4.3	1.7			V
V _{IL}	Input Voltage Low		2.4 to 3.6			0.5	V
			4.3			0.7	V
I _{IN}	Control Input Leakage	V _{SW} = 0 V to V _{CC}	4.3	-1.0		1.0	μA
I _{OZ}	Off State Leakage	0 ≤ D _n , HSD1 _n , HSD2 _n ≤ 3.6 V	4.3	-2.0		2.0	μA
I _{OFF}	Power-Off Leakage Current (All I/O Ports)	V _{SW} = 0 V to 4.3 V, V _{CC} = 0 V (Figure 2)	0	-2		2	μA
R _{ON}	HS Switch On Resistance (Note 4)	V _{SW} = 0.4 V, I _{ON} = -8 mA (Figure 1)	2.4		4.5	7.5	Ω
			3.0		3.9	6.5	
R _{ON}	HS Switch On Resistance (Note 4)	V _{SW} = 0.4 V, I _{ON} = -8 mA -40°C to 125°C (Figure 1)	2.4		4.5	9	Ω
			3.0		3.9	8	
ΔR _{ON}	HS Delta R _{ON} (Note 5)	V _{SW} = 0.4 V, I _{ON} = -8 mA	3.0		0.65		Ω
I _Q	Quiescent Supply Current	V _{CNTRL} = 0 or V _{CC} , I _{OUT} = 0	4.3			1.0	μA
I _{CC}	Increase in I _Q Current per Control Voltage and V _{CC}	V _{CNTRL} = 2.6 V, V _{CC} = 4.3 V	4.3			10.0	μA
		V _{CNTRL} = 1.8 V, V _{CC} = 4.3 V	4.3			20.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. All typical values are 25°C, and Min/Max values are -40°C to +85°C unless otherwise specified.

4. Measured by the voltage drop between HSD_n and D_n pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSD_n or D_n ports).

5. Guaranteed by characterization.

Table 6. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A (Note 3)			Unit
				Min	Typ	Max	
t _{ON}	Turn-On Time, SEL, OE to Output	R _L = 50 Ω, C _L = 5 pF, V _{SW} = 0.8 V (Figure 3), (Figure 4)	2.4		24	40	ns
			3.0 to 3.6		13	30	
t _{OFF}	Turn-Off Time, SEL, OE to Output	R _L = 50 Ω, C _L = 5 pF, V _{SW} = 0.8 V (Figure 3), (Figure 4)	2.4		15	35	ns
			3.0 to 3.6		12	25	
t _{PD}	Propagation Delay (Note 6)	R _L = 50 Ω, C _L = 5 pF -40°C to 125°C (Figure 3), (Figure 5)	3.3		0.25		ns
t _{BBM}	Break-Before-Make Time (Note 6)	R _L = 50 Ω, C _L = 5 pF, V _{SW1} = V _{SW2} = 0.8 V (Figure 7)	2.4	2.0		10	ns
			3.0 to 3.6	2.0		6.5	
OIRR	Off Isolation (Note 6)	R _L = 50 Ω, f = 240 Mhz (Figure 9)	3.0 to 3.6		-30		dB
Xtalk	Non-Adjacent Channel Crosstalk (Note 6)	R _L = 50 Ω, f = 240 Mhz (Figure 10)	3.0 to 3.6		-45		dB
BW	-3dB Bandwidth (Note 6)	R _L = 50 Ω, C _L = 0 pF (Figure 8)	3.0 to 3.6		720		MHz
		R _L = 50 Ω, C _L = 5 pF (Figure 8)			550		MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Guaranteed by characterization.

FSUSB43

Table 7. USB HIGH-SPEED-RELATED AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A (Note 3)			Unit
				Min	Typ	Max	
t _{SK(P)}	Skew of Opposite Transitions of the Same Output (Note 7)	R _L = 50 Ω, C _L = 5 pF (Figure 6)	3.0 to 3.6		20		ps
t _J	Total Jitter (Note 7)	R _L = 50 Ω, C _L = 5 pF, t _r = t _f = 500 ps (10–90%) at 480 Mbps (PRBS = 2 ¹⁵ – 1)	3.0 to 3.6		200		ps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by characterization.

Table 8. CAPACITANCE

Symbol	Parameter	Conditions	T _A (Note 3)			Unit
			Min	Typ	Max	
C _{IN}	Control Pin Input Capacitance (Note 8)	V _{CC} = 0 V		1.5		pF
C _{ON}	D+/D– On Capacitance (Note 8)	V _{CC} = 3.3 V, $\overline{OE}$ = 0 V, –40°C to 125°C f = 240 Mhz (Figure 12)		5.5		
C _{OFF}	D1n, D2n Off Capacitance (Note 8)	V _{CC} and $\overline{OE}$ = 3.3 V (Figure 11)		2.0		

8. Guaranteed by characterization.

TEST DIAGRAMS

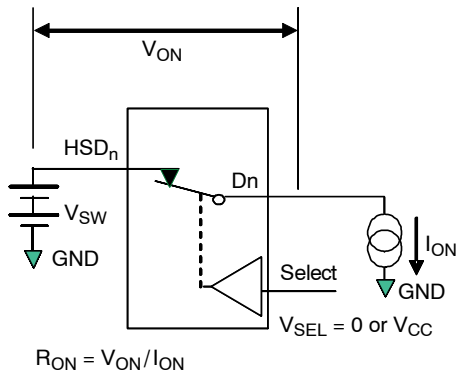
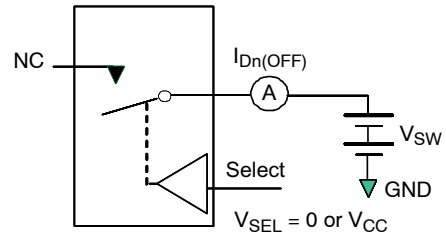
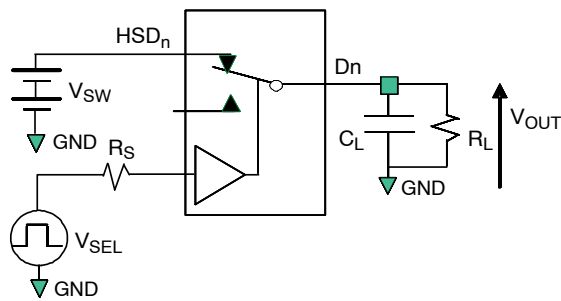


Figure 1. On Resistance



**Each switch port is tested separately

Figure 2. Off Leakage



R_L , R_S , and C_L are functions of the application environment (see AC Tables for specific values)
 C_L includes test fixture and stray capacitance.

Figure 3. AC Test Circuit Load

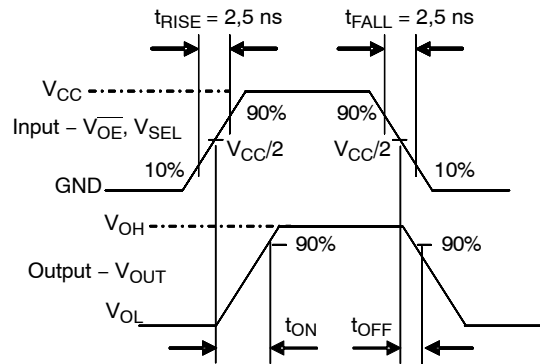


Figure 4. Turn-On / Turn-Off Waveforms

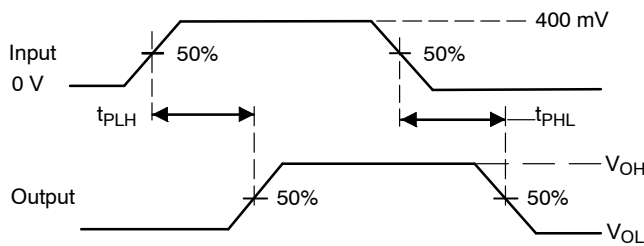


Figure 5. Propagation Delay ($t_R t_F - 500$ ps)

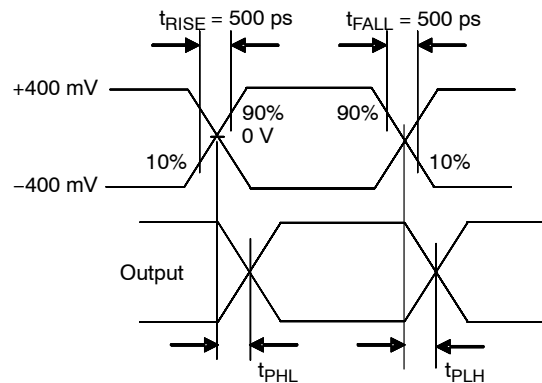


Figure 6. Intra-Pair Skew Test $t_{SK(P)}$

TEST DIAGRAMS (Continued)

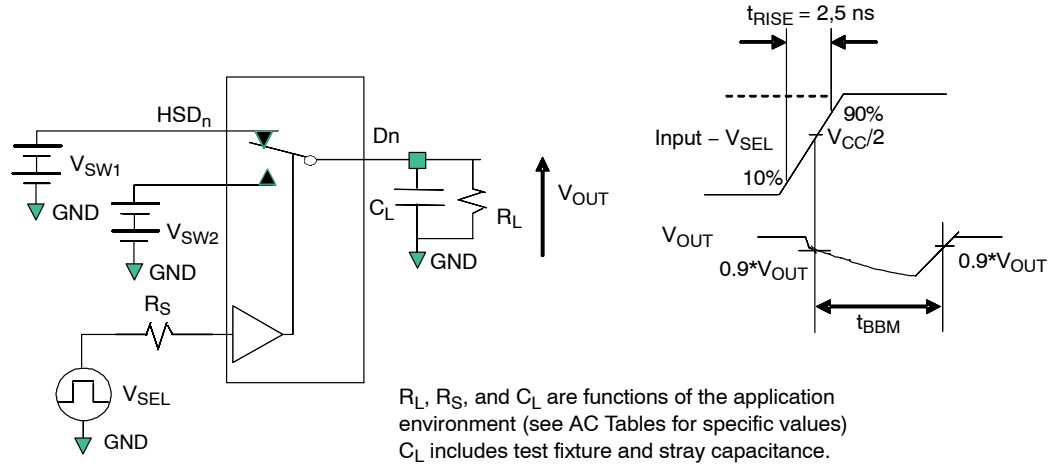


Figure 7. Break-Before-Make Interval Timing

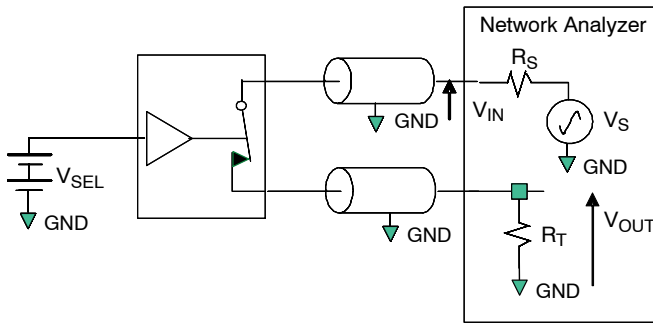
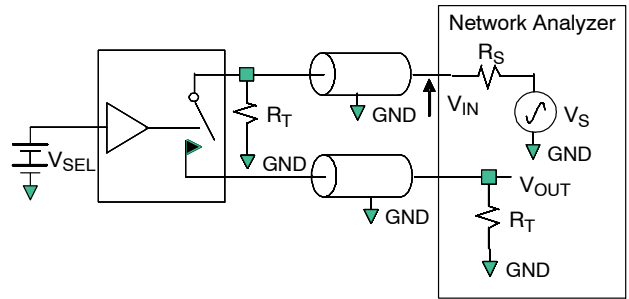


Figure 8. Bandwidth



$$\text{Off isolation} = 20 \log (V_{OUT}/V_{IN})$$

Figure 9. Channel Off Isolation

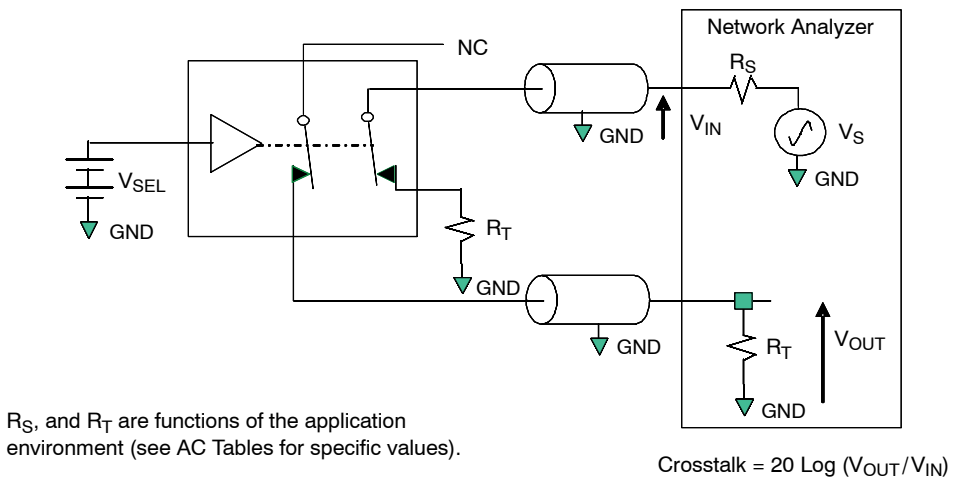


Figure 10. Non-Adjacent Channel-to-Channel Crosstalk

TEST DIAGRAMS (Continued)

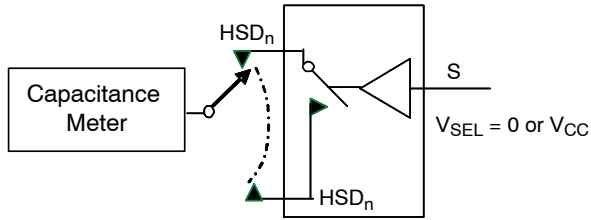


Figure 11. Channel Off Capacitance

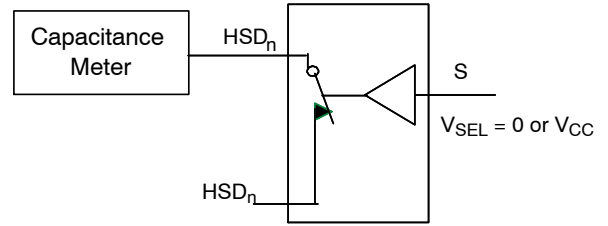
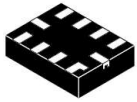


Figure 12. Channel On Capacitance

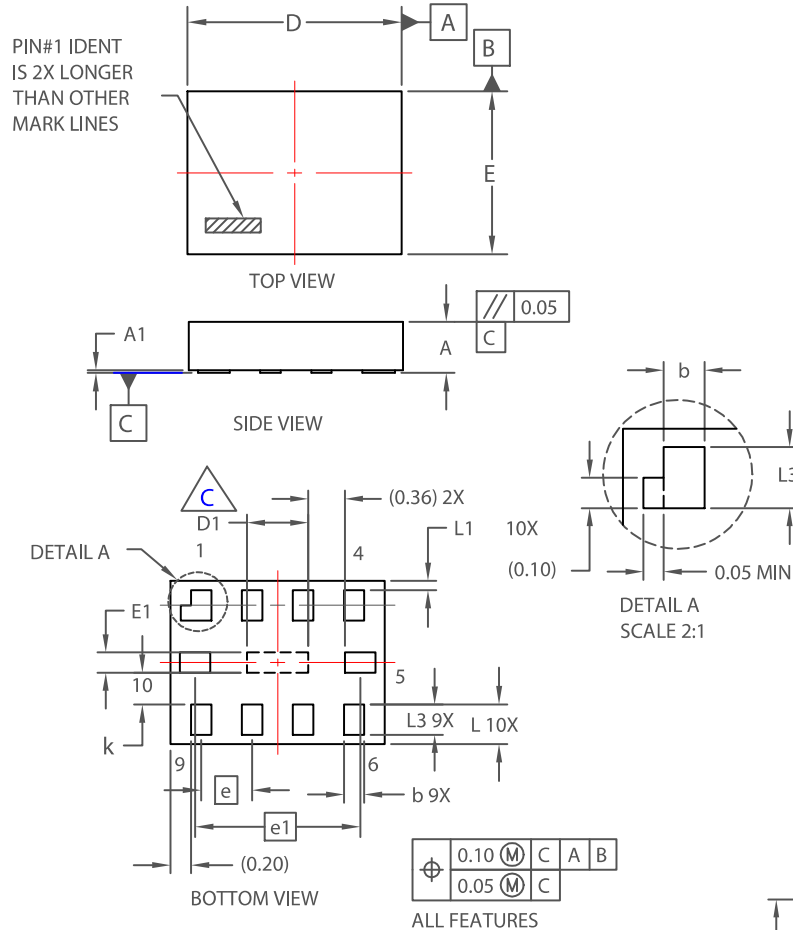
Table 9. ORDERING INFORMATION

Part Number	Device Code	Operating Temperature Range	Package	Shipping [†]
FSUSB43L10X	JH	–40 to 125°C	10-Lead MicroPak (1.6 x 2.1 mm) JEDEC MO–255B	5000 / Tape and Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.


UQFN10 (MICROPAK™), 1.6X2.1, 0.5P
CASE 523AZ
ISSUE A

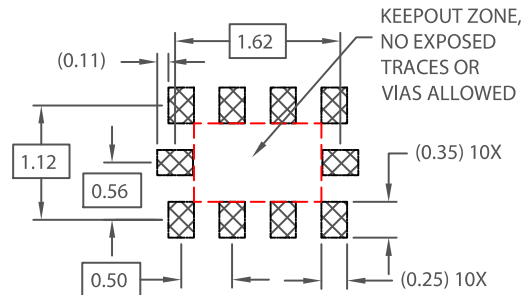
DATE 11 DEC 2019



NOTES:

- A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IT IS NOT INTENDED TO BE SOLDERED AND HAS A BLACK OXIDE FINISH.
- D. DIMENSIONS WITHIN () ARE UNCONTROLLED.

DIM	MIN.	NOM.	MAX.
A	0.50	0.55	0.65
A1	0.00	0.025	0.05
b	0.15	0.20	0.25
D	2.00	2.10	2.20
D1	0.55	0.60	0.65
E	1.50	1.60	1.70
E1	0.15	0.20	0.25
e	0.50 BSC		
e1	1.62 BSC		
k	0.20	--	--
L	0.25	0.30	0.42
L1	0.00	0.09	0.15
L3	0.25	0.30	0.35


**RECOMMENDED
MOUNTING FOOTPRINT ***

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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