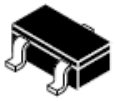
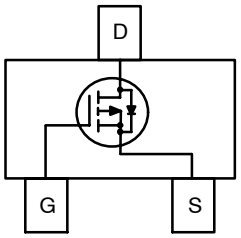
MOSFET – P-Channel, POWERTRENCH®

-150 V, -0.8 A, 1.2 Ω

FDN86265P



SOT−23/SUPERSOT™ −23, 3 LEAD, 1.4x2.9
CASE 527AG



General Description

This P−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been optimized for the on−state resistance and yet maintain superior switching performance.

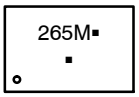
Features

- Max $r_{DS(on)}$ = 1.2 Ω at V_{GS} = −10 V, I_D = −0.8 A
  Max $r_{DS(on)}$ = 1.4 Ω at V_{GS} = −6 V, I_D = −0.7 A
- Very Low RDS−on Mid Voltage P−Channel Silicon Technology Optimised for Low Qg
- This Product is Optimised for Fast Switching Applications as Well as Load Switch Applications
- 100% UIL Tested
- Pb−Free, Halide Free and RoHS Compliant
- HBM ESD Level Class 0B, CDM ESD Level Class C3 (Note 4)

Applications

- Active Clamp Switch
- Load Switch

MARKING DIAGRAM



265 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
FDN86265P	SOT−23 (Pb−Free/ Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	−150	V
V_{GS}	Gate to Source Voltage	±25	V
I_D	Drain Current − Continuous (Note 1a) − Pulsed	 −0.8 −5	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	6	mJ
P_D	Power Dissipation (Note 1a) (Note 1b)	 1.5 0.6	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	80	°C/W

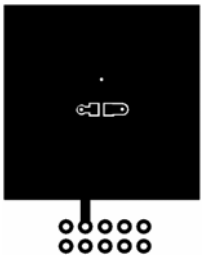
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = –250 μA, V_{GS} = 0 V	–150	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, referenced to 25°C	–	–129	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –120 V, V_{GS} = 0 V	–	–	–1	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±25 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = –250 μA	–2	–3.3	–4	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = –250 μA, referenced to 25°C	–	5	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = –10 V, I_D = –0.8 A V_{GS} = –6 V, I_D = –0.7 A V_{GS} = –10 V, I_D = –0.8 A, T_J = 125°C	– – –	0.85 0.96 1.54	1.2 1.4 2.2	Ω
g_{FS}	Forward Transconductance	V_{DS} = –10 V, I_D = –0.8 A	–	1.5	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = –75 V, V_{GS} = 0 V, f = 1 MHz	–	158	210	pF
C_{oss}	Output Capacitance		–	17	25	pF
C_{rss}	Reverse Transfer Capacitance		–	1.6	5	pF
R_g	Gate Resistance		0.1	3.3	6.7	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –75 V, I_D = –0.8 A, V_{GS} = –10 V, R_{GEN} = 6 Ω	–	5.7	12	ns
t_r	Rise Time		–	2.2	10	ns
$t_{d(off)}$	Turn–Off Delay Time		–	7.9	16	ns
t_f	Fall Time		–	9.9	20	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to –10 V, V_{DD} = –75 V, I_D = –0.8 A,	–	2.9	4.1	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = –75 V, I_D = –0.8 A	–	0.8	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	0.8	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = –0.8 A (Note 2)	–	–0.86	–1.3	V
t_{rr}	Reverse Recovery Time	I_F = –0.8 A, di/dt = 100 A/μs	–	49	78	ns
Q_{rr}	Reverse Recovery Charge		–	70	112	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a) 80°C/W when mounted on a 1 in^2 pad of 2 oz. copper.

b) 180°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.
3. Starting T_J = 25°C; N–ch: L = 3 mH, I_{AS} = –2 A, V_{DD} = –150 V, V_{GS} = –10 V. 100% test at L = 0.1 mH, I_{AS} = –9 A.
4. ESD between the gate and source serves only, no gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

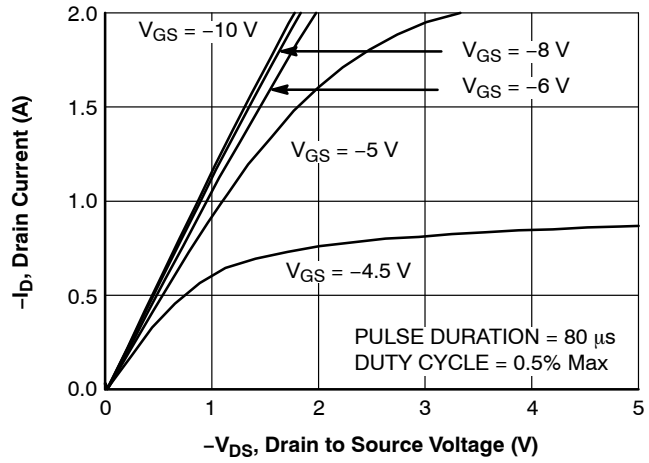


Figure 1. On Region Characteristics

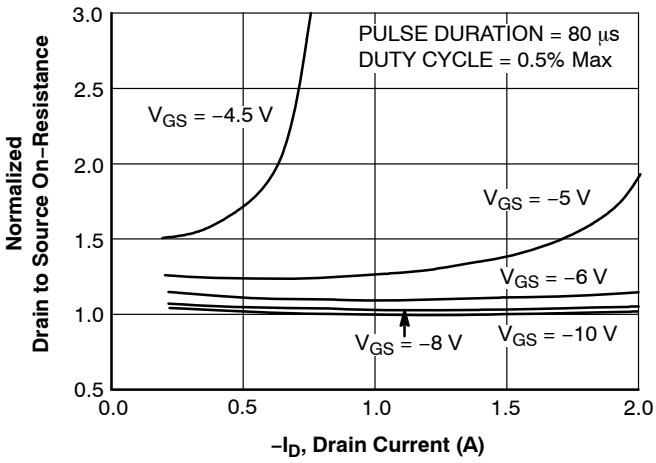


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

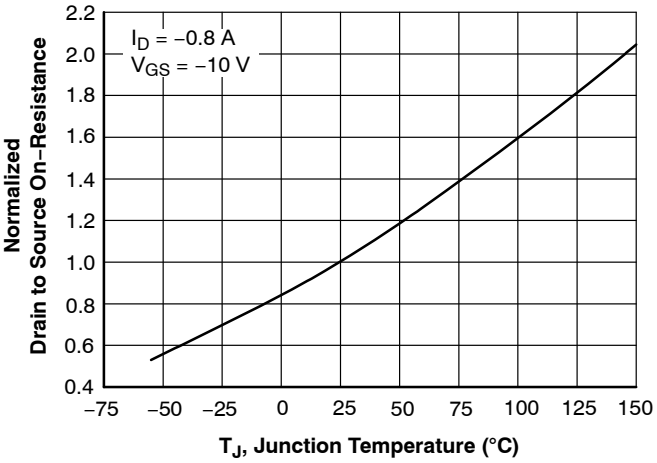


Figure 3. Normalized On Resistance vs. Junction Temperature

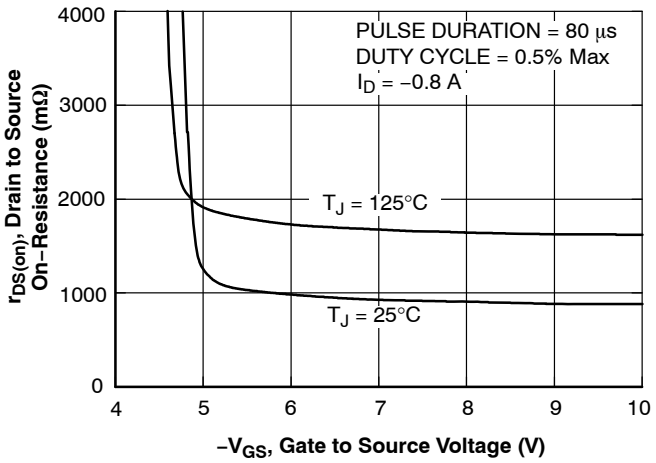


Figure 4. On−Resistance vs. Gate to Source Voltage

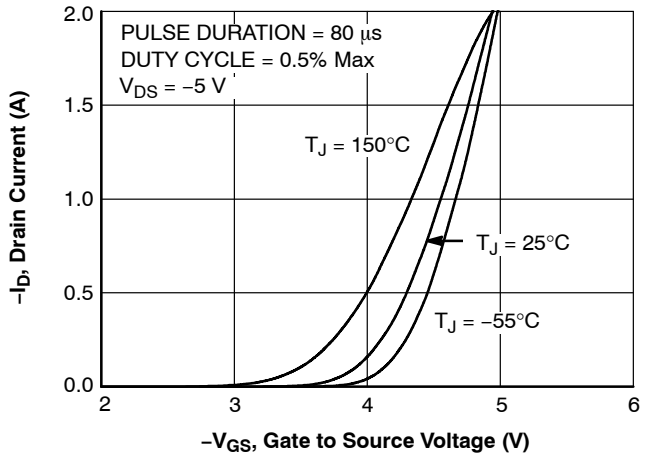


Figure 5. Transfer Characteristics

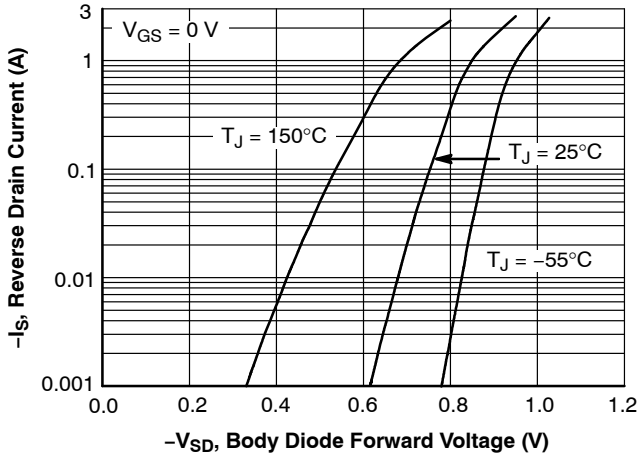


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (CONTINUED)

(T_J = 25°C unless otherwise noted)

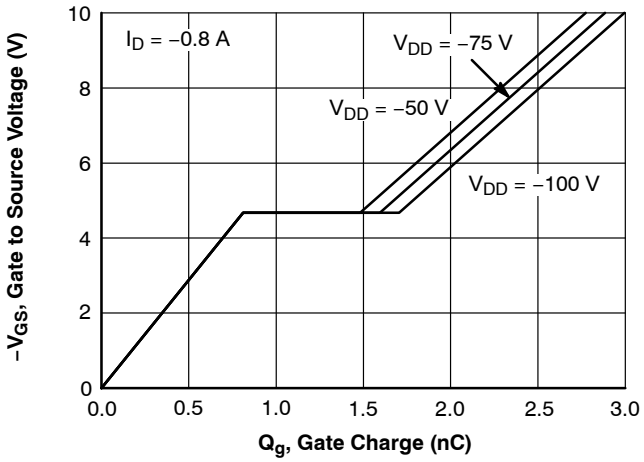


Figure 7. Gate Charge Characteristics

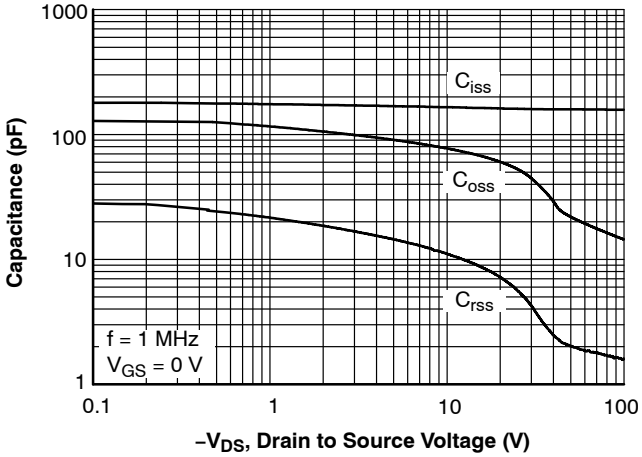


Figure 8. Capacitance vs. Drain to Source Voltage

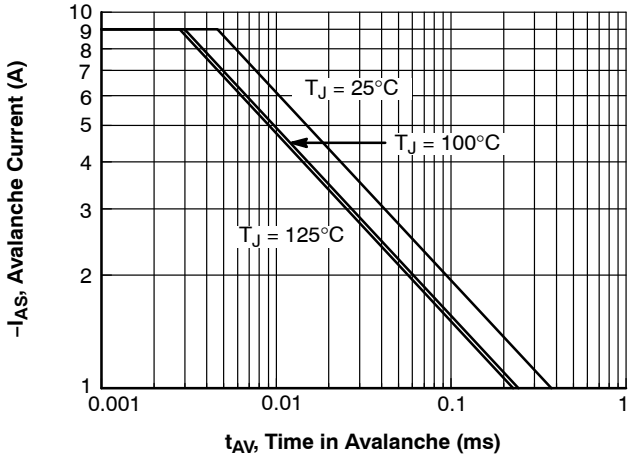


Figure 9. Unclamped Inductive Switching Capability

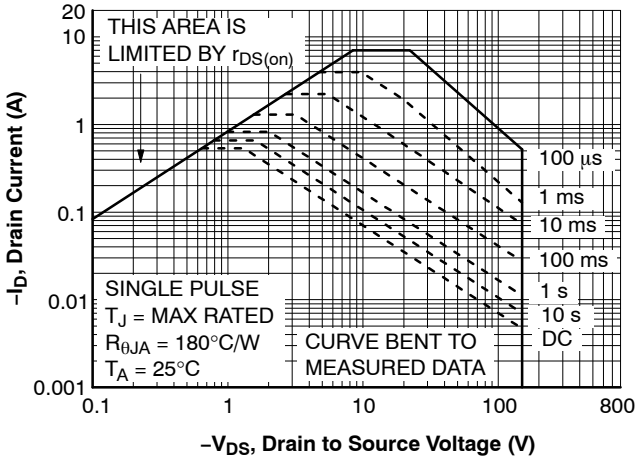


Figure 10. Forward Bias Safe Operating Area

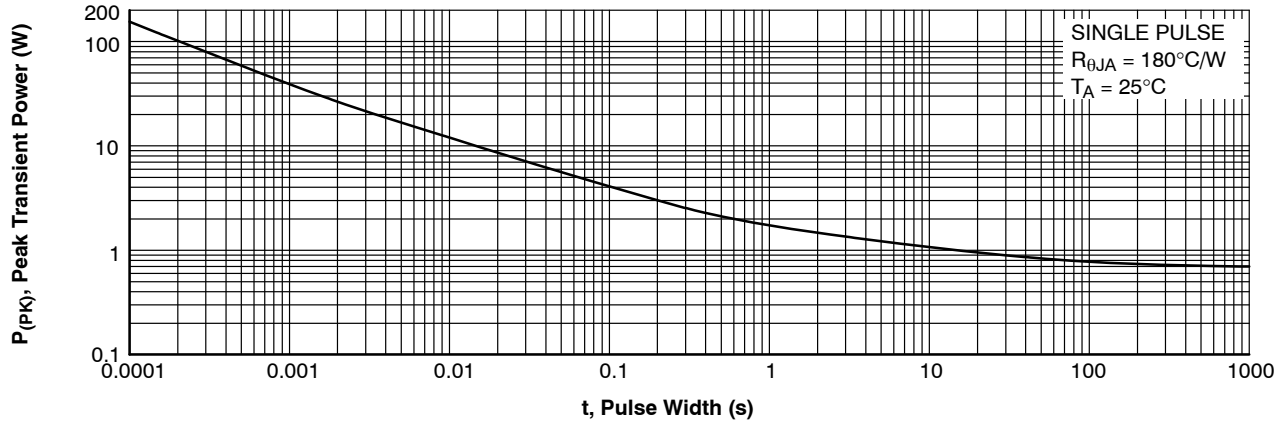


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED)

(T_J = 25°C unless otherwise noted)

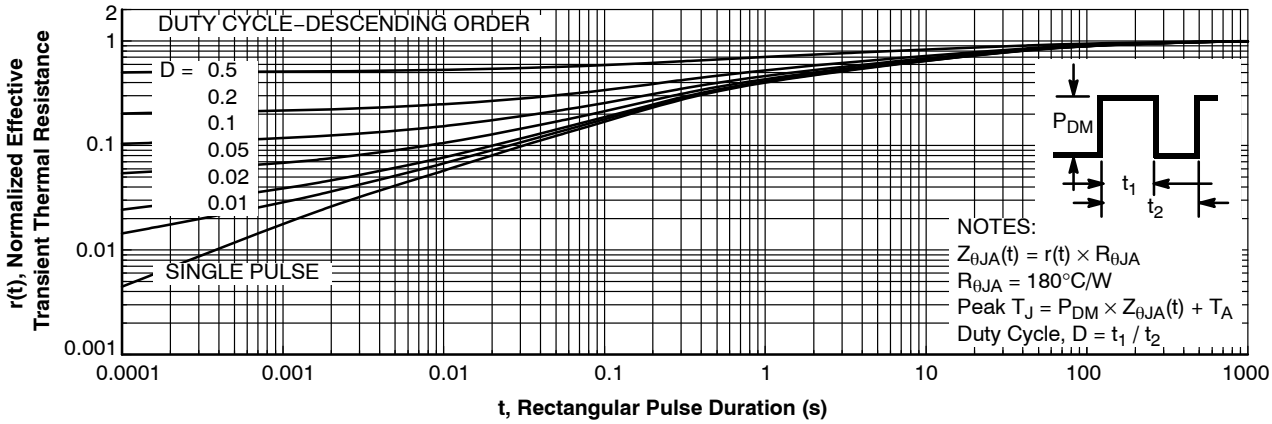
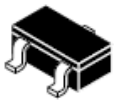
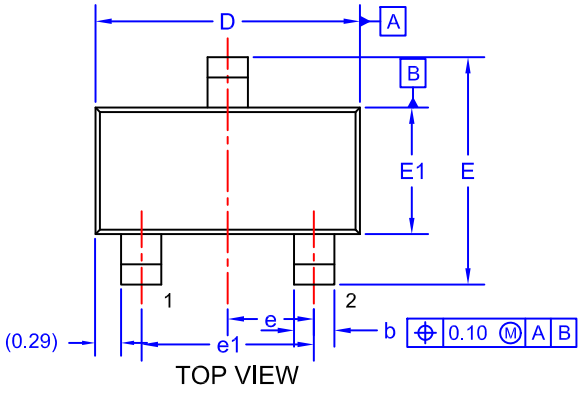


Figure 12. Junction−to−Ambient Transient Thermal Response Curve



SOT−23/SUPERSOT™ −23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019

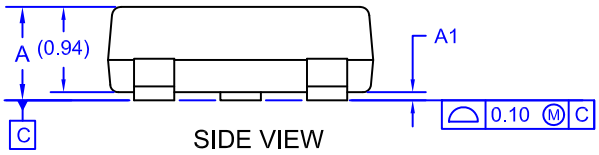


TOP VIEW

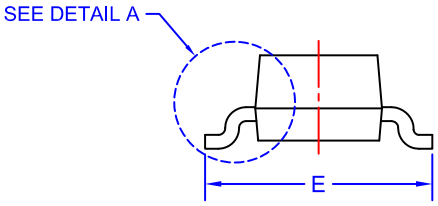
NOTES: UNLESS OTHERWISE SPECIFIED

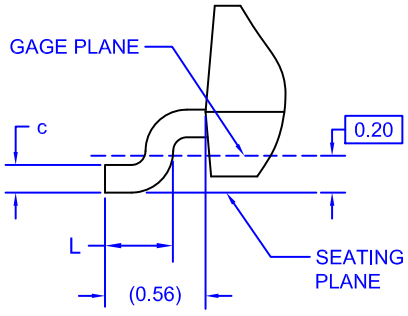
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43

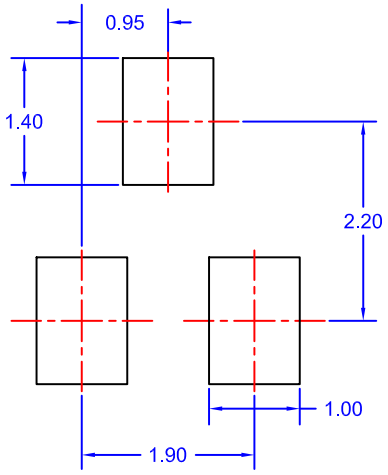


SIDE VIEW





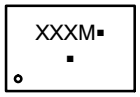
DETAIL A



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOT−23/SUPERSOT−23, 3 LEAD, 1.4X2.9**	**PAGE 1 OF 1**

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