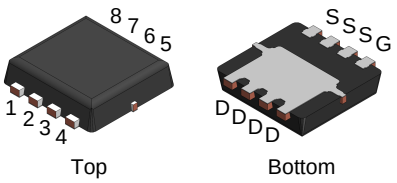
MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

100 V, 16 A, 56 mΩ

FDMC8622

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
100 V	56 mΩ @ 10 V	16 A
	90 mΩ @ 6 V	



Top Bottom

WDFN8 3.3x3.3, 0.65P
(MLP 3.3x3.3)
CASE 511DR

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

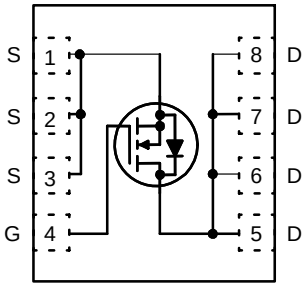
Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 56 mΩ at V_{GS} = 10 V, I_D = 4 A
- Max $r_{DS(on)}$ = 90 mΩ at V_{GS} = 6 V, I_D = 3 A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- 100% UIL Tested
- This Device is Pb−Free and is ROHS Compliant

MARKING DIAGRAM

$Y	= Logo
&Z	= Assembly Plant Code
&2	= 2−Digit Date Code Format
&K	= 2−Digits Lot Run Traceability Code
FDMC8622	= Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter			Ratings	Unit
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current	Continuous	T_C = 25°C	16	A
		Continuous (Note 3a)	T_A = 25°C	4	
		Pulsed (Note 2)		30	
E_{AS}	Single Pulse Avalanche Energy (Note 1)			37	mJ
P_D	Power Dissipation		T_C = 25°C	31	W
	Power Dissipation (Note 3a)		T_A = 25°C	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to +150	°C

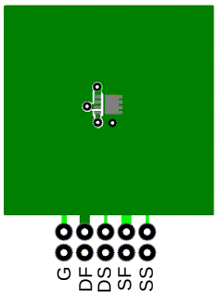
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting T_J = 25°C; N−ch: L = 3.0 mH, I_{AS} = 5.0 A, V_{DD} = 100 V, V_{GS} = 10 V.
2. Pulse Id refers to Figure 11. Forward Bias Safe Operation Area.

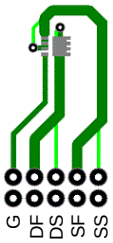
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 3)	4.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3a)	53	

3. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined bythe user's board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	69	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	2.9	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	−9	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 4 A	–	43.7	56	mΩ
		V_{GS} = 6 V, I_D = 3 A	–	59.9	90	
		V_{GS} = 10 V, I_D = 4 A, T_J = 125°C	–	76.4	98	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4 A	–	8.9	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	302	402	pF
C_{oss}	Output Capacitance		–	72.5	96	pF
C_{rss}	Reverse Transfer Capacitance		–	4.2	6	pF
R_g	Gate Resistance		–	1.0	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 4 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	5.9	12	ns
t_r	Rise Time		–	1.6	10	ns
$t_{d(off)}$	Turn−Off Delay Time		–	10.2	18	ns
t_f	Fall Time		–	2.2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 4 A	–	5.2	7.3	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 5 V, V_{DD} = 50 V, I_D = 4 A	–	3.0	4.1	nC
Q_{gs}	Total Gate Charge	V_{DD} = 50 V, I_D = 4 A	–	1.4	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	1.4	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 4 A (Note 4)	–	0.8	1.3	V
		V_{GS} = 0 V, I_S = 1.7 A (Note 4)	–	0.8	1.2	
t_{rr}	Reverse Recovery Time	I_F = 4 A, di/dt = 100 A/μs	–	36	57	ns
Q_{rr}	Reverse Recovery Charge		–	28	45	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

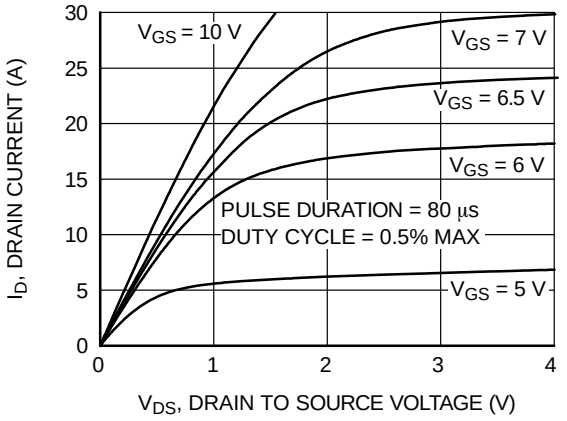


Figure 1. On Region Characteristics

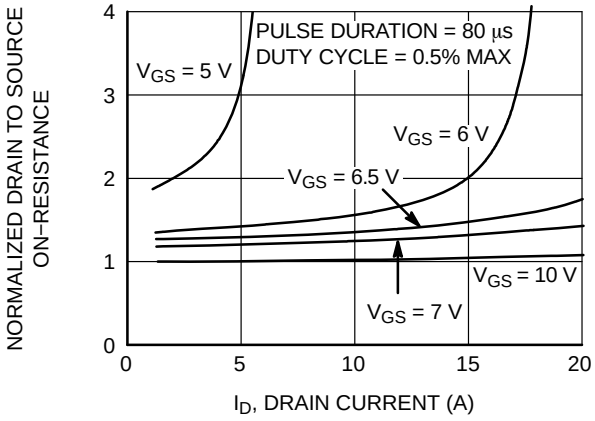


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

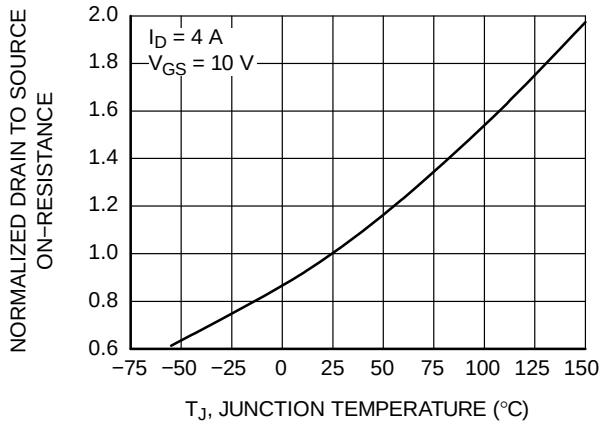


Figure 3. Normalized On−Resistance vs. Junction Temperature

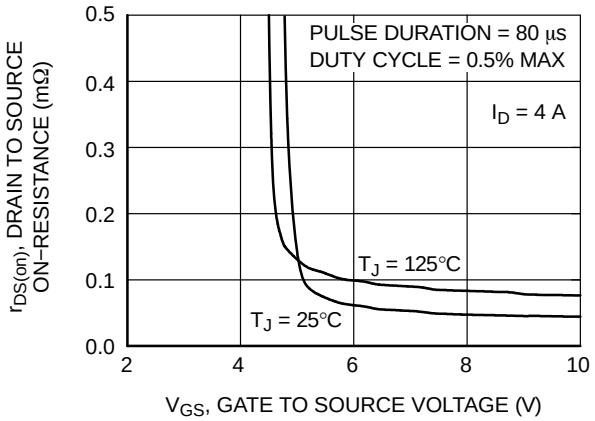


Figure 4. On−Resistance vs. Gate to Source Voltage

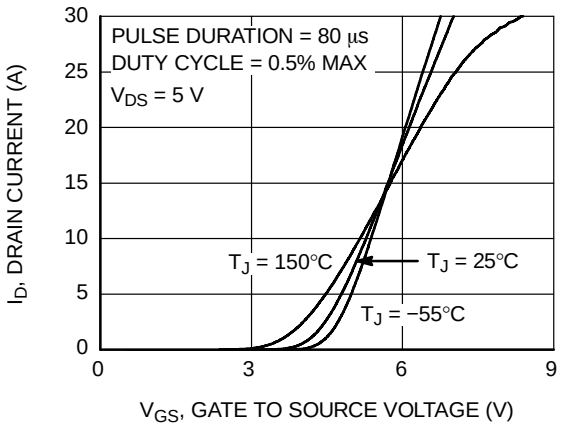


Figure 5. Transfer Characteristics

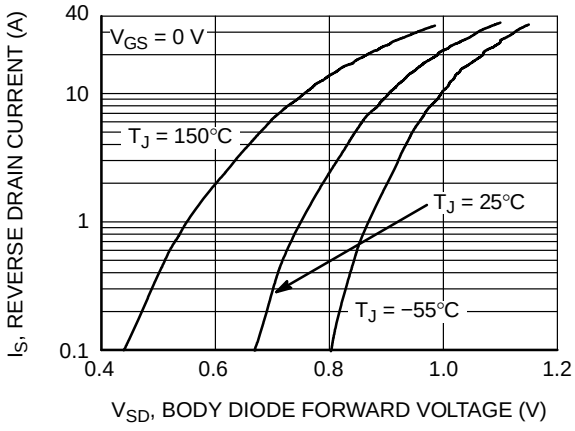


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

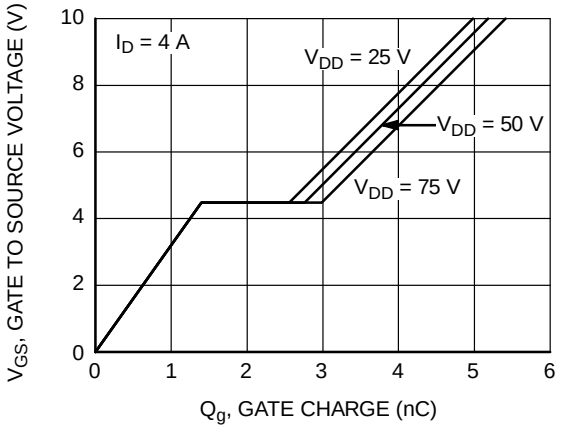


Figure 7. Gate Charge Characteristics

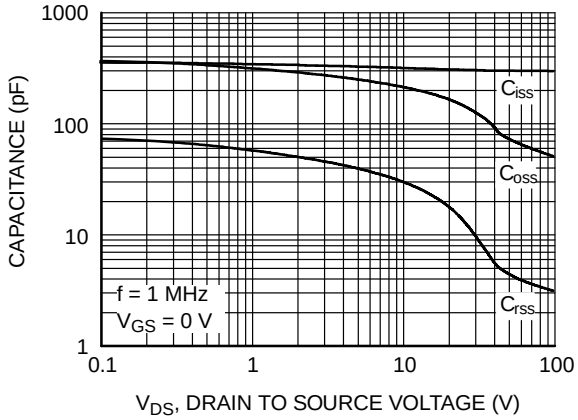


Figure 8. Capacitance vs. Drain to Source Voltage

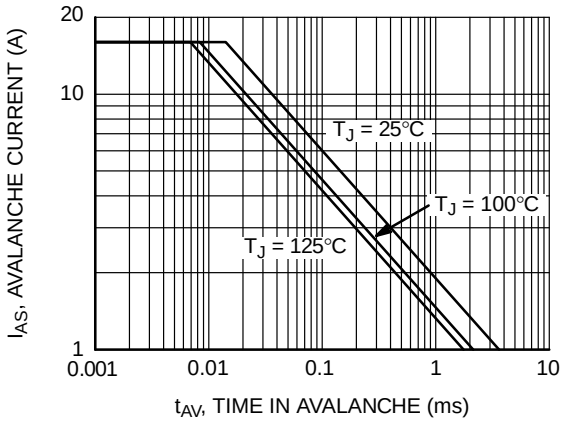


Figure 9. Unclamped Inductive Switching Capability

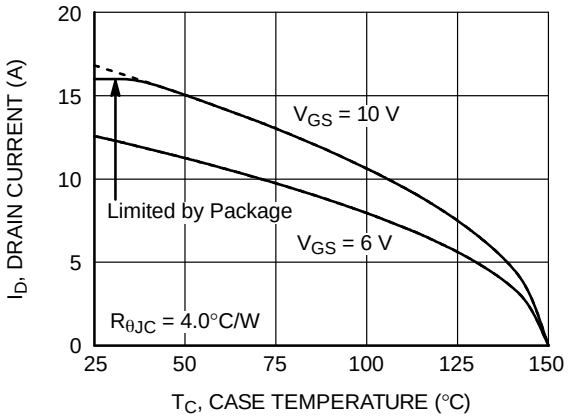


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

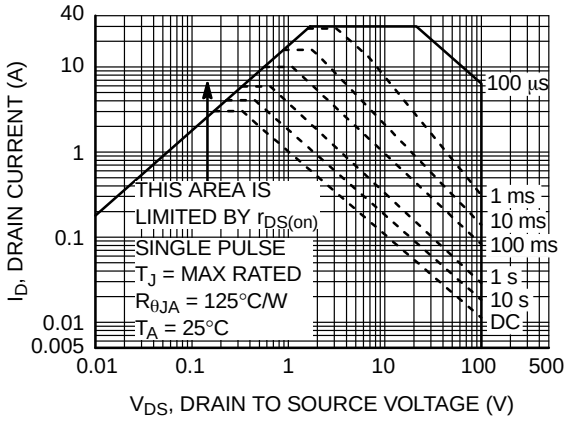


Figure 11. Forward Bias Safe Operating Area

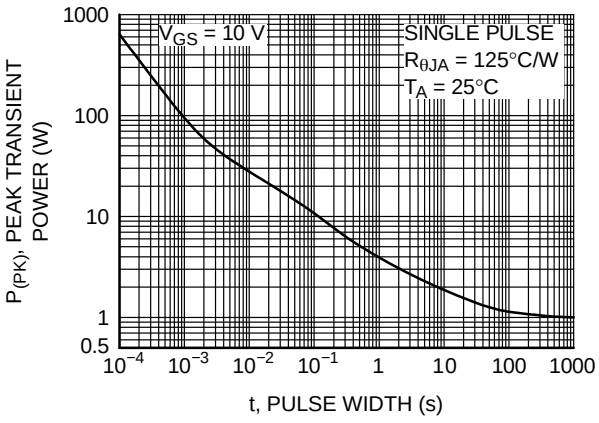


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

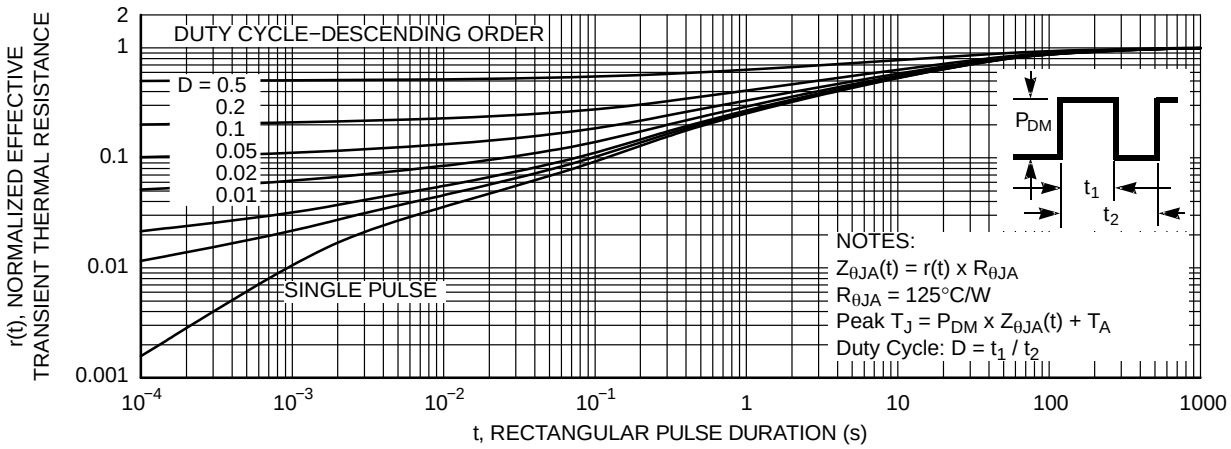


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDMC8622	FDMC8622	WDFN8 3.3x3.3, 0.65P (MLP 3.3x3.3) (Pb−Free)	13”	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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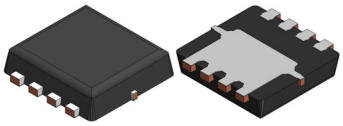
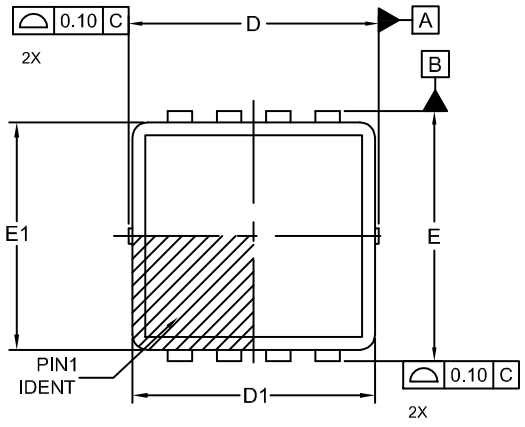
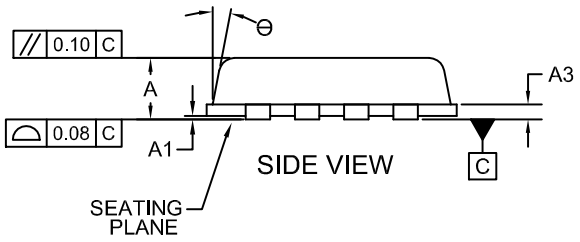


WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE B

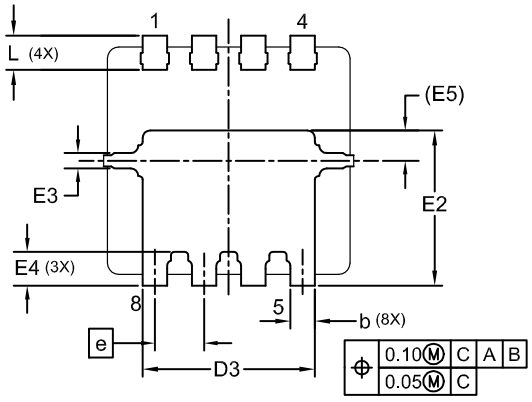
DATE 02 FEB 2022



TOP VIEW



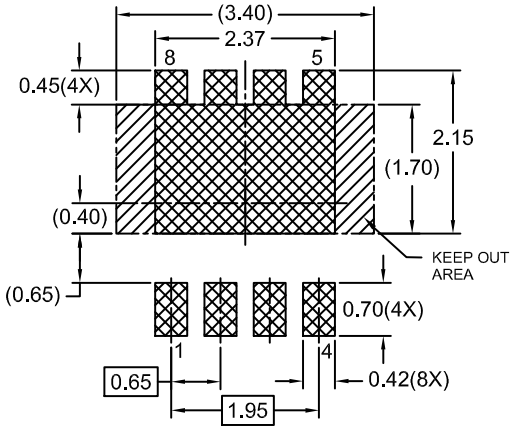
SIDE VIEW



BOTTOM VIEW

NOTES:
A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
E4	0.30	0.40	0.50
E5	0.40 REF		
e	0.65 BSC		
L	0.30	0.40	0.50
θ	0°	-	12°



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13650G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WDFN8 3.3x3.3, 0.65P**	**PAGE 1 OF 1**

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