

MOSFET – Single, P-Channel, POWERTRENCH®

-20 V, -9.4 A, 20 mΩ

FDMA910PZ

General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance and zener diode protection against ESD. The MicroFET™ 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- Max $r_{DS(on)}$ = 20 mΩ at $V_{GS} = -4.5$ V, $I_D = -9.4$ A
- Max $r_{DS(on)}$ = 24 mΩ at $V_{GS} = -2.5$ V, $I_D = -8.6$ A
- Max $r_{DS(on)}$ = 34 mΩ at $V_{GS} = -1.8$ V, $I_D = -7.2$ A
- Low Profile – 0.8 mm Maximum in the New Package MicroFET 2x2 mm
- HBM ESD Protection Level > 2.8 kV Typical (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb-Free, Halide Free and is RoHS Compliant

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

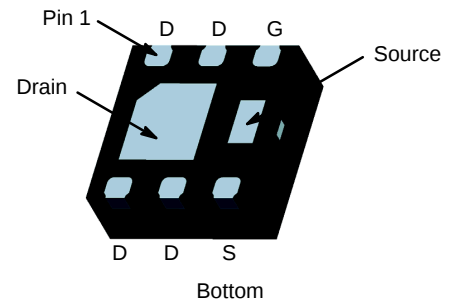
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	- Continuous $T_A = 25^\circ\text{C}$ (Note 1a) - Pulsed	-9.4 -45	A
P_D	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a) $T_A = 25^\circ\text{C}$ (Note 1b)	2.4 0.9	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

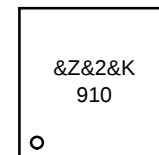
THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
-20 V	20 mΩ @ -4.5 V	-9.4 A
	24 mΩ @ -2.5 V	
	34 mΩ @ -1.8 V	

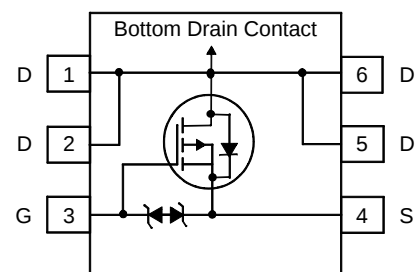


MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = 2-Digit Date Code
&K = 2-Digits Lot Run Traceability Code
910 = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDMA910PZ

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	-12	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -16 V, V _{GS} = 0 V	-	-	-1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±8 V, V _{DS} = 0 V	-	-	±1	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-0.4	-0.5	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	3	-	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = -4.5 V, I _D = -9.4 A	-	16	20	mΩ
		V _{GS} = -2.5 V, I _D = -8.6 A	-	19	24	
		V _{GS} = -1.8 V, I _D = -7.2 A	-	24	34	
		V _{GS} = -4.5 V, I _D = -9.4 A, T _J = 125°C	-	20	25	
g _{FS}	Forward Transconductance	V _{DD} = -5 V, I _D = -9.4 A	-	52	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	-	2110	2805	pF
C _{oss}	Output Capacitance		-	414	620	pF
C _{rss}	Reverse Transfer Capacitance		-	388	580	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = -10 V, I _D = -9.4 A, V _{GS} = -4.5 V, R _{GEN} = 6 Ω	-	9.4	19	ns
t _r	Rise Time		-	19	34	ns
t _{d(off)}	Turn-Off Delay Time		-	135	216	ns
t _f	Fall Time		-	103	165	ns
Q _g	Total Gate Charge	V _{GS} = -4.5 V, V _{DD} = -10 V, I _D = -9.4 A	-	21	29	nC
Q _{gs}	Gate to Source Charge		-	2.5	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	6	-	nC

DRAIN-SOURCE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -2 A (Note 2)	-	-0.6	-1.2	V
		V _{GS} = 0 V, I _S = -9.4 A (Note 2)	-	-0.8	-1.2	V
t _{rr}	Reverse Recovery Time	I _F = -9.4 A, di/dt = 100 A/μs	-	23	37	ns
Q _{rr}	Reverse Recovery Charge		-	6.3	13	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θJA} is determined by the user's board design.



a. 52°C/W when mounted on a
1 in² pad of 2 oz copper



b. 145°C/W when mounted on a
minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

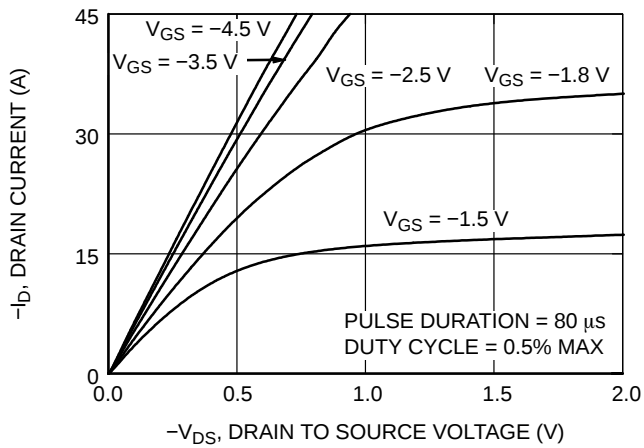
TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Figure 1. On-Region Characteristics

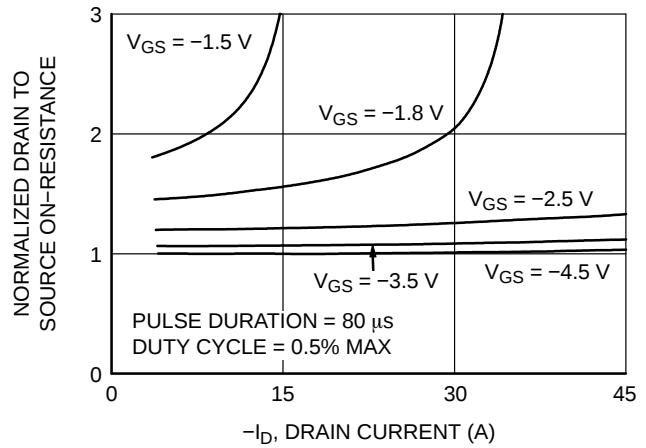


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

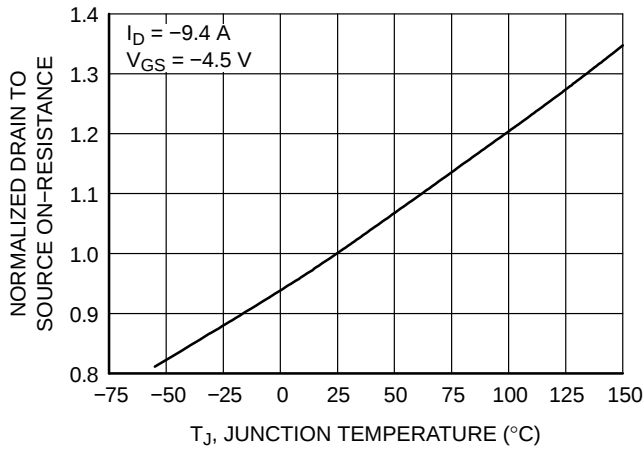


Figure 3. Normalized On-Resistance vs. Junction Temperature

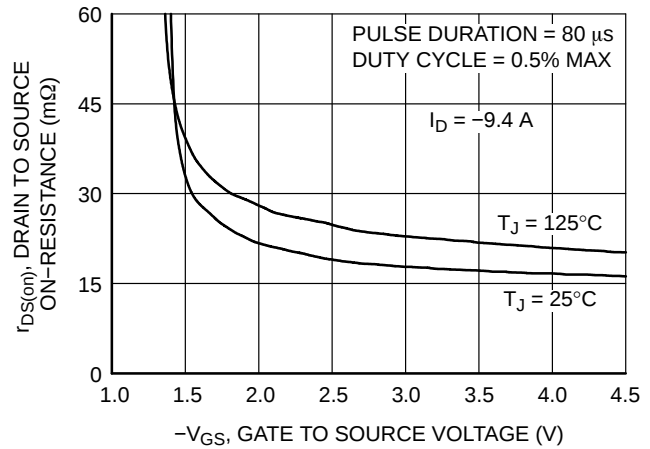


Figure 4. On-Resistance vs. Gate to Source Voltage

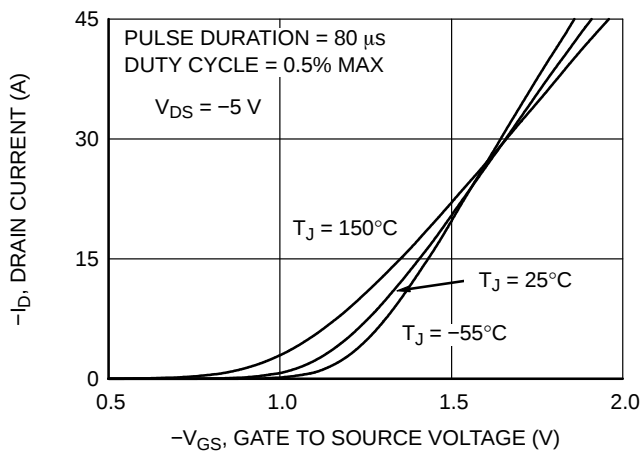


Figure 5. Transfer Characteristics

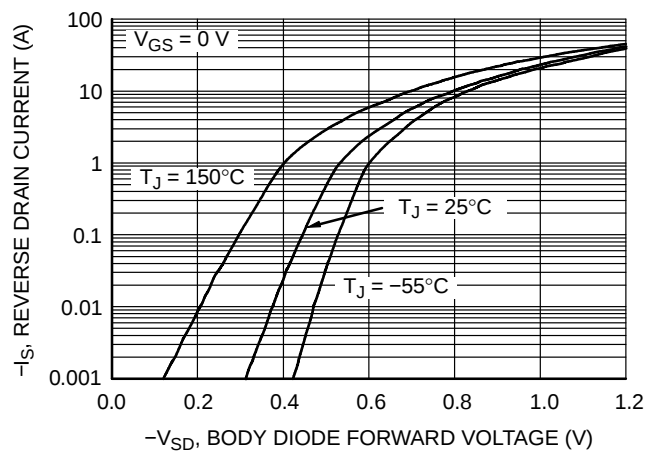


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

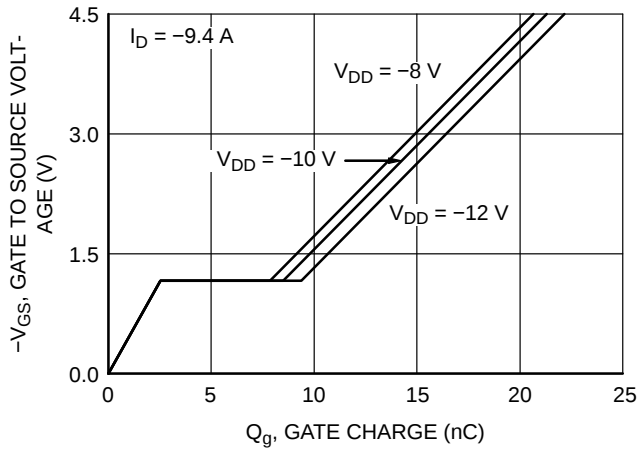


Figure 7. Gate Charge Characteristics

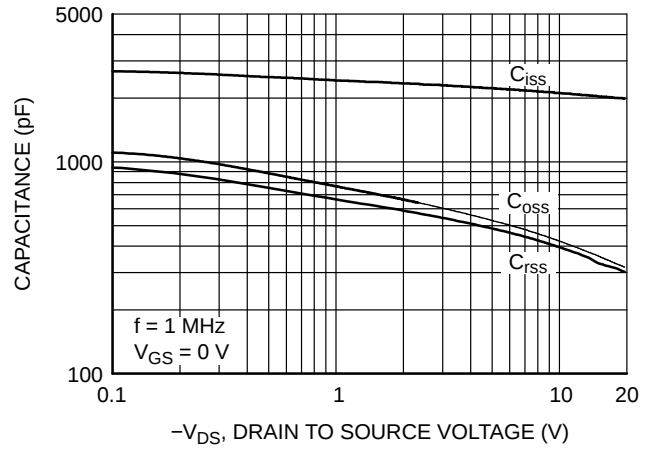


Figure 8. Capacitance vs. Drain to Source Voltage

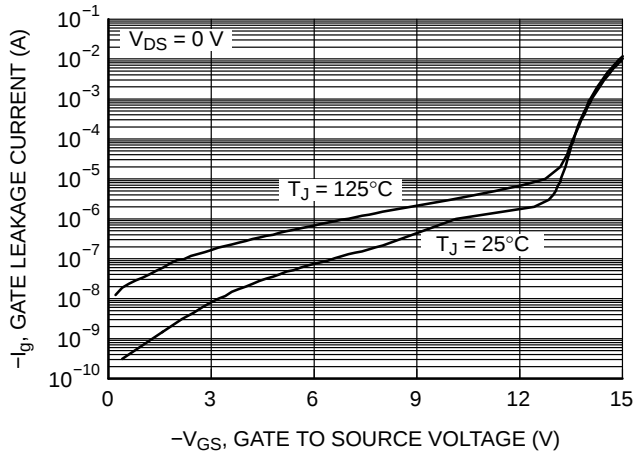


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

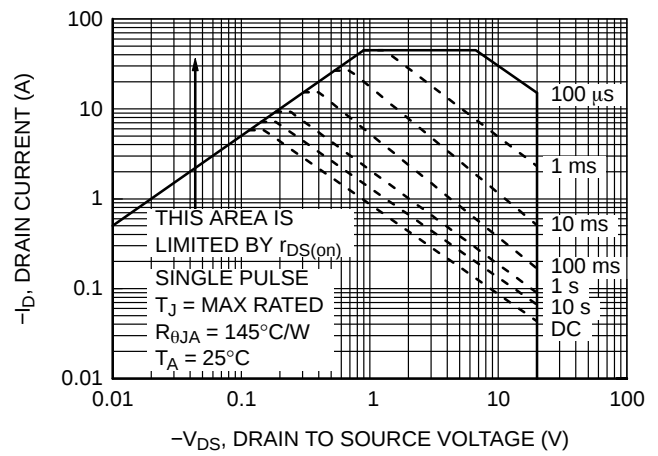


Figure 10. Forward Bias Safe Operating Area

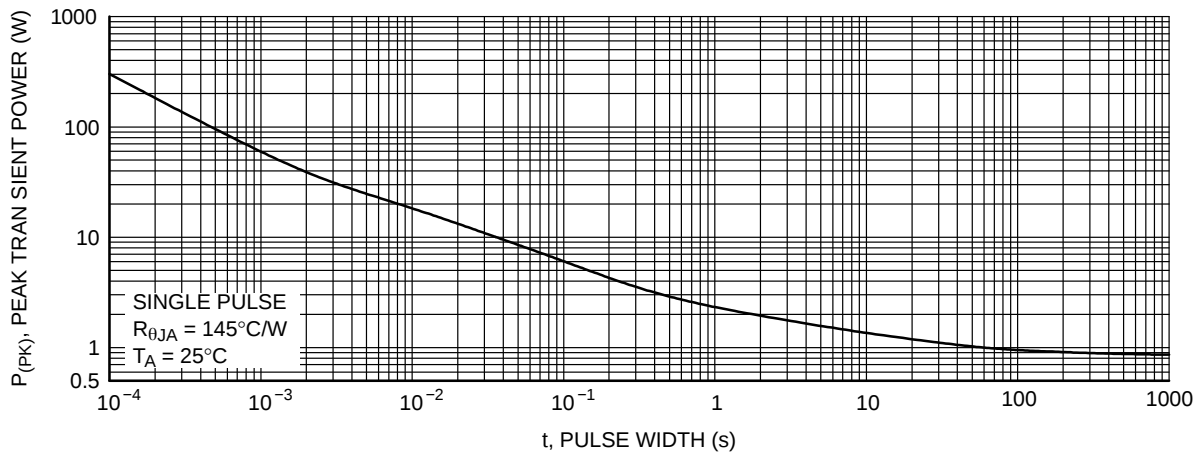


Figure 11. Single Pulse Maximum Power Dissipation

FDMA910PZ

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

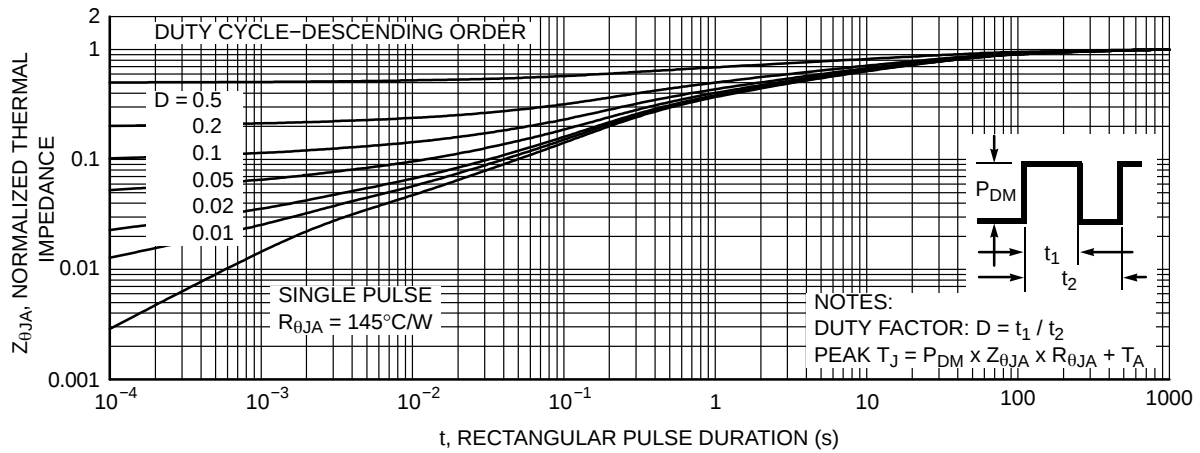


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDMA910PZ	910	WDFN6 2x2, 0.65P (MicroFET 2x2) (Pb-Free, Halide Free)	7"	8 mm	3000 / Tape & Reel

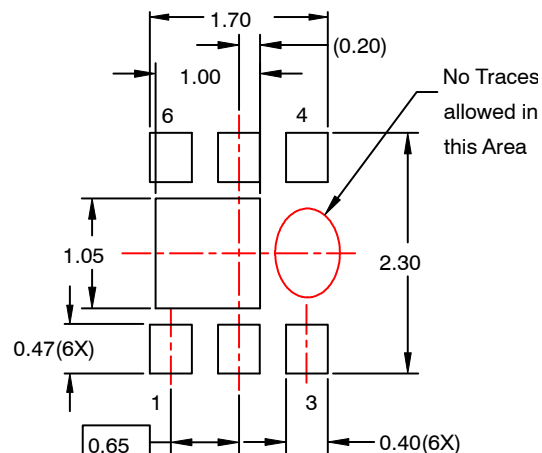
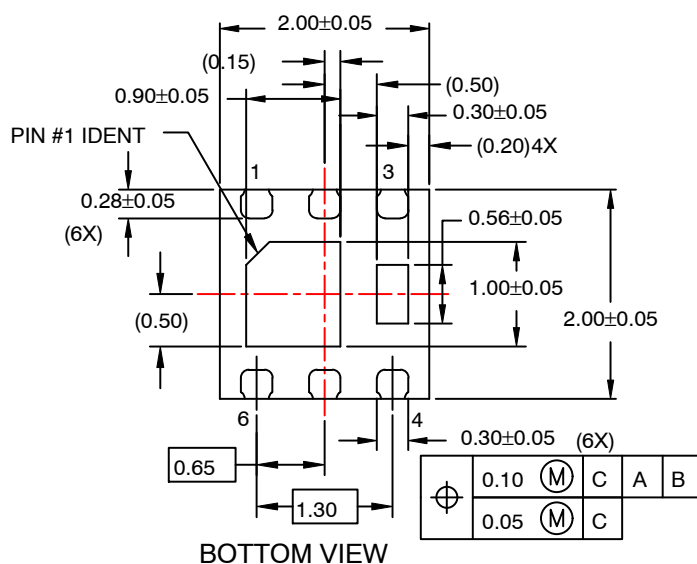
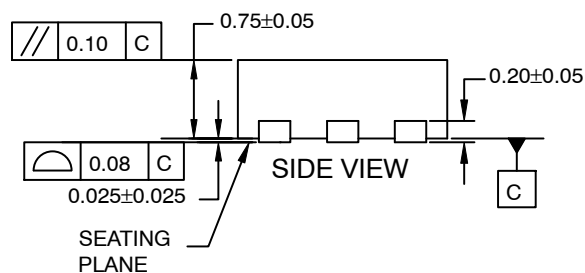
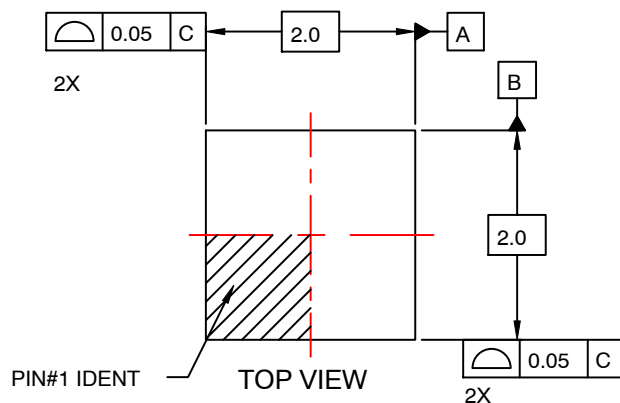
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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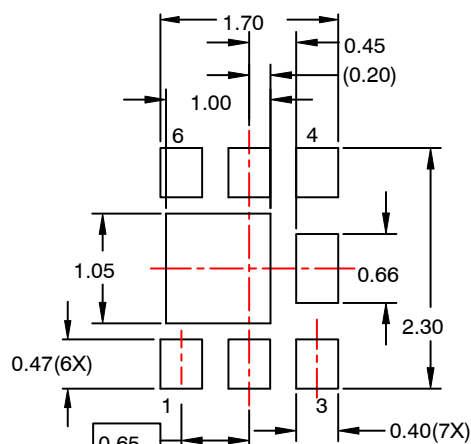
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WDFN6 2x2, 0.65P
CASE 511CZ
ISSUE O

DATE 31 JUL 2016



RECOMMENDED
LAND PATTERN OPT 1



RECOMMENDED
LAND PATTERN OPT 2

NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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