



PESD5V0U1UB

Ultra low capacitance unidirectional ESD protection diodes

6 August 2026

Product data sheet

1. General description

Ultra low capacitance unidirectional ElectroStatic Discharge (ESD) protection diodes in small Surface-Mounted Device (SMD) plastic packages designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Unidirectional ESD protection of one line
- Ultra low diode capacitance: $C_d = 2 \text{ pF}$
- Very low leakage current: $I_{RM} = 1 \text{ nA}$
- ESD protection up to 9 kV
- IEC 61000-4-2; level 4 (ESD)

3. Applications

- USB interfaces
- 10/100/1000 Mbit/s Ethernet
- FireWire
- High-speed data lines
- Subscriber Identity Module (SIM) card protection
- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals
- Audio and video equipment

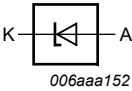
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25 \text{ }^{\circ}\text{C}$	-	-	5	V
C_d	diode capacitance	$f = 1 \text{ MHz}; V_R = 0 \text{ V}; T_{amb} = 25 \text{ }^{\circ}\text{C}$	-	2	2.6	pF
		$f = 1 \text{ MHz}; V_R = 5 \text{ V}; T_{amb} = 25 \text{ }^{\circ}\text{C}$	-	1.7	2.3	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode 1[1]	 SC-79 (SOD523)	 006aaa152
2	A	anode		

[1] The marking bar indicates the cathode.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0U1UB	SC-79	plastic, surface-mounted package; 2 leads; 1.2 mm x 0.8 mm x 0.6 mm body	SOD523

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0U1UB	LÄ

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1] [2]	-	9	kV
		MIL-STD-883 (human body model)		-	10	kV

- [1] Device stressed with ten non-repetitive ESD pulses.
[2] Measured from pin 1 to pin 2.

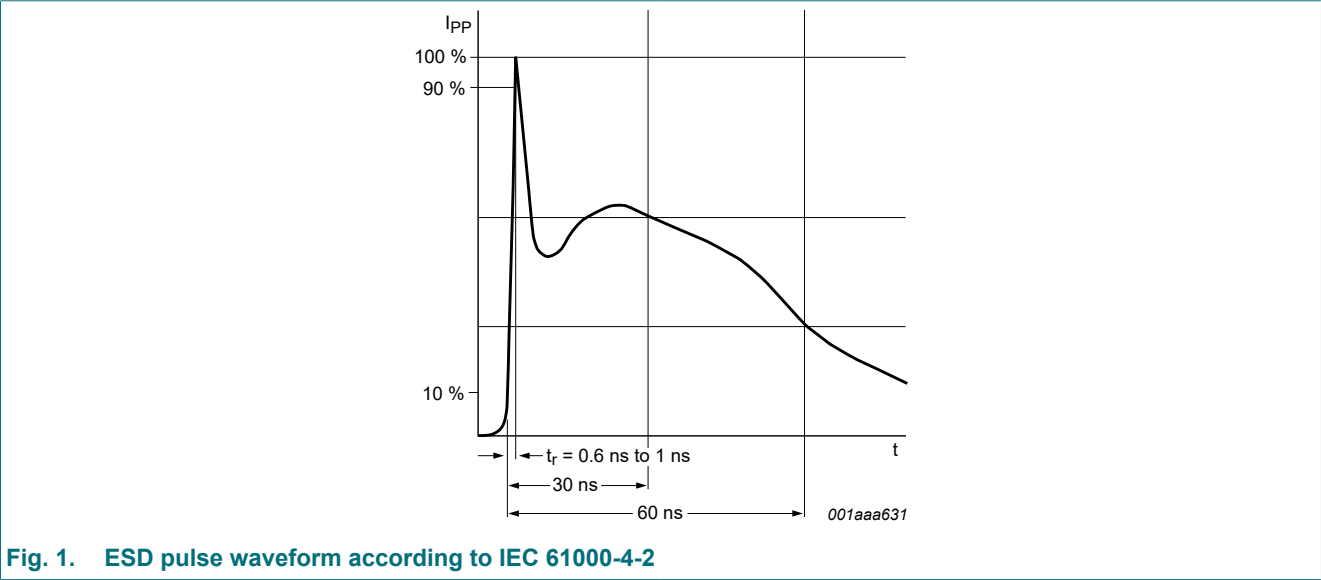
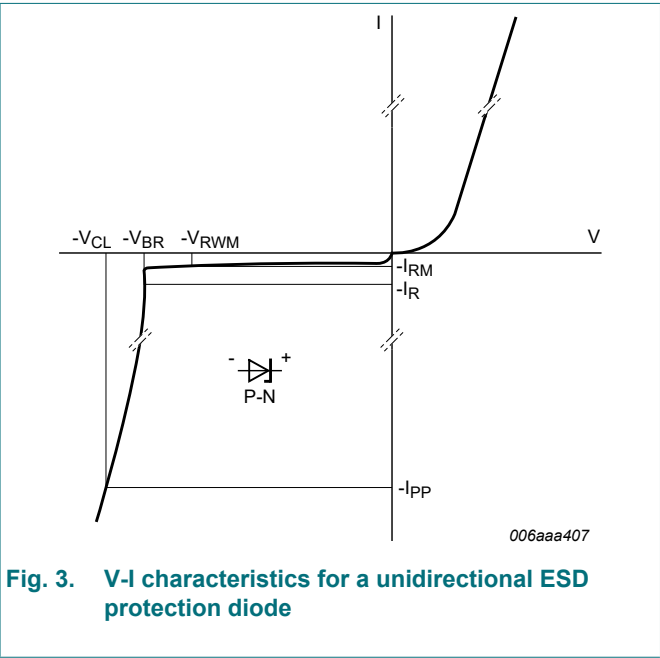
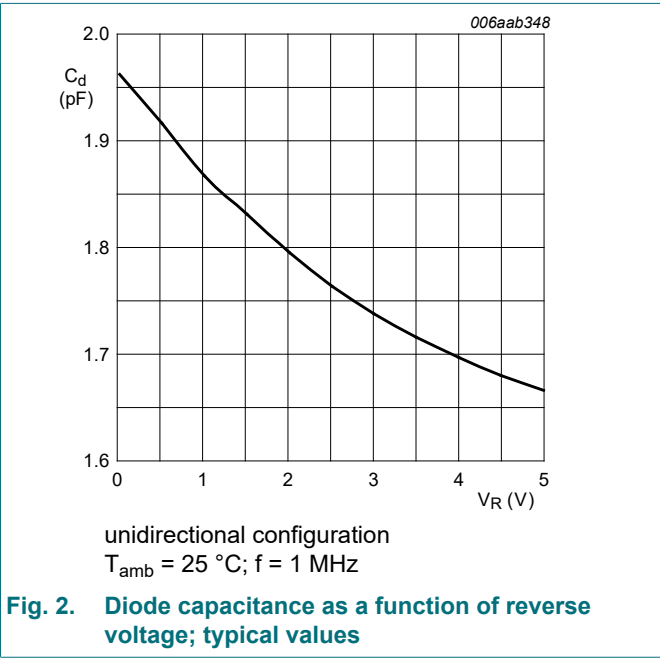


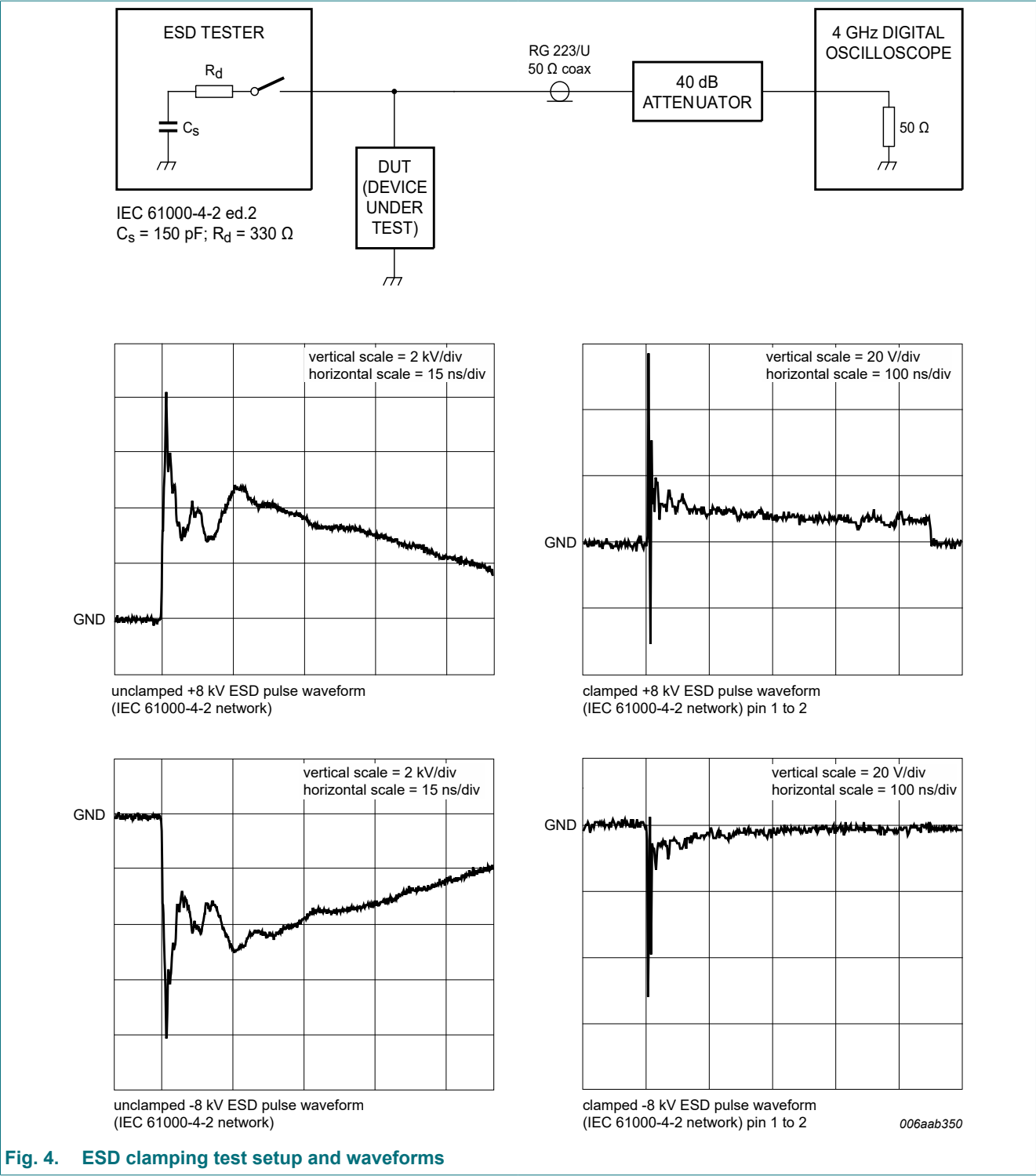
Fig. 1. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	5	V
V_{BR}	breakdown voltage	$I_R = 5\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	5.8	6.8	8.8	V
I_{RM}	reverse leakage current	$V_{RWM} = 5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	1	100	nA
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	2	2.6	pF
		$f = 1\text{ MHz}; V_R = 5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	1.7	2.3	pF
R_{diff}	differential resistance	$I_R = 1\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	100	Ω





10. Application information

The device is designed for the protection of one unidirectional data or signal line from the damage caused by ESD. The device may be used on lines where the signal polarities are either positive or negative with respect to ground.

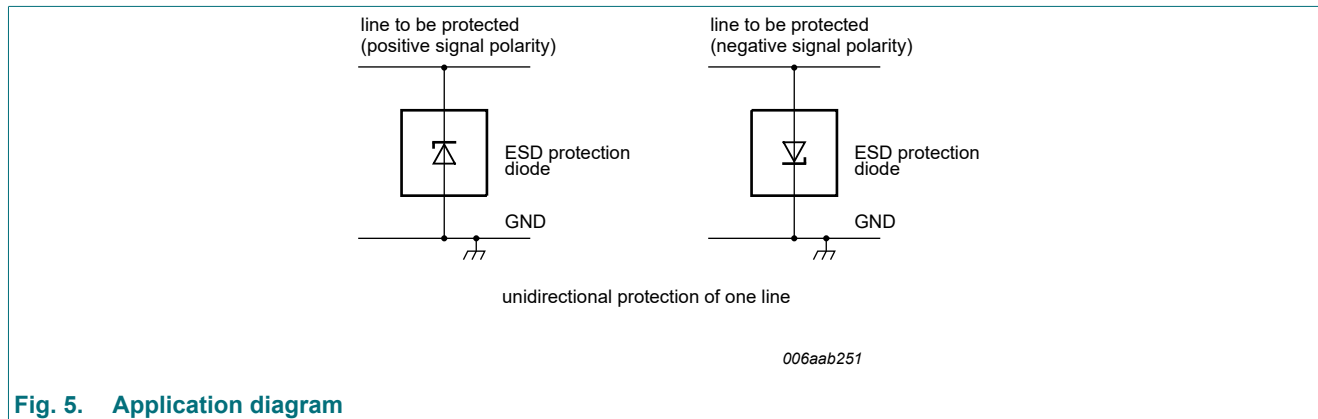


Fig. 5. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

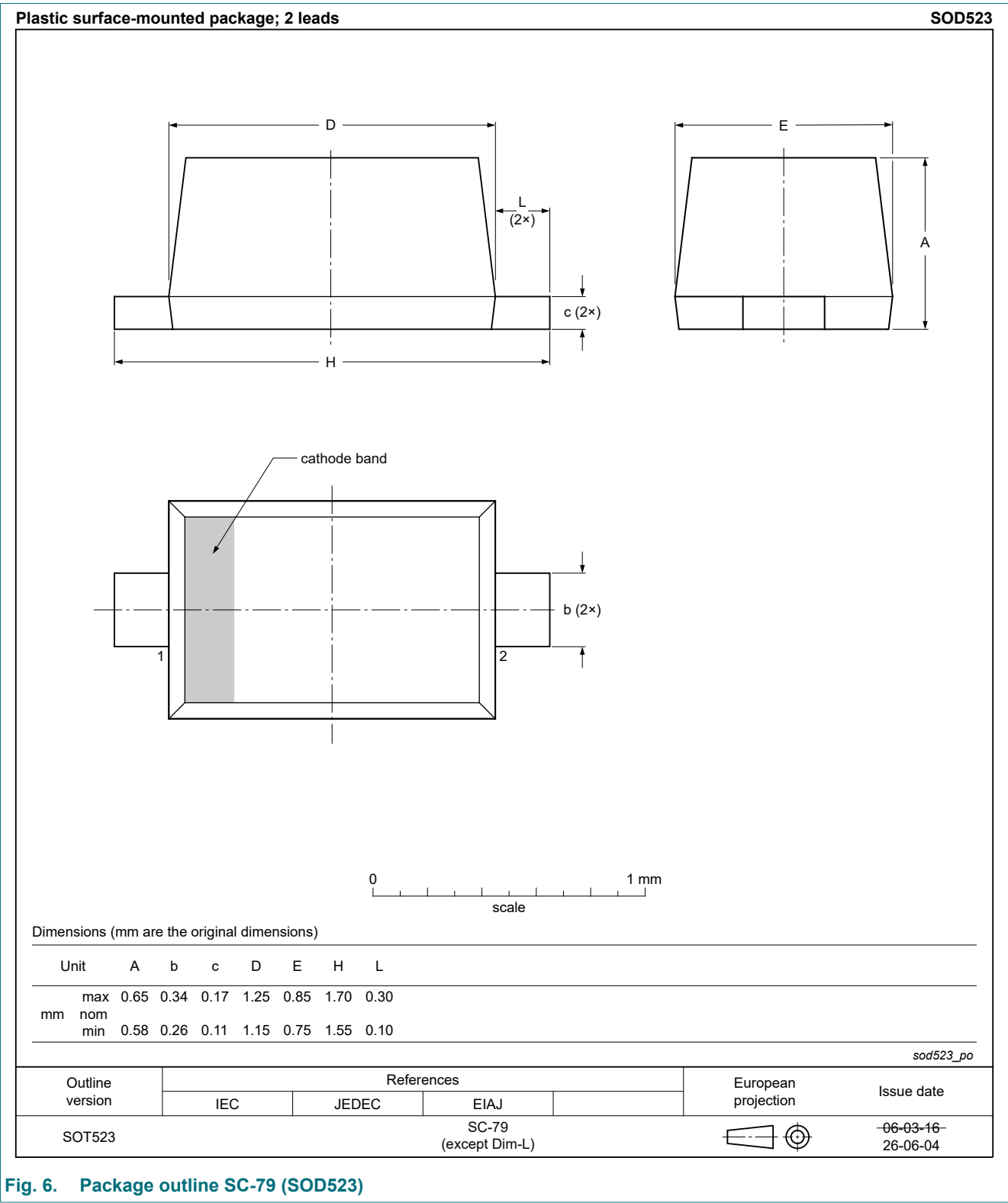
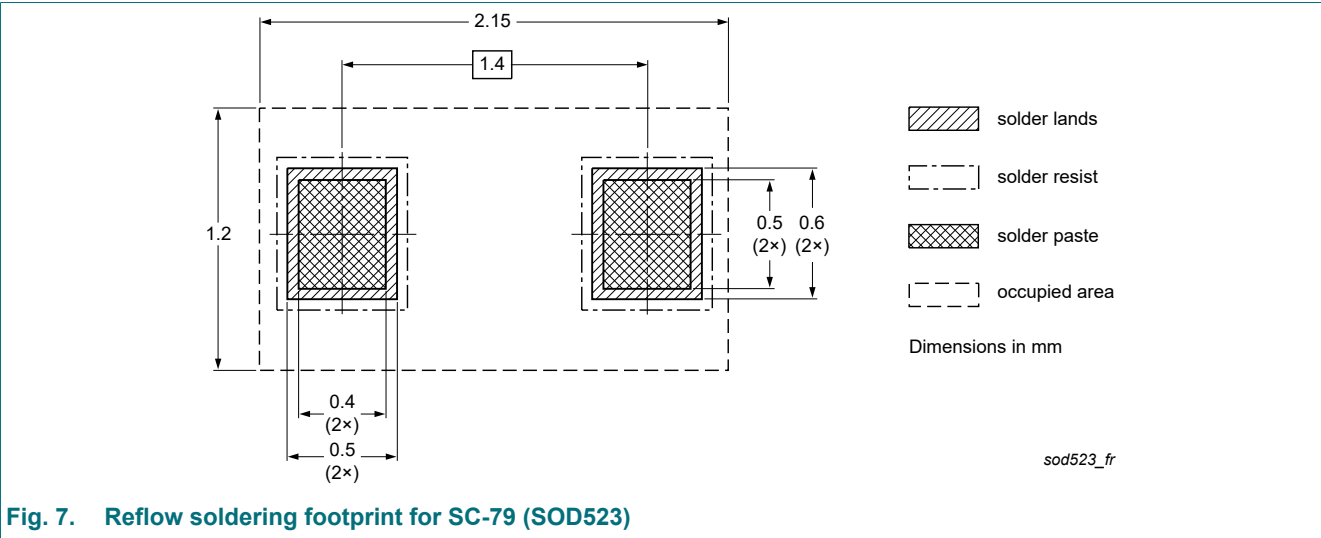


Fig. 6. Package outline SC-79 (SOD523)

12. Soldering



13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0U1UB v.4	20260806	Product data sheet	-	PESD5V0U1UB v.3
Modifications:	• Aligned SOD523 package outline drawing			
PESD5V0U1UB v.3	20230401	Product data sheet	-	PESD5V0U1UB v.2
PESD5V0U1UB v.2	20210406	Product data sheet	-	PESD5V0U1UA_UB_UL_1
PESD5V0U1UA_UB_UL_1	20081030	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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