Data Sheet
April 2019

MAX24505, MAX24510
5 or 10 Output Any-to-Any Clock Multipliers with Internal EEPROM

General Description

The MAX24505 and MAX24510 are flexible, high-performance clock multiplier/synthesizer ICs with two independent APLLs. Each APLL performs any-to-any frequency conversion. From any input clock frequency 9.72MHz to 750MHz these devices can produce frequency-locked APLL output frequencies up to 750MHz and as many as 10 differential output clock signals that are integer divisors of the APLL frequencies. Output jitter is typically 0.18 to 0.3ps RMS for an integer multiply and 0.25 to 0.4ps RMS for a fractional multiply (12kHz to 20MHz). Each device can configure itself from internal EEPROM so that clock signals are available immediately after power-up or reset.

Applications

Frequency conversion and synthesis applications in a wide variety of equipment types

Ordering Information

PART	OUTPUTS	TEMP RANGE	PIN-PACKAGE
MAX24505EXG2	5	-40 to +85	81-CSBGA
MAX24510EXG2	10	-40 to +85	81-CSBGA

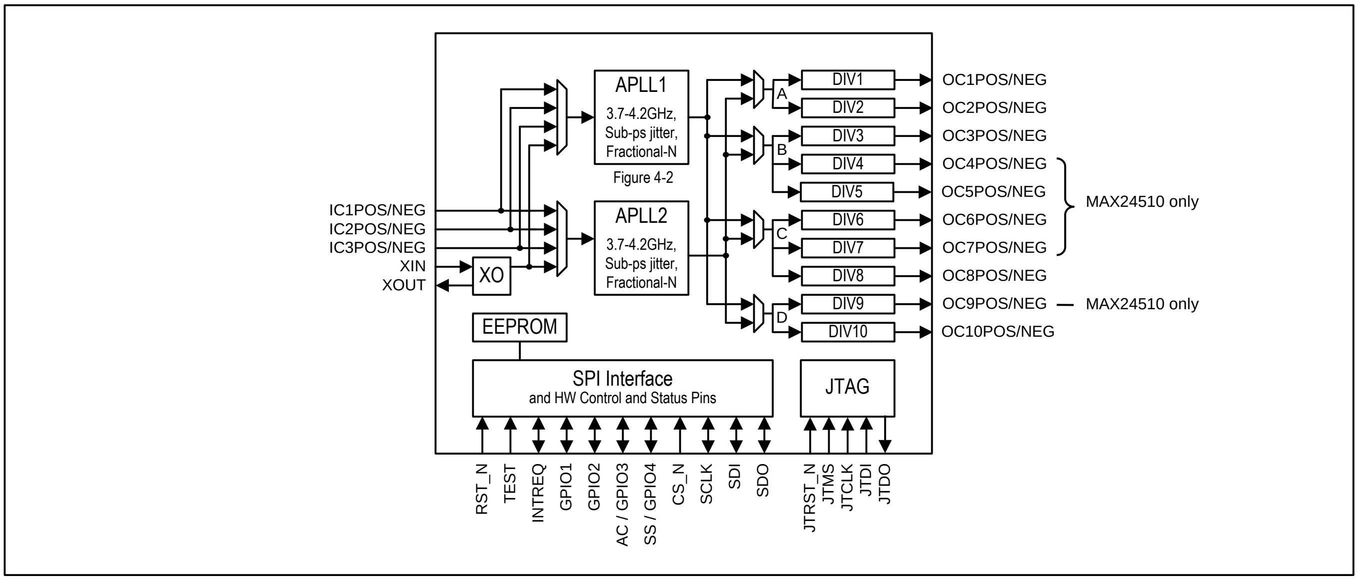
Suffix 2 denotes a lead(Pb)-free/RoHS-compliant package.

Register Map appears on page 18.

Features

- **Input Clocks**
    - One Crystal or CMOS Input
    - Three Differential or CMOS Inputs
    - Differential to 750MHz, CMOS/TTL to 160MHz
    - Clock Selection By Pin or Register Control
- **Two APLLs Plus 5 or 10 Output Clocks**
    - APLLs Perform High Resolution Fractional-N Clock Multiplication
    - Any Output Frequency from <1Hz to 750MHz
    - Each Output Has an Independent Divider
    - Output Jitter Typically 0.18 to 0.3ps RMS for Integer Multiply and 0.25 to 0.4ps RMS for Fractional Multiply (12kHz to 20MHz)
    - Outputs are CML or 2xCMOS, Can Interface to LVDS, LVPECL, HSTL, SSTL and HCSL
    - CMOS Output Voltage from 1.5V to 3.3V
- **General Features**
    - Automatic Self-Configuration at Power-Up from Internal EEPROM Memory
    - SPI™ Processor Interface
    - 1.8V + 3.3V Operation (5V Tolerant)
    - -40 to +85°C Operating Temp. Range

Block Diagram



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1. Application Examples

Figure 1-1. Frequency Synthesis Application Example

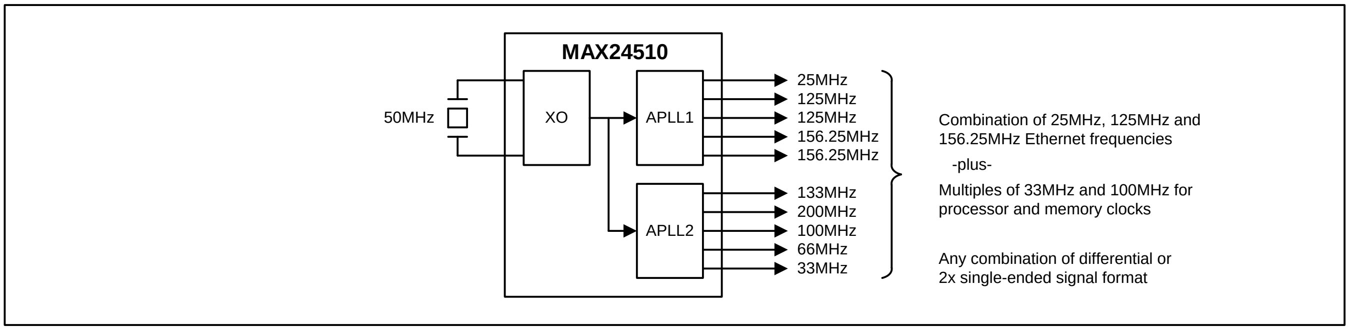
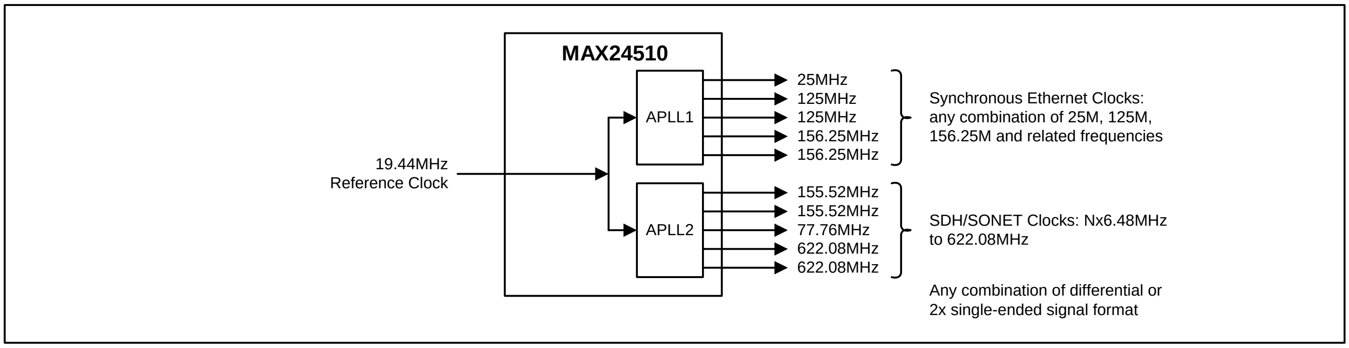


Figure 1-2. Frequency Conversion Application Example



2. Detailed Features

2.1 APLL Features

- Two independent APLLs
- Very high-resolution fractional scaling (i.e. non-integer multiplication)
- Output jitter is typically 0.18 to 0.3ps RMS for an integer multiply and 0.25 to 0.4ps RMS for a fractional multiply (12kHz to 20MHz integration band, for output frequencies >100MHz)
- Telecom output frequencies include 622.08MHz for SONET/SDH and 625MHz for Synchronous Ethernet
- Bypass mode for each APLL supports system testing and allows the devices to be used in fanout applications

2.2 Output Clock Features

- Up to five (MAX24505) or ten (MAX24510) low-jitter output clocks
- Each output can be one differential output or two CMOS/TTL outputs
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL components
- Each output can be any integer divisor of an APLL output clock
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can also produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Can produce PCIe-compliant output clocks (PCIe gen. 1, 2 and 3)
- Per-output delay adjustment
- Per-output enable/disable

2.3 General Features

- SPI serial microprocessor interface
- Automatic self-configuration at power-up from internal EEPROM memory
- Four general-purpose I/O pins
- Register set can be write-protected

3. Pin Descriptions

Table 3-1. Input Clock Pin Descriptions

PIN NAME	TYPE(1)	PIN DESCRIPTION
IC1POS, IC1NEG	I_{DIFF}	**Input Clocks 1 – 3.** Differential or CMOS/TTL signal format. Programmable frequency. *Differential:* See Table 7-4 for electrical specifications, and see Figure 7-1 for recommended external circuitry for interfacing these differential inputs to LVDS, LVPECL or CML output pins on other devices. *CMOS/TTL:* Connect the single-ended signal to the POS pin. Connect the NEG pin to a capacitor (0.1µF or 0.01µF) to VSS_IO. As shown in Figure 7-1, the NEG pin is internally biased to approximately 1.2V. Treat the NEG pin as a sensitive node; minimize stubs; do not connect to anything else including other NEG pins. *Unused:* The POS and NEG pins can be left floating.
IC2POS, IC2NEG		
IC3POS, IC3NEG		
XIN	I	**Crystal Oscillator Input.** An on-chip XO circuit is designed to work with an external crystal connected to the XIN and XOUT pins. See section 4.2.2 for crystal characteristics and recommended external components. Alternately, the on-chip XO circuit can be disabled, and XIN can be used as a single-ended input clock pin that can accept a clock signal amplitude from 1.8V to 3.3V.
XOUT	O	**Crystal Oscillator Output.** See section 4.2.2 for crystal characteristics and recommended external components.

Table 3-2. Output Clock Pin Descriptions

PIN NAME	TYPE(1)	PIN DESCRIPTION
OC1POS, OC1NEG OC2POS, OC2NEG OC3POS, OC3NEG OC4POS, OC4NEG OC5POS, OC5NEG OC6POS, OC6NEG OC7POS, OC7NEG OC8POS, OC8NEG OC9POS, OC9NEG OC10POS, OC10NEG	O_{DIFF}	**Differential Output Clocks 1 through 10.** CML, HSTL or 1 or 2 CMOS. Programmable frequency. See Table 7-5 and Figure 7-2 for electrical specifications and recommended external circuitry for interfacing to LVDS, LVPECL or CML input pins on other devices. See Table 7-6 for electrical specifications for interfacing to CMOS and HSTL inputs on other devices. See Figure 7-3 for recommended external circuitry for interfacing to HCSL inputs on other devices.

Table 3-3. Global Pin Descriptions

PIN NAME	TYPE(1)	PIN DESCRIPTION
RST_N	I_{PU}	**Reset (Active Low).** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as RST_N is low. RST_N should be held low for at least 100ns.
TEST	I_{PD}	**Factory Test Mode Select.** Wire this pin to VSS for normal operation.
GPIO1	I/O_{PU}	**General-Purpose I/O Pin 1.** GPCR.GPIO1C configures this pin. Its state is indicated in GPSR.GPIO1.
GPIO2	I/O_{PD}	**General-Purpose I/O Pin 2.** GPCR.GPIO2C configures this pin. Its state is indicated in GPSR.GPIO2.
AC / GPIO3	I/O_{PU}	**Auto Configuration / General-Purpose I/O Pin 3.** If this pin is high when RST_N goes high the device automatically configures its registers based on the configuration script stored in EEPROM memory. See section 4.9. After reset GPCR.GPIO3C configures this pin. Its state is indicated in GPSR.GPIO3.
SS / GPIO4	I/O_{PD}	**Source Switch / General-Purpose I/O Pin 4.** When APLLCR2.EXTSW=1 this pin behaves as SS, the source-switching control input.. See section 4.4.1. When EXTSW=0 this pin behaves as GPIO4, it is configured by GPCR.GPIO4C, and its state is indicated in GPSR.GPIO4.

Table 3-4. SPI Interface Pin Descriptions

See section 4.6 for functional description and Table 7-12 for timing specifications.

PIN NAME	TYPE(1)	PIN DESCRIPTION
CS_N	I	**Chip Select.** The CS_N, SCLK, SDI and SDO pins together are a SPI slave port through which an external SPI master can communicate with the device. This pin must be asserted (low) to read or write internal registers.
SCLK	I	**Serial Clock.** SCLK is always driven by the SPI bus master.
SDI	I	**Serial Data Input.** The SPI bus master transmits data to the device on this pin.
SDO	O_3	**Serial Data Output.** The device transmits data to the SPI bus master on this pin.

Table 3-5. JTAG Interface Pin Descriptions

See Section 6 for functional description and Table 7-13 for timing specifications.

PIN NAME	TYPE(1)	PIN DESCRIPTION
JTRST_N	I_{PU}	**JTAG Test Reset (Active Low).** Asynchronously resets the test access port (TAP) controller. JTRST_N should be held low during device power-up. If not used, JTRST_N can be held low or high after power-up.
JTCLK	I	**JTAG Clock.** Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high.
JTDI	I_{PU}	**JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high.
JTDO	O_3	**JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave floating.
JTMS	I_{PU}	**JTAG Test Mode Select.** Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used connect to 3.3V or leave floating.

Table 3-6. Power-Supply Pin Descriptions

PIN NAME	TYPE(1)	PIN DESCRIPTION
VDD_18	P	**Digital I/O Power Supply.** 1.8V ±5%.
VDD_33	P	**Digital I/O Power Supply.** 3.3V ±5%.
VDD_APLL1_18	P	**APLL1 Power Supply.** 1.8V ±5%. Also supply for IC1 input.
VDD_APLL1_33	P	**APLL1 Power Supply.** 3.3V ±5%. Also supply for IC1 input.
VDD_APLL2_18	P	**APLL2 Power Supply.** 1.8V ±5%. Also supply for IC2 and IC3 inputs.
VDD_APLL2_33	P	**APLL2 Power Supply.** 3.3V ±5%. Also supply for IC2 and IC3 inputs.
VDD_DIG_18	P	**Core Digital Power Supply.** 1.8V ±5%.
VDD_OC_18	P	**Output Clock Power Supply.** 1.8V ±5%.
VDD_XO_18	P	**Crystal Oscillator Power Supply.** 1.8V ±5%.
VDD_XO_33		**Crystal Oscillator Power Supply.** 3.3V ±5%.
VDDO18A	P	**Output Clock Power Supply, Bank A (OC1, OC2).** 1.8V ±5%.
VDDO18B	P	**Output Clock Power Supply, Bank B (OC3–OC5).** 1.8V ±5%.
VDDO18C	P	**Output Clock Power Supply, Bank C (OC6-OC8).** 1.8V ±5%.
VDDO18D	P	**Output Clock Power Supply, Bank D (OC9, OC10).** 1.8V ±5%.
VDDOA	P	**Output Clock Power Supply, Bank A (OC1, OC2).** 1.5V to 3.3V ±5%.
VDDOB	P	**Output Clock Power Supply, Bank B (OC3–OC5).** 1.5V to 3.3V ±5%.
VDDOC	P	**Output Clock Power Supply, Bank C (OC6-OC8).** 1.5V to 3.3V ±5%.
VDDOD	P	**Output Clock Power Supply, Bank D (OC9, OC10).** 1.5V to 3.3V ±5%.
VSS_APLL1	P	**Return for VDD_APLL1 Supplies.**
VSS_APLL2	P	**Return for VDD_APLL2 Supplies.**
VSS_DIG	P	**Core Digital Return.**
VSS_OC	P	**Output Clock Return.**
VSS_XO	P	**Crystal Oscillator Return.**
VSSOA	P	**Return for VDDOA Supply.**
VSSOB	P	**Return for VDDOB Supply.**
VSSOC	P	**Return for VDDOC Supply.**

PIN NAME	TYPE(1)	PIN DESCRIPTION
VSSOD	P	**Return for VDDOD Supply.**
VSUB	P	**Substrate Voltage.** Connect to board ground.

Note 1: All pins, except power and analog pins, are CMOS/TTL unless otherwise specified in the pin description.

PIN TYPES

I = input pin
I_{DIFF} = differential input, can be interfaced to LVDS, LVPECL, CML, HSTL or CMOS/TTL signals
I_{PD} = input pin with internal 50kΩ pulldown
I_{PU} = input pin with internal 50kΩ pullup
I/O = input/output pin
IO_{PD} = input/output pin with internal 50kΩ pulldown
IO_{PU} = input/output pin with internal 50kΩ pullup
O = output pin
O_3 = output pin that can be tri-stated (i.e., placed in a high-impedance state)
O_{DIFF} = differential output, CML format
P = power-supply pin

Note 2: All digital pins, except ICn and OCn, are I/O pins in JTAG mode. ICn and OCn pins do not have JTAG functionality.

4. Functional Description

4.1 Device Identification and Protection

The 16-bit read-only ID field in the ID1 and ID2 registers is set to 00C3h = 195 decimal. The device revision can be read from the REV register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the PROT register.

4.2 Local Oscillator or Crystal

Section 4.2.1 describes how to connect an external oscillator and the required characteristics of the oscillator. Section 4.2.2 describes how to connect an external crystal to the on-chip crystal oscillator and the required characteristics of the crystal.

4.2.1 External Oscillator

A signal from an external oscillator can be connected to any of the clock inputs: IC1, IC2, IC3 or XIN. The external oscillator can be any frequency from 9.72MHz to 750MHz and either differential or single-ended (single-ended only on XIN). For lowest output jitter, a differential signal is best. To minimize jitter when a single-ended signal is used, the signal must be properly terminated and must have very short trace length. A poorly terminated single-ended signal can greatly increase output jitter, and long single-ended trace lengths are more susceptible to noise. If the oscillator is located more than 2cm away from the device, consider connecting the single-ended oscillator output to an LVDS driver IC (such as MAX9110) and sending a differential clock signal to the device pins.

While the stability of the external oscillator over temperature can be important, its absolute frequency accuracy is less important. This is because any known frequency inaccuracy of the oscillator can be compensated in the APLLs by adjusting the APLLs' fractional feedback divider values (AFBDIV) by ppb or ppm to compensate for oscillator frequency error.

4.2.1.1 Oscillator Characteristics to Minimize Output Jitter

The jitter on output clock signals depends on the phase noise and frequency of the external oscillator. For the device to operate with the lowest possible output jitter, the external oscillator should have the following characteristics:

- Phase Noise: Typical value of -148dBc/Hz or lower at 10kHz offset from the carrier.
- Frequency: The higher the better, subject to 102.4MHz maximum.

4.2.2 On-Chip Crystal Oscillator

The crystal oscillator is designed to drive a fundamental mode, AT-cut crystal resonator. See Table 4-1 for recommended crystal specifications. When a crystal is not connected between XIN and XOUT, the XIN pin can be used as a single-ended input to the APLLs.

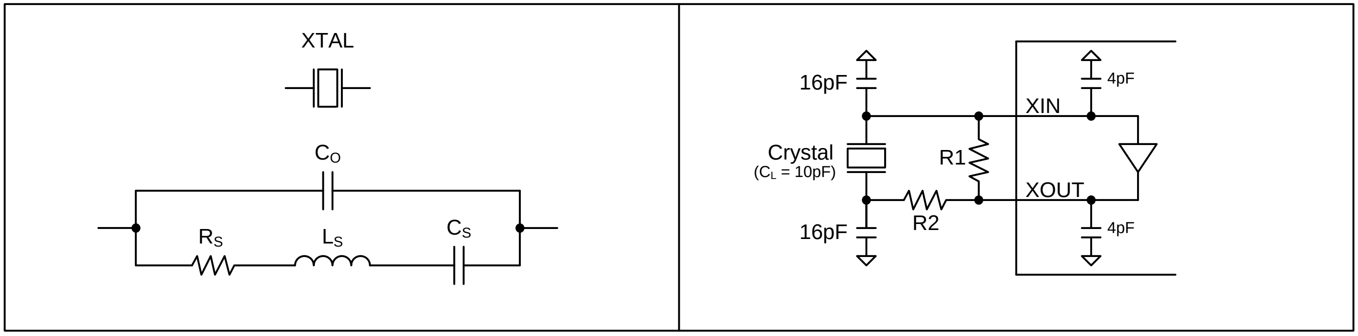
To use the crystal oscillator with an external crystal, set MCR2.XIEN=1 to enable the XIN pin logic and set MCR2.XOEN=1 to enable the XOUT pin so the XO can oscillate. To use the XIN pin as a single-ended input, set MCR2.XIEN=1 to enable the XIN pin and set MCR2.XOEN=0 to disable the XOUT pin to minimize power and noise. If the XIN pin is not used, set MCR2.XIEN=0 and MCR2.XOEN=0 to minimize power and noise.

See Figure 4-1 for the crystal equivalent circuit and the recommended external capacitor connections. To achieve a crystal load (C_L) of 10pF, an external 16pF is placed in parallel with the 4pF internal capacitance of the XIN pin, and an external 16pF is placed in parallel with the 4pF internal capacitance of the XOUT pin. The crystal then sees a load of 20pF in series with 20pF, which is 10pF total load. Note that the 16pF capacitance values in Figure 4-1 include all capacitance on those nodes. If, for example, PCB trace capacitance between crystal pin and IC pin is 2pF then 14pF capacitors should be used to make 16pF total.

The crystal, traces, and two external capacitors should be placed on the board as close as possible to the XIN and XOUT pins to reduce crosstalk of active signals into the oscillator. Also no active signals should be routed under the crystal circuitry.

Note: Crystals have temperature sensitivies that can cause crystal oscillator frequency changes in response to ambient temperature changes. In applications where significant temperature changes are expected near the crystal, it is recommended that the crystal be covered with a thermal cap, or an external XO, TCXO or OCXO should be used instead.

Figure 4-1. Crystal Equivalent Circuit / Crystal and Capacitor Connections



Note 1: R1=1MΩ. The value of R2 is a function of crystal frequency, loading and maximum power rating. Contact the factory for guidance in choosing the right R1 resistor for a specific crystal.

Table 4-1. Crystal Selection Parameters

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillation Frequency		f_{OSC}	25	25, 50, 51.2[1]	52	MHz
Shunt Capacitance		C_O		2	5	pF
Load Capacitance		C_L		10		pF
Equivalent Series Resistance (ESR)[2]	f_{OSC} < 40MHz	R_S			60	Ω
	f_{OSC} > 40MHz	R_S			50	Ω
Maximum Crystal Drive Level			100			µW

Note 1: Crystal frequencies of 49.152MHz, 50MHz and 51.2MHz are excellent choices for lowest output jitter.

Note 2: These ESR limits are chosen to constrain crystal drive level to less than 100µW. If the crystal can tolerate a drive level greater than 100µW then proportionally higher ESR is acceptable.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillator Frequency Stability vs. Power Supply	f_{FVD}		0.2	0.5	ppm per 10% Δ in VDD

Any known frequency inaccuracy of the crystal can be compensated in the APLLs by adjusting the APLLs' fractional feedback divider values (AFBDIV) by ppb or ppm to compensate for crystal frequency error.

4.3 Input Signal Format Configuration

Input clocks IC1 and IC2 are enabled by setting MCR2.IC1EN=1 and IC2EN=1, respectively. The power consumed by a differential receiver is shown in Table 7-2. The electrical specifications for these inputs are listed in Table 7-4. Each input clock can be configured to accept nearly any differential signal format by using the proper set of external components (see Table 7-4 and Figure 7-1). To configure these differential inputs to accept single-ended CMOS or TTL signals, connect the single-ended signal to the POS pin, and connect the NEG pin to a capacitor (0.1µF or 0.01µF) to VSS. As shown in Figure 7-1, the NEG pin is internally biased to approximately 1.2V. If a 1.2V bias is unsuitable, an external voltage divider can be used to set a different bias. If an input is not used, both POS and NEG pins can be left floating.

Table 4-2. Input Clock Capabilities

Input Clock	Signal Format	Frequence Range (MHz)
IC1	Diferential or CMOS/TTL	Differential: 9.72MHz to 750MHz Single-ended: 9.72MHz to 160MHz
IC2		
IC3		

4.4 APLL Configuration

4.4.1 Input Selection and Frequency

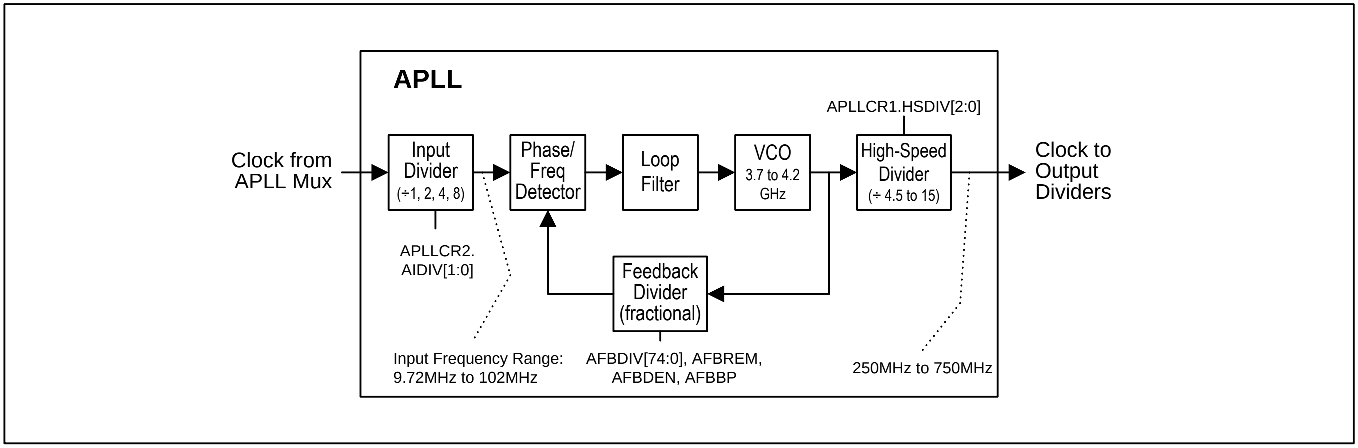
The input to each APLL can be controlled by the SS input pin or by the APLLCR2.APLLMUX register field. When APLLCR2.EXTSW=0, the APLLCR2.APLLMUX register field controls the APLL input mux.

When APLLCR2.EXTSW=1, the SS input pin controls the APLL input mux. When SS=0, the mux selects the input specified by APLLCR2.APLLMUX. When SS=1, the mux selects the input specified by APLLCR2.ALTMUX.

The input signal to the APLL's phase-frequency detector must be in the range 9.72MHz to 102.4MHz. For input frequencies above 102.4MHz, the APLL's input divider can be configured to divide the signal by 2, 4 or 8 (APLLCR2.AIDIV) to get a frequency below 102.4MHz. Note that higher APLL input frequencies give lower output jitter, all else being equal.

4.4.2 Output Frequency

Figure 4-2. APLL Block Diagram



An APLL is enabled when APLLCR1.APLLEN=1. The APLLs have a fractional-N architecture and therefore can produce output frequencies that are either integer or non-integer multiples of the input clock frequency. Figure 4-2 shows a block diagram of the APLL, which is built around an ultra-low-jitter multi-GHz VCO. Register fields AFBDIV, AFBREM, AFBDEN and AFBBP configure the frequency multiplication ratio of the APLL. The APLLCR1.HSDIV field specifies how the VCO frequency is divided down by the high-speed divider. Dividing by six is the typical setting to produce 622.08MHz for SDH/SONET or 625MHz for Ethernet applications. The HSDIV divider produces a clock signal with a 50% duty cycle for all divider values including odd numbers.

Internally, the exact APLL feedback divider value is expressed in the form AFBDIV + AFBREM / AFBDEN * $2^{-(66\text{-AFBBP})}$. This feedback divider value must be chosen such that APLL_input_frequency * feedback_divider_value is in the operating range of the VCO (as specified in Table 7-7). The AFBDIV term is a fixed-point number with 9 integer bits and a configurable number of fractional bits (up to 66, as specified by AFBBP). Typically AFBBP is set to 42 to specify that AFBDIV has 66 – 42 = 24 fractional bits. Using more than 24 fractional bits does not yield a detectable benefit. Using less than 12 fractional bits is not recommended.

The following equations show how to calculate the feedback divider values for the situation where the APLL should multiply the APLL input frequency by integer M and also fractionally scale by the ratio of integers N / D. In other words, VCO_frequency = input_frequency * M * N / D. An example of this is multiplying 77.76MHz by M=48 and scaling by N / D = 255 / 237 for forward error correction applications.

$$\text{AFBDIV} = \text{trunc}(M * N / D * 2^{24}) \quad (1)$$

$$\text{lsb\_fraction} = M * N / D * 2^{24} - \text{AFBDIV} \quad (2)$$

$$\text{AFBDEN} = D \quad (3)$$

$$\text{AFBREM} = \text{round}(\text{lsb\_fraction} * \text{AFBDEN}) \quad (4)$$

$$\text{AFBBP} = 66 - 24 = 42 \quad (5)$$

The trunc() function returns only the integer portion of the number. The round() function rounds the number to the nearest integer. In Equation (1), AFBDIV is set to the full-precision feedback divider value, M * N / D, truncated after the 24th fractional bit. In Equation (2) the temporary variable 'lsb_fraction' is the fraction that was truncated in Equation (1) and therefore is not represented in the AFBDIV value. In Equation (3), AFBDEN is set to the denominator of the original M * N / D ratio. In Equation (4), AFBREM is calculated as the integer numerator of a fraction (with denominator AFBDEN) that equals the 'lsb_fraction' temporary variable. Finally, in Equation (5) AFBBP is set to 66 – 24 = 42 to correspond with AFBDIV having 24 fractional bits.

When a fractional scaling scenario involves multiplying an integer M times multiple scaling ratios N_1 / D_1 through N_n / D_n, the equations above can still be used if the numerators are multiplied together to get $N = N_1 \times N_2 \times \ldots \times N_n$ and the denominators are multiplied together to get $D = D_1 \times D_2 \times \ldots \times D_n$.

Note that one easy way to calculate the exact values to write to the APLL registers is to use the MAX24505/MAX24510 evaluation board software, available on the MAX24505/MAX24510 page of Microsemi's website. This software can be used even when no evaluation board is attached to the computer.

Note: After the APLL's feedback divider settings are configured in register fields AFBDIV, AFBREM, AFBDEN and AFBBP, the APLL enable bit APLLCR1.APLLEN must be changed from 0 to 1 to cause the APLL to reacquire lock with the new settings.

4.5 Output Clock Configuration

The MAX24505 has five output clocks signals. The MAX24510 has ten output clocks signals. Each output has individual divider, enable and signal format controls.

4.5.1 Enable, Signal Format, Voltage and Interfacing

Using the OCCR2.OCSF register field, each output pair can be disabled or configured as a CML output, an HSTL output, or one or two CMOS outputs. When an output is disabled it is high impedance and the output driver is in a low-power state. In CMOS mode, the OCxNEG pin can be disabled, in phase or inverted vs. the OCxPOS pin. In CML mode the normal 800mV V_{OD} differential voltage is available as well as a lower-power 400mV V_{OD}. All of these options are specified by OCCR2.OCSF.

Device clock outputs are grouped into four banks as shown below:

Bank	MAX24505 Outputs	MAX24510 Outputs
A	OC1, OC2	OC1, OC2
B	OC3	OC3, OC4, OC5
C	OC8	OC6, OC7, OC8
D	OC10	OC9, OC10

Each bank has its own power supply and ground pin to allow CMOS or HSTL signal swing from 1.5V to 3.3V for glueless interfacing to neighboring components. If OCSF is set to HSTL mode then a 1.5V power supply voltage should be used to get a standards-compliant HSTL output.

Note that differential (CML) outputs must have a bank power supply of 3.3V. If other outputs in that bank are configured for CMOS operation, the CMOS outputs will also have a 3.3V power supply. However, CMOS outputs from that bank can be externally attenuated using resistor divider networks if needed.

The differential outputs can be easily interfaced to LVDS, LVPECL, CML, HSTL and other differential inputs on neighboring ICs using a few external passive components. See App Note HFAN-1.0 for details.

4.5.2 Frequency Configuration

The frequency of each output is determined by which APLL it is connected to, the configuration the APLL and the per-output dividers. Each bank of outputs can be connected to either APLL1 or APLL2. The register fields to control the bank muxes are AMUX, BMUX, CMUX and DMUX, respectively, in the MCR1 register.

Each output has two output dividers, a 7-bit medium-speed divider (OCCR1.MSDIV) and a 24-bit output divider (OCDIV registers). These dividers are in series, medium-speed divider first then output divider. These dividers produce signals with 50% duty cycle for all divider values including odd numbers.

Since each output has its own independent dividers, the device can output families of related frequencies that have an APLL output frequency as a common multiple. For example, for Ethernet clocks, a 625MHz APLL output clock can be divided by four for some outputs to get 156.25MHz, divided by five for other outputs to get 125MHz, and divided by 25 for other outputs to get 25MHz. Similarly, for SDH/SONET clocks, a 622.08MHz APLL output clock can be divided by 4 to get 155.52MHz, by 8 to get 77.76MHz, by 16 to get 38.88MHz or by 32 to get 19.44MHz.

Various divisors of the APLL output clock can be brought out on any combination of outputs. For the very lowest output jitter, however, frequencies such as 156.25MHz and 125MHz that are not integer divisors of one another should come from separate banks whenever possible.

4.5.3 Phase Adjustment

The phase of an output signal can be shifted by 180° by setting OCCR1.POL=1. In addition, the phase can be adjusted using the OCCR3.PHADJ register field. The adjustment is in units of APLL output clock cycles. For example, if the APLL output frequency is 625MHz then one APLL output clock cycle is 1.6ns, the smallest phase adjustment is 0.8ns, and the adjustment range is ±5.6ns.

4.6 Microprocessor Interface

The device presents a SPI slave port on the CS_N, SCLK, SDI, and SDO pins. SPI is a widely used master/slave bus protocol that allows a master and one or more slaves to communicate over a serial bus. The device is always a slave. Masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master, which also generates the SCLK signal. The device receives serial data on the SDI pin and transmits serial data on the SDO pin. SDO is high impedance except when the device is transmitting data to the bus master.

Bit Order. The register address and all data bytes are transmitted most significant bit first on both SDI and SDO.

Clock Polarity and Phase. The device latches data on SDI on the rising edge of SCLK and updates data on SDO on the falling edge of SCLK. SCLK does not have to toggle between accesses, i.e., when CS_N is high.

Device Selection. Each SPI slave has its own chip-select line. To select the device, the bus master drives its CS_N pin low.

Command and Address. After driving CS_N low, the bus master transmits an 8-bit command followed by a 16-bit register address. The available commands are shown below.

Command	Hex	Bit Order, Left to Right
Write Enable	0x06	0000 0110
Write	0x02	0000 0010
Read	0x03	0000 0011
Read Status	0x05	0000 0101

Read Transactions. The device registers are accessible when EESEL=0. The internal EEPROM memory is accessible when EESEL=1. See section 5.1.3. After driving CS_N low, the bus master transmits the read command followed by the 16-bit register address. The device then responds with the requested data byte on SDO, increments its address counter, and prefetches the next data byte. If the bus master continues to demand data, the device continues to provide the data on SDO, increment its address counter, and prefetch the following byte. The read transaction is completed when the bus master drives CS_N high. See Figure 4-3.

Register Write Transactions. The device registers are accessible when EESEL=0. After driving CS_N low, the bus master transmits the write command followed by the 16-bit register address followed by the first data byte to be written. The device receives the first data byte on SDI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the device continues to write the data received and increment its address counter. The write transaction is completed when the bus master drives CS_N high. See Figure 4-5.

EEPROM Writes. The EEPROM memory is accessible when EESEL=1. After driving CS_N low, the bus master transmits the write enable command and then drives CS_N high to set the internal write enable latch. The bus master then drives CS_N low again and transmits the write command followed by the 16-bit register address followed by the first data byte to be written. The device first copies the page to be written from EEPROM to its page buffer. The device then receives the first data byte on SDI, writes it to its page buffer, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the device continues to write the data received to its page buffer and continues to increment its address counter. The address counter rolls over at the 32-byte boundary (i.e. when the five least-significant address bits are 11111). When the bus master drives CS_N high, the device transfers the data in the page buffer to the appropriate page in the EEPROM memory. See Figure 4-4 and Figure 4-5.

EEPROM Read Status. After the bus master drives CS_N high to end an EEPROM write command, the EEPROM memory is not accessible for up to 5ms while the data is transferred from the page buffer. To determine when this transfer is complete, the bus master can use the Read Status command. After driving CS_N low, the bus master transmits the Read Status command. The device then responds with the status byte on SDO. In this byte, the least significant bit is set to 1 if the transfer is still in progress and 0 if the transfer has completed.

Early Termination of Bus Transactions. The bus master can terminate SPI bus transactions at any time by pulling CS_N high. In response to early terminations, the device resets its SPI interface logic and waits for the start of the next transaction. If a register write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, the data byte is not written. If an EEPROM write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, none of the bytes in that write transaction are written.

Design Option: Wiring SDI and SDO Together. Because communication between the bus master and the device is half-duplex, the SDI and SDO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the SDI/SDO line when the device is transmitting.

AC Timing. See Table 7-12 and Figure 7-4 for AC timing specifications for the SPI interface.

Figure 4-3. SPI Read Transaction Functional Timing

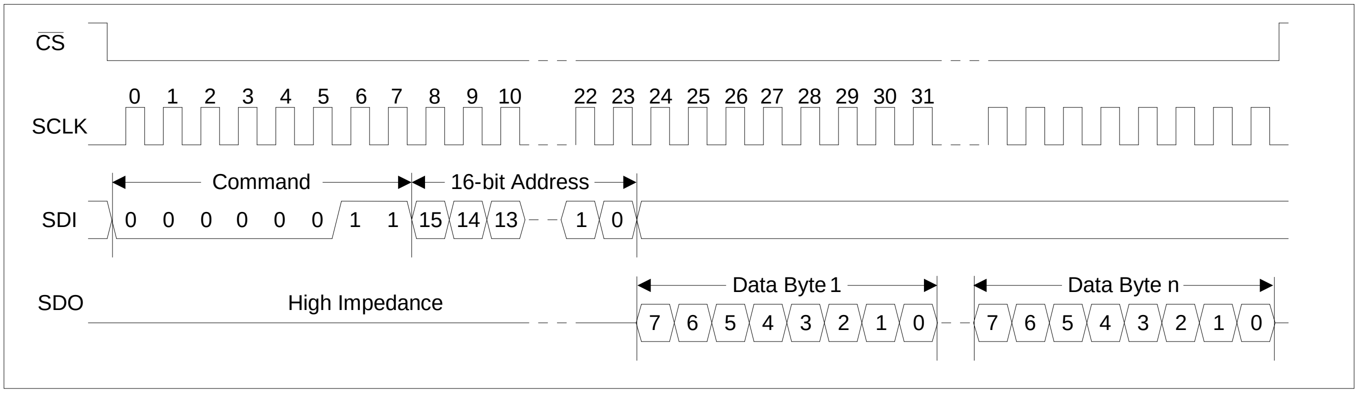


Figure 4-4. SPI Write Enable Transaction Functional Timing

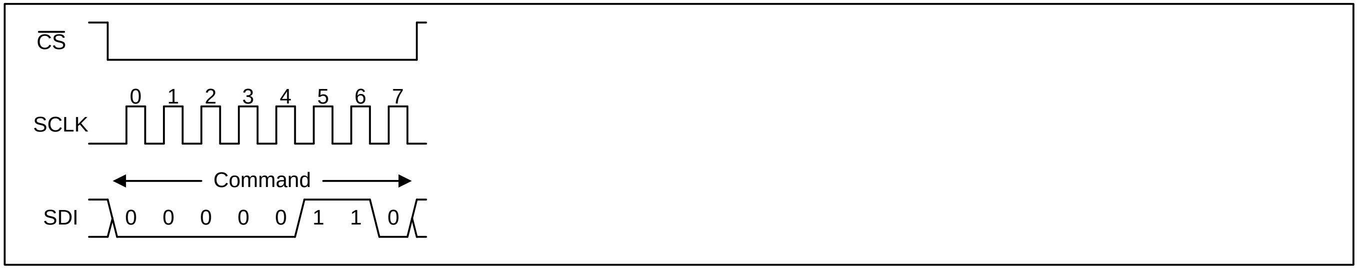
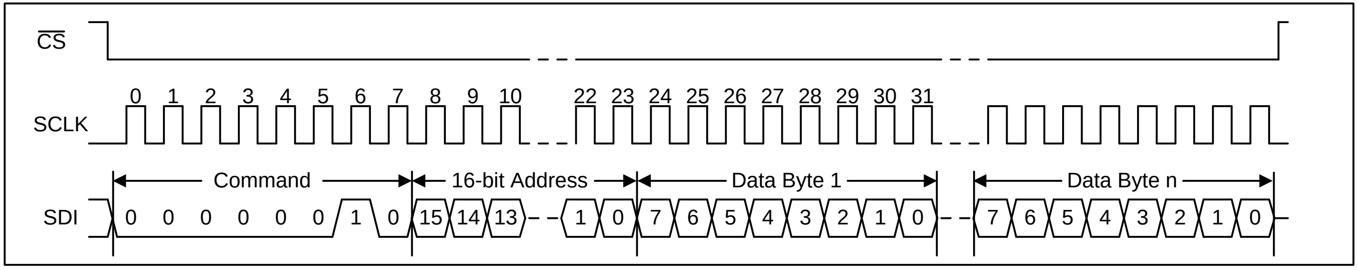


Figure 4-5. SPI Write Transaction Functional Timing



4.7 Reset Logic

The device has three reset controls: the RST_N pin, the RST bit in MCR1, and the JTAG reset pin JTRST_N. The RST_N pin asynchronously resets the entire device, except for the JTAG logic. When the RST_N pin is low all internal registers are reset to their default values, including those fields which latch their default values from, or based on, the states of configuration input pins when the RST_N goes high. **The RST_N pin must be asserted once after power-up while the external oscillator is stabilizing.** Reset should be asserted for at least 100ns.

The MCR1.RST bit resets the entire device (except for the microprocessor interface, the JTAG logic and the RST bit itself), but when RST is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead these fields are reset to the default values that were latched when the RST_N pin was last active.

Microsemi recommends holding RST_N low while the external oscillator starts up and stabilizes. An incorrect reset condition could result if RST_N is released before the oscillator has started up completely.

Important: System software must wait at least 100µs after reset (RST_N pin or RST bit) is deasserted before initializing the device as described in section 4.9.

4.8 Power-Supply Considerations

Due to the multi-power-supply nature of the device, some I/Os have parasitic diodes between a <3.3V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the <3.3V supply and the 3.3V supply to force the 3.3V supply to be within one parasitic diode drop of the <3.3V supply. The second method is to ramp up the 3.3V supply first and then ramp up the <3.3V supply.

4.9 Initialization and EEPROM Configuration Memory

After power-up or reset, a series of writes must be done to the device to tune it for optimal performance. This series of writes is called the initialization script. Each die revision has a different initialization script. For the latest initialization scripts contact Microsemi timing products technical support. The initialization script must be part of the self-configuration script stored in the device’s internal EEPROM memory. The MAX24505/MAX24510 EV kit software automatically includes the correct initialization script in configuration scripts it creates.

5. Register Descriptions

The device has an overall address range from 000h to 1FFh. Table 5-1 in Section 5.2 shows the register map. In each register, bit 7 is the MSB and bit 0 is the LSB. Register addresses not listed and bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 5-1.

5.1 Register Types

5.1.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status bits can cause an interrupt request if enabled to do so by corresponding interrupt enable bits.

5.1.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

5.1.3 Bank-Switched Registers

To simplify the device's register map and documentation, some registers are bank-switched, meaning banks of registers are switched in and out of the register map based on the value of a bank-select control field.

At the top level, The EESEL register is a bank-select control field that maps the device registers into the memory map at address 0x1 and above when EESEL=0 and maps the EEPROM memory into the memory map at address 0x1 and above when EESEL=1. The EESEL register itself is always in the memory map at address 0x0 for both EESEL=0 and EESEL=1.

When EESEL=0 (device registers) the bank-switched sections of the memory map are: the APLL registers and the output clock registers.

The registers for the APLLs are bank-switched in the APLL Registers section of Table 5-1. The APLLSEL register is the bank-select control field for the APLL registers.

The registers for the output clocks are bank-switched in the Output Clock Registers section of Table 5-1. The OCSEL register is the bank-select control field for the output clock registers.

5.2 Register Map

Table 5-1. Register Map

Note: *Register names are hyperlinks to register definitions. Underlined fields are read-only.*

ADDR	*REGISTER*	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Global Registers									
00h	EESEL	—	—	—	—	—	—	—	EESEL
01	ID1	ID[7:0]							
02	ID2	ID[15:8]							
03	REV	REV[7:0]							
04	PROT	PROT[7:0]							
05	MCR1	RST	—	—	—	AMUX	BMUX	CMUX	DMUX
06	MCR2	XIEN	XOEN	IC1EN	IC2EN	IC3EN	—	—	—
07	APLLSR	—	A2LKIE	A2LKL	A2LK	—	A1LKIE	A1LKL	A1LK
GPIO Registers									
08	GPCR	GPIO4C[1:0]		GPIO3C[1:0]		GPIO2C[1:0]		GPIO1C[1:0]	
09	GPSR	—	—	—	—	GPIO4	GPIO3	GPIO2	GPIO1
0A	GPIO1SS	POL	OD	REG[2:0]			BIT[2:0]		
0B	GPIO2SS	POL	OD	REG[2:0]			BIT[2:0]		
0C	GPIO3SS	POL	OD	REG[2:0]			BIT[2:0]		
0D	GPIO4SS	POL	OD	REG[2:0]			BIT[2:0]		
APLL Registers									
10	APLLSEL	—	—	—	—	—	—	APLLSEL[1:0]	
11	APLLCR1	APLLEN	APLLBYP	DALIGN	—	HSDIV[3:0]			
12	APLLCR2	AIDIV[1:0]		EXTSW	ALTMUX[1:0]		APLLMUX[2:0]		
22	AFBDIV1	AFBDIV[3:0]				—	—	—	—
23	AFBDIV2	AFBDIV[11:4]							
24	AFBDIV3	AFBDIV[19:12]							
25	AFBDIV4	AFBDIV[27:20]							
26	AFBDIV5	AFBDIV[35:28]							
27	AFBDIV6	AFBDIV[43:36]							
28	AFBDIV7	AFBDIV[51:44]							
29	AFBDIV8	AFBDIV[59:52]							
2A	AFBDIV9	AFBDIV[67:60]							
2B	AFBDIV10	—	AFBDIV[74:68]						
2C	AFBDEN1	AFBDEN[7:0]							
2D	AFBDEN2	AFBDEN[15:8]							
2E	AFBDEN3	AFBDEN[23:16]							
2F	AFBDEN4	AFBDEN[31:24]							
30	AFBREM1	AFBREM[7:0]							
31	AFBREM2	AFBREM[15:8]							
32	AFBREM3	AFBREM[23:16]							
33	AFBREM4	AFBREM[31:24]							
34	AFBBP	AFBBP[7:0]							
Output Clock Registers									
40	OCSEL	—	—	—	—	OCSEL[3:0]			
41	OCCR1	—	MSDIV[6:0]						

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
42	OCCR2	—	—	DRIVE[1:0]		OCSF[3:0]			
43	OCCR3	PHADJ[3:0]				—	POL	—	DALEN
44	OCDIV1	OCDIV[7:0]							
45	OCDIV2	OCDIV[15:8]							
46	OCDIV3	OCDIV[23:16]							

5.3 Register Definitions

5.3.1 Global Registers

Register Name:	EESEL
Register Description:	EEPROM Memory Selection Register
Register Address:	00h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	—	EESEL
Default	0	0	0	0	0	0	0	0

Bit 0: EEPROM Memory Select (EESEL). This bit is a bank-select that specfies whether device register space or EEPROM memory is mapped into addresses 0x1 and above. See sections 4.6 and 5.1.3.

0 = Device registers
1= EEPROM memory

Register Name: ID1
Register Description: Device Identification Register, LSB
Register Address: 01h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ID[7:0]							
Default	see below							

Bits 7 to 0: Device ID (ID[7:0]). The full 16-bit ID field spans this register and ID2.
MAX24505: ID[15:0] = 0x00C6.
MAX24510: ID[15:0] = 0x00C7.

Register Name: ID2
Register Description: Device Identification Register, MSB
Register Address: 02h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ID[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Device ID (ID[15:8]). See the ID1 register description.

Register Name: REV
Register Description: Device Revision Register
Register Address: 03h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REV[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Device Revision (REV[7:0]). Contact the factory to interpret this value and determine the latest revision.

Register Name: PROT
Register Description: Protection Register
Register Address: 04h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PROT[7:0]							
Default	1	0	0	0	0	1	0	1

Bits 7 to 0: Protection Control (PROT[7:0]). This field can be used to protect the rest of the register set from inadvertent writes. In protected mode writes to all other registers are ignored. In single unprotected mode, one register (other than PROT) can be written, but after that write the device reverts to protected mode (and the value of PROT is internally changed to 00h). In fully unprotected mode all register can be written without limitation. See section 4.1.
1000 0101 = Fully unprotected mode
1000 0110 = Single unprotected mode
All other values = Protected mode

Register Name: MCR1
Register Description: Master Configuration Register 1
Register Address: 05h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RST	—	—	—	AMUX	BMUX	CMUX	DMUX
Default	0	0	0	0	0	0	0	0

Bit 7: Device Reset (RST). When this bit is high the entire device is held in reset, and all register fields, except the RST bit itself, are reset to their default states. When RST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead these fields are reset to the default values that were latched from the pins when the RST pin was last active. See section 4.7.
0 = Normal operation
1 = Reset

Bit 3: Bank A Mux Control (AMUX). This field selects the source APLL for the bank A outputs. See the block diagram on page 1 and section 4.5.2.
0 = APLL1
1 = APLL2

Bit 2: Bank B Mux Control (BMUX). This field selects the source APLL for the bank B outputs. See the block diagram on page 1 and section 4.5.2.
0 = APLL1
1 = APLL2

Bit 1: Bank C Mux Control (CMUX). This field selects the source APLL for the bank C outputs. See the block diagram on page 1 and section 4.5.2.
0 = APLL1
1 = APLL2

Bit 0: Bank D Mux Control (DMUX). This field selects the source APLL for the bank D outputs. See the block diagram on page 1 and section 4.5.2.
0 = APLL1
1 = APLL2

Register Name: MCR2
Register Description: Master Configuration Register 2
Register Address: 06h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	XIEN	XOEN	IC1EN	IC2EN	IC3EN	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 7: XIN Enable (XIEN). This field enables/disables the XIN pin and the XO analog circuitry. See section 4.2.2.
0 = Disable
1 = Enable

Bit 6: XOUT Enable (XOEN). This field enables and disables the XOUT pin driver. When XOUT is disabled the external crystal is not driven and the XO doesn't oscillate. See section 4.2.2.
0 = Disable (high impedance)
1 = Enable (XO amplifier drives external crystal)

Bit 5: IC1POS/NEG Enable (IC1EN). This field enables and disables the IC1POS/NEG differential receiver. The power consumption for the differential receiver is shown in Table 7-2. See section 4.3.
0 = Disable (power down)
1 = Enable

Bit 4: IC2POS/NEG Enable (IC2EN). This field enables and disables the IC2POS/NEG differential receiver. The power consumption for the differential receiver is shown in Table 7-2. See section 4.3.
0 = Disable (power down)
1 = Enable

Bit 3: IC3POS/NEG Enable (IC3EN). This field enables and disables the IC3POS/NEG differential receiver. The power consumption for the differential receiver is shown in Table 7-2. See section 4.3.
0 = Disable (power down)
1 = Enable

Register Name: APLLSR
Register Description: APLL Status Register
Register Address: 07h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	A2LKIE	A2LKL	A2LK	—	A1LKIE	A1LKL	A1LK
Default	0	0	0	0	0	0	0	0

Bit 6: APLL2 Lock Interrupt Enable (A2LKIE). This bit is an interrupt enable for the A2LKL bit.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 5: APLL2 Lock Latched Status (A2LKL). This latched status bit is set to 1 when the A2LK status bit changes state (set or cleared). A2LKL is cleared when written with a 1. When A2LKL is set it can cause an interrupt request if the A2LKIE interrupt enable bit is set.

Bit 4: APLL2 Lock Status (A2LK). This real-time status bit indicates the lock status of APLL2.
0 = Not locked
1 = Locked

Bit 2: APLL1 Lock Interrupt Enable (A1LKIE). This bit is an interrupt enable for the A1LKL bit.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 1: APLL1 Lock Latched Status (A1LKL). This latched status bit is set to 1 when the A1LK status bit changes state (set or cleared). A1LKL is cleared when written with a 1. When A1LKL is set it can cause an interrupt request if the A1LKIE interrupt enable bit is set.

Bit 0: APLL1 Lock Status (A1LK). This real-time status bit indicates the lock status of APLL1.
0 = Not locked
1 = Locked

5.3.2 GPIO Registers

Register Name: GPCR
Register Description: GPIO Configuration Register
Register Address: 08h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO4C[1:0]		GPIO3C[1:0]		GPIO2C[1:0]		GPIO1C[1:0]	
Default	0	0	0	0	0	0	0	0

Bits 7 to 6: GPIO4 Configuration (GPIO4C[1:0]). When APLLCR2.EXTSW=0, the SS/GPIO4 pin behaves as GPIO4, and this field configures the GPIO4 pin as a general-purpose input a general-purpose output driving low or high, or a status output. When GPIO4 is an input its current state can be read from GPSR.GPIO4. When GPIO4 is a status output, the GPIO4SS register specifies which status bit is output. When APLLCR2.EXTSW=1 the SS/GPIO4 pin behaves as SS and this field is ignored.
00 = General-purpose input
01 = Status output
10 = General-purpose output driving low
11 = General-purpose output driving high

Bits 5 to 4: GPIO3 Configuration (GPIO3C[1:0]). This field configures the GPIO3 pin as a general-purpose input, a general-purpose output driving low or high, or a status output. When GPIO3 is an input its current state can be read from GPSR.GPIO3. When GPIO3 is a status output, the GPIO3SS register specifies which status bit is output.
00 = General-purpose input
01 = Status output
10 = General-purpose output driving low
11 = General-purpose output driving high

Bits 3 to 2: GPIO2 Configuration (GPIO2C[1:0]). This field configures the GPIO2 pin as a general-purpose input, a general-purpose output driving low or high, or a status output. When GPIO2 is an input its current state can be read from GPSR.GPIO2. When GPIO2 is a status output, the GPIO2SS register specifies which status bit is output.
00 = General-purpose input
01 = Status output
10 = General-purpose output driving low
11 = General-purpose output driving high

Bits 1 to 0: GPIO1 Configuration (GPIO1C[1:0]). This field configures the GPIO1 pin as a general-purpose input a general-purpose output driving low or high, or a status output. When GPIO1 is an input its current state can be read from GPSR.GPIO1. When GPIO1 is a status output, the GPIO1SS register specifies which status bit is output.
00 = General-purpose input
01 = Status output
10 = General-purpose output driving low
11 = General-purpose output driving high

Register Name: GPSR
Register Description: GPIO Status Register
Register Address: 09h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	GPIO4	GPIO3	GPIO2	GPIO1
Default	0	0	0	0	0	0	0	0

Bit 3: GPIO4 State (GPIO4). This bit indicates the current state of the GPIO4 pin.
0 = low
1 = high

Bit 2: GPIO3 State (GPIO3). This bit indicates the current state of the GPIO3 pin.
0 = low
1 = high

Bit 1: GPIO2 State (GPIO2). This bit indicates the current state of the GPIO2 pin.
0 = low
1 = high

Bit 0: GPIO1 State (GPIO1). This bit indicates the current state of the GPIO1 pin.
0 = low
1 = high

Register Name: GPIO1SS
Register Description: GPIO1 Status Select Register
Register Address: 0Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	POL	OD	REG[2:0]			BIT[2:0]		
Default	0	0	0	0	0	0	0	0

Bit 7: Pin Polarity (POL).
0 = Normal: GPIO pin has the same polarity as the status bit it follows
1 = Inverted: GPIO pin has inverted polarity vs. the status bit it follows

Bit 6: Open-Drain Enable (OD).
0 = Push-Pull: GPIO pin is driven in both inactive and active state
1 = Open-Drain: GPIO pin is driven in the active state but is high impedance in the inactive state

Bits 5 to 3: Status Register (REG[2:0]). When GPCR.GPIO1C=01, this field specifies the register of the status bit that GPIO1 will follow while the BIT field below specifies the status bit within the register. Setting the combination of this field and the BIT field below to point to a bit that isn't implemented as a real-time or latched status register bit results in GPIO1 being driven low.
000 – 100 = {unused value}
101 = APLL Lock. The address of the status bit that GPIO follows is 07h (APLLSR register)
110 = {unused value}
111 = Interrupt Output: GPIO1 is active when a latched status bit and its corresponding interrupt enable bit are both active. The POL and OD bits define pin behavior for the active and inactive states.

Bits 2 to 0: Status Bit (BIT[2:0]). When GPCR.GPIO1C=01, the REG field above specifies the register of the status bit that GPIO1 will follow while this field specifies the status bit within the register. Setting the combination of the REG field and this field to point to a bit that isn't implemented as a real-time or latched status register bit results in GPIO1 being driven low. 000=bit 0 of the register. 111=bit 7 of the register.

Register Name: GPIO2SS
Register Description: GPIO2 Status Select Register
Register Address: 0Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	POL	OD	REG[2:0]			BIT[2:0]		
Default	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO1SS except they control GPIO2.

Register Name: GPIO3SS
Register Description: GPIO3 Status Select Register
Register Address: 0Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	POL	OD	REG[2:0]			BIT[2:0]		
Default	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO1SS except they control GPIO3.

Register Name: GPIO4SS
Register Description: GPIO4 Status Select Register
Register Address: 0Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	POL	OD	REG[2:0]			BIT[2:0]		
Default	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO1SS except they control GPIO4.

5.3.3 APLL Registers

Register Name: APLLSEL
Register Description: APLL Select Register
Register Address: 10h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	APLLSEL[1:0]	
Default	0	0	0	0	0	0	0	1

Bits 1 to 0: APLL Select (APLLSEL[1:0]). This field is a bank-select control that specifies the APLL for which registers are mapped into the APLL Registers section of Table 5-1. See Section 5.1.3.

00 = {unused value}
01 = APLL1
10 = APLL2
11 = {unused value}

Register Name: APLLCR1
Register Description: APLL Configuration Register 1
Register Address: 11h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	APLLEN	APLLBYP	DALIGN	—	HSDIV[3:0]			
Default	0	0	0	0	0	0	0	0

The APLL registers are bank-selected by the APLLSEL register. See section 5.1.3.

Bit 7: APLL Enable (APLLEN). This bit enables and disables the APLL. When unused, the APLL should be disabled to reduce power consumption. See section 4.4.2.

0 = Disabled
1 = Enabled

Bit 6: APLL Bypass (APLLBYP). This bit controls an internal bypass mux in the APLL.

0 = Normal APLL operation
1 = APLL bypass: the APLL input signal is routed directly to the APLL output

Bit 5: Align Output Dividers (DALIGN). A 0 to 1 transition on this bit causes a simultaneous reset of the medium-speed dividers and the output clock dividers for all output clocks where OCCR3.DALEN=1. After this reset all DALEN=1 output clocks derived from the same APLL will be falling-edge aligned. This bit should be set then cleared once during system startup. Setting this bit during normal system operation can cause phase jumps in the output clock signals.

Bits 3 to 0: APLL High-Speed Divider (HSDIV[3:0]). This bit controls the high-speed divider block in the APLL (see Figure 4-2). See section 4.4.2.

0000 = Divide by 6
0001 = Divide by 4.5
0010 = Divide by 5
0011 = Divide by 5.5
0100 = Divide by 6
0101 = Divide by 6.5
0110 = Divide by 7
0111 = Divide by 7.5
1000 = Divide by 8
1001 = Divide by 9
1010 = Divide by 10
1011 = Divide by 11
1100 = Divide by 12
1101 = Divide by 13
1110 = Divide by 14
1111 = Divide by 15

Register Name: APLLCR2
Register Description: APLL Configuration Register 2
Register Address: 12h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AIDIV[1:0]		EXTSW	ALTMUX[1:0]		APLLMUX[2:0]		
Default	0	0	0	0	0	0	0	0

The APLL registers are bank-selected by the APLLSEL register. See section 5.1.3.

Bits 7 to 6: APLL Input Divider (AIDIV). This field controls the APLL input divider. See Figure 4-2.

00 = Divide by 1
01 = Divide by 2
10 = Divide by 4
11 = Divide by 8

Bit 5: APLL External Switching Mode (EXTSW). This bit enables APLL external reference switching mode. In this mode, if the SS pin is low the APLL input mux is controlled by APLLCR2.APLLMUX. If the the SS pin is high the APLL input mux is controlled by APLLCR2.ALTMUX. See section 4.4.1.

Bits 4 to 3: APLL Alternate Mux Control (ALTMUX[1:0]). When APLLCR2.EXTSW=0 this field is ignored. When APLLCR2.EXTSW=1 and the SS pin is high this field controls the APLL input mux. See section 4.4.1.

00 = IC1 input
01 = IC2 input
10 = Crystal oscillator (XO) block if crystal is connected, otherwise XIN input
11 = IC3 input

Bits 2 to 0: APLL Mux Control (APLLMUX[2:0]). By default this field controls the APLL input mux. See the block diagram on page 1 for the location of this mux. When APLLCR2.EXTSW=1 and the SS pin is high, this field is ignored, and the APLL's clock source is specified by APLLCR2.ALTMUX. See section 4.4.1.

000 = IC1 input
001 = IC2 input
010 = Crystal oscillator (XO) block if crystal is connected, otherwise XIN input
011 = IC3 input
100 to 111 = {unused value}

Register Name: AFBDIV1
Register Description: APLL Feedback Divider Register 1
Register Address: 22h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[3:0]				—	—	—	—
Default	0	0	0	0	0	0	0	0

The APLL registers are bank-selected by the APLLSEL register. See section 5.1.3.

Bits 7 to 4: APLL Feedback Divider Register (AFBDIV[3:0]). The full 75 bit AFBDIV[74:0] field spans the AFBDIV1 through AFBDIV10 registers. AFBDIV is an unsigned number with 9 integer bits (AFBDIV[74:66]) and up to 66 fractional bits. AFBDIV specifies the fixed-point term of the APLL's fractional feedback divide value. The value AFBDIV=0 is undefined. Unused least significant bits must be written with 0. See section 4.4.2.

Register Name: AFBDIV2
Register Description: APLL Feedback Divider Register 2
Register Address: 23h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[11:4]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[11:4]). See the AFBDIV1 register description.

Register Name: AFBDIV3
Register Description: APLL Feedback Divider Register 3
Register Address: 24h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[19:12]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[19:12]). See the AFBDIV1 register description.

Register Name: AFBDIV4
Register Description: APLL Feedback Divider Register 4
Register Address: 25h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[27:20]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[27:20]). See the AFBDIV1 register description.

Register Name: AFBDIV5
Register Description: APLL Feedback Divider Register 5
Register Address: 26h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[35:28]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[35:28]). See the AFBDIV1 register description.

Register Name: AFBDIV6
Register Description: APLL Feedback Divider Register 6
Register Address: 27h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[43:36]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[43:36]). See the AFBDIV1 register description.

Register Name: AFBDIV7
Register Description: APLL Feedback Divider Register 7
Register Address: 28h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[51:44]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[51:44]). See the AFBDIV1 register description.

Register Name: AFBDIV8
Register Description: APLL Feedback Divider Register 8
Register Address: 29h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[59:52]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[59:52]). See the AFBDIV1 register description.

Register Name: AFBDIV9
Register Description: APLL Feedback Divider Register 9
Register Address: 2Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[67:60]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[67:60]). See the AFBDIV1 register description.

Register Name: AFBDIV10
Register Description: APLL Feedback Divider Register 10
Register Address: 2Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	AFBDIV[74:68]						
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[74:68]). See the AFBDIV1 register description.

Register Name: AFBDEN1
Register Description: APLL Feedback Divider Denominator Register 1
Register Address: 2Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDEN[7:0]							
Default	0	0	0	0	0	0	0	1

The APLL registers are bank-selected by the APLLSEL register. See section 5.1.3.

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[7:0]). The full 32-bit AFBDEN[31:0] field spans AFBDEN1 through AFBDEN4 registers. AFBDEN is an unsigned integer that specifies the denominator of the APLL's fractional feedback divide value. The value AFBDEN=0 is undefined. When AFBBP=0, AFBDEN must be set to 1. See section 4.4.2.

Register Name: AFBDEN2
Register Description: APLL Feedback Divider Denominator Register 2
Register Address: 2Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDEN[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[15:8]). See the AFBDEN1 register description.

Register Name: AFBDEN3
Register Description: APLL Feedback Divider Denominator Register 3
Register Address: 2Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDEN[23:16]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[23:16]). See the AFBDEN1 register description.

Register Name: AFBDEN4
Register Description: APLL Feedback Divider Denominator Register 4
Register Address: 2Fh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDEN[31:24]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[31:24]). See the AFBDEN1 register description.

Register Name: AFBREM1
Register Description: APLL Feedback Divider Remainder Register 1
Register Address: 30h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBREM[7:0]							
Default	0	0	0	0	0	0	0	0

The APLL registers are bank-selected by the APLLSEL register. See section 5.1.3.

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[7:0]). The full 32-bit AFBDEN[31:0] field spans AFBREM1 through AFBREM4 registers. AFBREM is an unsigned integer that specifies the remainder of the APLL's fractional feedback divider value. When AFBBP=0, AFBREM must be set to 0. See section 4.4.2.

Register Name: AFBREM2
Register Description: APLL Feedback Divider Remainder Register 2
Register Address: 31h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBREM[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[15:8]). See the AFBREM1 register description.

Register Name: AFBREM3
Register Description: APLL Feedback Divider Remainder Register 3
Register Address: 32h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBREM[23:16]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[23:16]). See the AFBREM1 register description.

Register Name: AFBREM4
Register Description: APLL Feedback Divider Remainder Register 4
Register Address: 33h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBREM[31:24]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[31:24]). See the AFBREM1 register description.

Register Name: AFBBP
Register Description: APLL Feedback Divider Truncate Bit Position
Register Address: 34h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBBP[7:0]							
Default	0	0	0	0	0	0	0	0

The APLL registers are bank-selected by the APLLSEL register. See section 5.1.3.

Bits 7 to 0: APLL Feedback Divider Truncate Bit Position (AFBBP[7:0]). This unsigned integer specifies the number of fractional bits that are valid in the AFBDIV value. There are 66 fractional bits in AFBDIV. The value in this AFBBP field specifies 66 – number_of_valid_AFBDIV_fractional_bits. When AFBBP=0 all 66 AFBDIV fractional bits are valid. When AFBBP=42, the most significant 24 AFBDIV fractional bits are valid and the least significant 42 bits must be set to 0. This register field is only used when the feedback divider value is expressed in the form AFBDIV + AFBREM / AFBDEN. AFBBP values greater than 66 are invalid. When AFBBP=0, AFBREM must be set to 0 and AFBDEN must be set to 1. See section 4.4.2.

5.3.4 Output Clock Registers

Register Name: OCSEL
Register Description: Output Clock Select Register
Register Address: 40h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	0	0	0	0	OCSEL[3:0]			
Default	0	0	0	0	0	0	0	1

Bits 3 to 0: Output Clock Select (OCSEL[2:0]). This field is a bank-select control that specifies the output clock for which registers are mapped into the Output Clock Registers section of Table 5-1. See section 5.1.3.

0000 = {unused value}
0001 = Output clock 1
0010 = Output clock 2
0011 = Output clock 3
0100 = Output clock 4 (MAX24510 only)
0101 = Output clock 5 (MAX24510 only)
0110 = Output clock 6 (MAX24510 only)
0111 = Output clock 7 (MAX24510 only)
1000 = Output clock 8
1001 = Output clock 9 (MAX24510 only)
1010 = Output clock 10
1011 to 1111 = {unused value}

Register Name: OCCR1
Register Description: Output Clock Configuration Register 1
Register Address: 41h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	MSDIV[6:0]						
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See section 5.1.3.

Bits 6 to 0: Medium-Speed Divider Value (MSDIV[6:0]). This field specifies the setting for the output clock's medium-speed divider. The divisor is MSDIV+1. Note that MSDIV must be set to a value that causes the output clock of the medium-speed divider to be 312.5MHz or less. See section 4.5.2.

Register Name: OCCR2
Register Description: Output Clock Configuration Register 2
Register Address: 42h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	DRIVE[1:0]		OCSF[3:0]			
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See section 5.1.3.

Bits 5 to 4: CMOS/HSTL Output Drive Strength (DRIVE[1:0]). The CMOS/HSTL output drivers have four equal sections that can be enabled or disabled to achieve four different drive strengths from 1x to 4x. When the output power supply VDDOx is 3.3V or 2.5V, the user should start with 1x and only increase drive strength if the output is highly loaded and signal transition time is unacceptable. When VDDOx is 1.8V or 1.5V the user should start with 4x and only decrease drive strength if the output signal has unacceptable overshoot.
00 = 1x
01 = 2x
10 = 3x
11 = 4x

Bits 3 to 0: Output Clock Signal Format (OCSF[3:0]). See section 4.5.1.
0000 = Disabled (high-impedance, low power mode)
0001 = CML, standard swing (V_{OD}=800mV_{P-P} typical)
0010 = CML, narrow swing (V_{OD}=400mV_{P-P} typical)
0011 = {unused value}
0100 = One CMOS, OCxPOS enabled, OCxNEG high impedance
0101 = Two CMOS, OCxNEG in phase with OCxPOS
0110 = Two CMOS, OCxNEG inverted vs. OCxPOS
0111 = HSTL (Set OCCR2.DRIVE=11 (4x) to meet JESD8-6)

Register Name: OCCR3
Register Description: Output Clock Configuration Register 3
Register Address: 43h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHADJ[3:0]				—	POL	—	DALEN
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See section 5.1.3.

Bits 7 to 4: Output Clock Phase Adjustment (PHADJ[3:0]). This field can be used to adjust the phase of output OCxPOS/NEG vs. the phase of the other clock outputs. The adjustment is in units of APLL output clock cycles. For example, if the APLL output frequency is 625MHz then one APLL output clock cycle is 1.6ns, the smallest phase adjustment is 0.8ns, and the adjustment range is ±5.6ns. See section 4.5.3.

0000 = 0 APLL output clock cycles
0001 = 0.5
0010 = 1.0
0011 = 1.5
0100 = 2.0
0101 = 2.5
0110 = 3.0
0111 = 3.5
1000 = -1.0 APLL output clock cycles
1001 = -0.5
1010 = -2.0
1011 = -1.5
1100 = -3.0
1101 = -2.5
1110 = -4.0
1111 = -3.5

Bit 2: Polarity (POL). This bit specifies the polarity of the output clock signal. When OCCR2.OCSF configures the output for one of the 2x CMOS modes, POL=1 inverts both CMOS outputs vs. the polarity they have when POL=0. See section 4.5.3.

0 = Normal
1 = Inverted

Bit 0: Divider Align Enable (DALEN). This bit enables alignment of the output clock's medium-speed divider and output clock divider when the APLLCR1.DALIGN bit is set to 1. For best results, this signal should be set to 1 for at least 2ms then set back to 0.

0 = Do not align the output clock dividers
1 = Align the output clock dividers

Register Name: OCDIV1
Register Description: Output Clock Divider Register 1
Register Address: 44h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OCDIV[7:0]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See section 5.1.3.

Bits 7 to 0: Output Clock Divider (OCDIV[7:0]). The full 24-bit OCDIV[23:0] field spans this register, OCDIV2 and OCDIV3. OCDIV is an unsigned integer. The frequency of the clock from the medium-speed divider is divided by OCDIV+1 to make the output clock signal. See section 4.5.2.

Register Name: OCDIV2
Register Description: Output Clock Divider Register 2
Register Address: 45h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OCDIV[15:8]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See section 5.1.3.

Bits 7 to 0: Output Clock Divider (OCDIV[15:8]). See the OCDIV1 register description.

Register Name: OCDIV3
Register Description: Output Clock Divider Register 3
Register Address: 46h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OCDIV[23:16]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See section 5.1.3.

Bits 7 to 0: Output Clock Divider (OCDIV[23:16]). See the OCDIV1 register description.

6. JTAG and Boundary Scan

6.1 JTAG Description

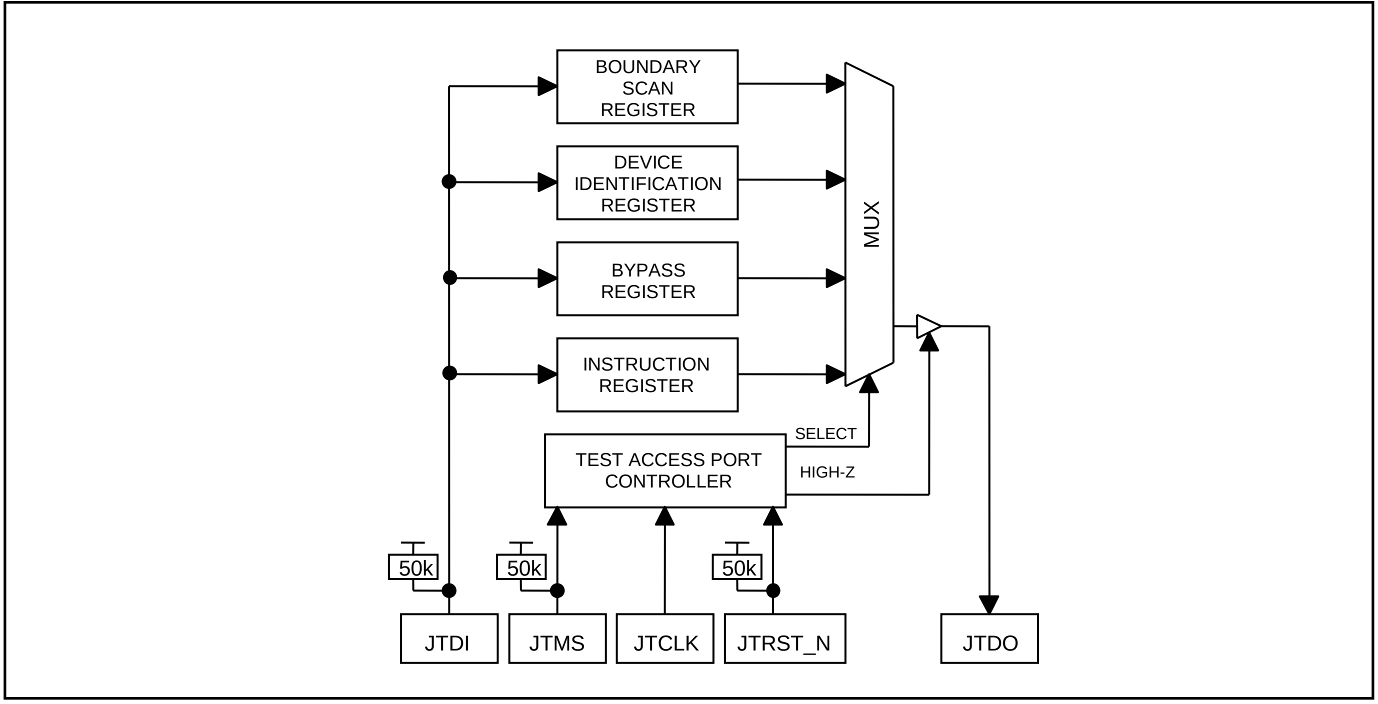
The device supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. Figure 6-1 shows a block diagram. The device contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

Test Access Port (TAP)
TAP Controller
Instruction Register

Bypass Register
Boundary Scan Register
Device Identification Register

The TAP has the necessary interface pins, namely JTCLK, JTRST_N, JTDI, JTDO, and JTMS. Details on these pins can be found in Table 3-5. Details about the boundary scan architecture and the TAP can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

Figure 6-1. JTAG Block Diagram



6.2 JTAG TAP Controller State Machine Description

This section discusses the operation of the TAP controller state machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. Each of the states denoted in Figure 6-2 is described in the following paragraphs.

Test-Logic-Reset. Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the device operates normally.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The instruction register and all test registers remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR. Data can be parallel-loaded into the test register selected by the current instruction. If the instruction does not call for a parallel load or the selected test register does not allow parallel loads, the register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

Shift-DR. The test register selected by the current instruction is connected between JTDI and JTDO and data is shifted one stage toward the serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output because of changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the instruction register's shift register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and the test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state, while moving data one stage through the instruction shift register.

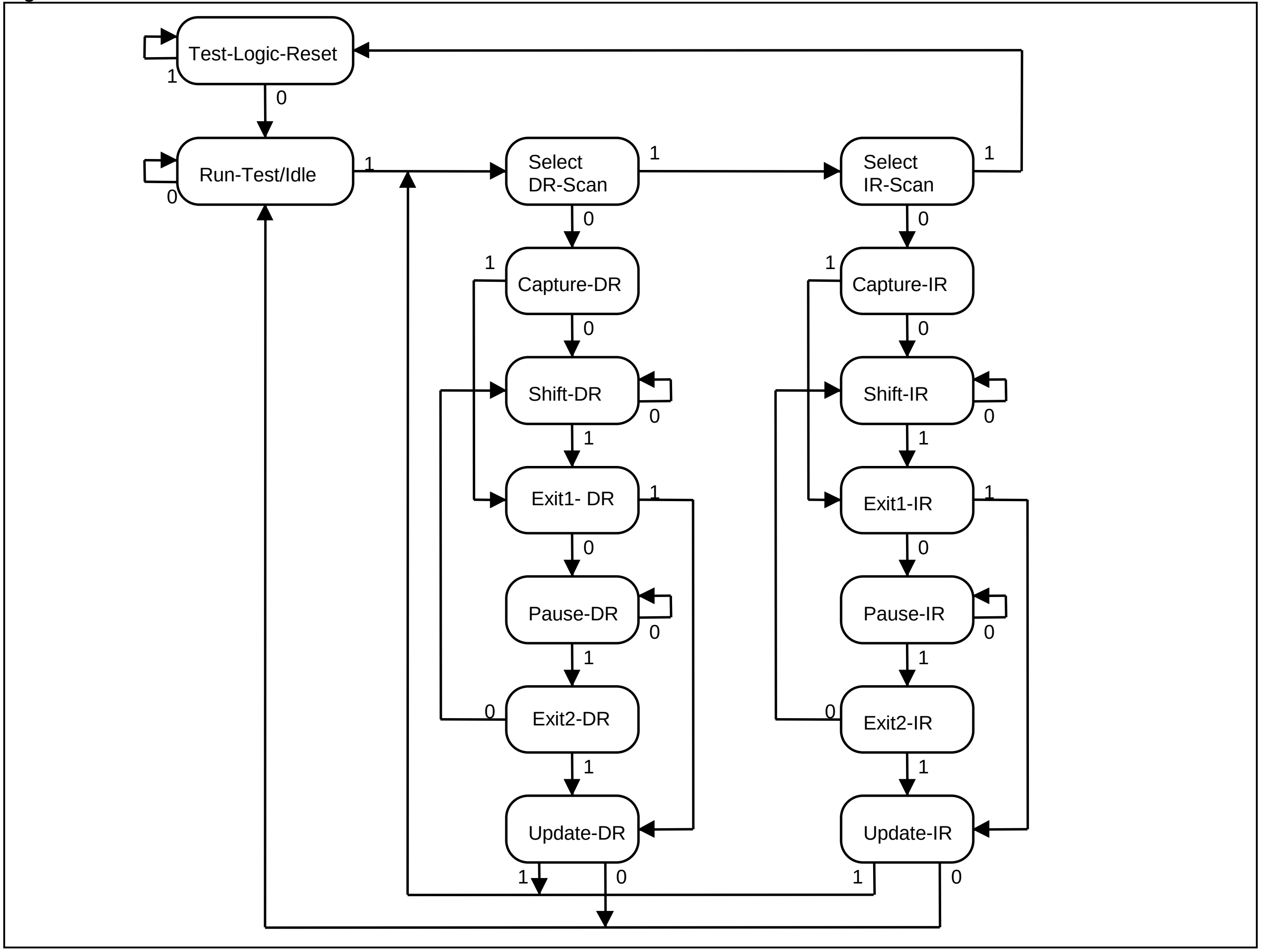
Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

Pause-IR. Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Figure 6-2. JTAG TAP Controller State Machine



6.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Table 6-1 shows the instructions supported and their respective operational binary codes.

Table 6-1. JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD. SAMPLE/PRELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. First, the digital I/Os of the device can be sampled at the boundary scan register, using the Capture-DR state, without interfering with the device's normal operation. Second, data can be shifted into the boundary scan register through JTDI using the Shift-DR state.

EXTEST. EXTEST allows testing of the interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur: (1) Once the EXTEST instruction is enabled through the Update-IR state, the parallel outputs of the digital output pins are driven. (2) The boundary scan register is connected between JTDI and JTDO. (3) The Capture-DR state samples all digital inputs into the boundary scan register.

BYPASS. When the BYPASS instruction is latched into the parallel instruction register, JTDI is connected to JTDO through the 1-bit bypass register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

IDCODE. When the IDCODE instruction is latched into the parallel instruction register, the device identification register is selected. The device ID code is loaded into the device identification register on the rising edge of JTCLK, following entry into the Capture-DR state. Shift-DR can be used to shift the ID code out serially through JTDO. During Test-Logic-Reset, the ID code is forced into the instruction register's parallel output.

HIGHZ. All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

CLAMP. All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

6.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included in the device design. It is used with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Bypass Register. This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions to provide a short path between JTDI and JTDO.

Boundary Scan Register. This register contains a shift register path and a latched parallel output for control cells and digital I/O cells. BSDL files are available on the MAX24505/10 page of Microsemi's website.

Identification Register. This register contains a 32-bit shift register and a 32-bit latched parallel output. It is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. The device identification codes for the MAX24505 and MAX24510 are shown in Table 6-2.

Table 6-2. JTAG ID Code

DEVICE	REVISION	DEVICE CODE	MANUFACTURER CODE	REQUIRED
MAX24505	Contact factory	0000 0000 1100 0110	00010100001	1
MAX24510	Contact factory	0000 0000 1100 0111	00010100001	1

7. Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin with Respect to V_{SS} (except Power Supply Pins) .... -0.3V to +5.5V
Supply Voltage Range, Nominal 1.8V Supply with Respect to V_{SS} .... -0.3V to +1.98V
Supply Voltage Range, Nominal 3.3V Supply with Respect to V_{SS} .... -0.3V to +3.63V
Supply Voltage Range, VDDOx (x=A|B|C|D) with Respect to V_{SS} .... -0.3V to +3.63V
Ambient Operating Temperature Range .... -40°C to +85°C
Junction Operating Temperature Range .... -40°C to +125°C
Storage Temperature Range .... -55°C to +125°C
Soldering Temperature (reflow)
  Lead (Pb) free .... +260°C
  Containing lead (Pb)... +240°C

Stresses beyond those listed under *"Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device. Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.*

Note 1: The typical values listed in the tables of Section 7 are not production tested.
Note 2: Specifications to -40°C are guaranteed by design and not production tested.

Table 7-1. Recommended DC Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, Nominal 1.8V	VDD18		1.71	1.8	1.89	V
Supply Voltage, Nominal 3.3V	VDD33		3.135	3.3	3.465	V
Supply Voltage, VDDOx (x=A|B|C|D)	VDDOx		1.425	1.5, 1.8, 2.5, 3.3	3.465	V
Ambient Temperature Range	T_A		-40		+85	°C
Junction Temperature Range	T_J		-40		+125	°C

Table 7-2. Electrical Characteristics: Supply Currents

(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP[2]	MAX	UNITS
MAX24505 Total Current, All 1.8V Supply Pins	I_{DD18}	Note 1		264	325	mA
MAX24505 Total Current, All 3.3V Supply Pins	I_{DD33}	Note 1		246	305	mA
MAX24510 Total Current, All 1.8V Supply Pins	I_{DD18}	Note 1		369	455	mA
MAX24510 Total Current, All 3.3V Supply Pins	I_{DD33}	Note 1		327	408	mA
1.8V Supply Current Change from Enabling or Disabling APLL2	$\Delta I_{DD18APLL}$			50		mA
3.3V Supply Current Change from Enabling or Disabling APLL2	$\Delta I_{DD33APLL}$			75		mA
1.8V Supply Current Change from Enabling or Disabling a CML Output, Standard Swing	$\Delta I_{DD18CML}$			22		mA
3.3V Supply Current Change from Enabling or Disabling a CML Output, Standard Swing	$\Delta I_{DD33CML}$			16		mA
1.8V Supply Current Change from Enabling or Disabling a CML Output, Narrow Swing	$\Delta I_{DD18CMLN}$			22		mA
3.3V Supply Current Change from Enabling or Disabling a CML Output, Narrow Swing	$\Delta I_{DD33CMLN}$			8		mA
VDDO18x Supply Current Change from Enabling or Disabling a Pair of Single-Ended Outputs	$\Delta I_{DD18CMOS}$			8		mA
VDDOx Supply Current Change from Enabling or Disabling a Pair of Single-Ended Outputs	$\Delta I_{DD33CMOS}$			6		mA
1.8V Supply Current Change from Enabling or Disabling an Input Clock	ΔI_{DD18IN}			6		mA
1.8V Supply Current Change from Enabling or Disabling the Crystal Oscillator	$\Delta I_{DD18DFS}$			4		mA

Note 1: Max I_{DD} measurements made with all blocks enabled, 750MHz signals on both inputs, and all outputs enabled as CML outputs driving 750MHz signals.

Note 2: Typical values measured at 1.80V and 3.30V supply voltages and 25°C ambient temperature.

Note 3: Limits are 100% production tested at Ta = +25C and/or Ta = +85C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

Table 7-3. Electrical Characteristics: Non-Clock CMOS/TTL Pins

(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	Note 1	-10		10	µA
Input Leakage, Pins with Internal Pullup Resistor (50kΩ typ)	I_{ILPU}	Note 1	-85		10	µA
Input Leakage, Pins with Internal Pulldown Resistor (50kΩ typ)	I_{ILPD}	Note 1	-10		85	µA
Output Leakage (when High Impedance)	I_{LO}	Note 1	-10		10	µA
Output High Voltage	V_{OH}	I_O = -4.0mA	2.4			V
Output Low Voltage	V_{OL}	I_O = 4.0mA			0.4	V
Input Capacitance	C_{IN}			3		pF

Note 1: 0V < V_{IN} < VDD33 for all other digital inputs.

Table 7-4. Electrical Characteristics: Clock Inputs

(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Tolerance (ICPOS or ICNEG, Single-Ended)	V_{TOL}	Note 1	0		VDD33	V
Input Voltage Range, (ICPOS or ICNEG, Single-Ended)	V_{IN}	$\|V_{ID}\|$ = 100mV	0		2.4	V
Input Bias Voltage	V_{CMI}	Note 2		1.2		V
Input Differential Voltage	$\|V_{ID}\|$	Note 3	0.1		1.4	V
Input Frequency to APLL Mux	f_I	Differential	9.72		750	MHz
Input Frequency to APLL Mux	f_I	Single-Ended	9.72		160	MHz
Minimum Input Clock High, Low Time	t_H, t_L			smaller of 3ns or 0.3 x 1/ f_I		ns
Differential Input Capacitance	C_{ID}			1.5		pF

Note 1: The device can tolerate voltages as specified in V_{TOL} w.r.t. VSS on its ICxPOS and ICxNEG pins without being damaged.
For differential input signals, proper operation of the input circuitry is only guaranteed when the other specifications in this table, including V_{IN}, are met.
For single-ended signals, the input circuitry accepts signals that meet the V_{IH} and V_{IL} specifications in Table 7-3 above (but with V_{IH} max of VDD33).

Note 2: See internal resistors in Figure 7-1. Other common mode voltages can be set using external resistors.

Note 3: $V_{ID}=V_{ICPOS} - V_{ICNEG}$

Note 4: The differential inputs can easily be interfaced to LVDS, LVPECL, and CML outputs on neighboring ICs using a few external passive components. See Figure 7-1 and App Note HFAN-1.0 for details.

Figure 7-1. Recommended External Components for Interfacing to Differential Inputs

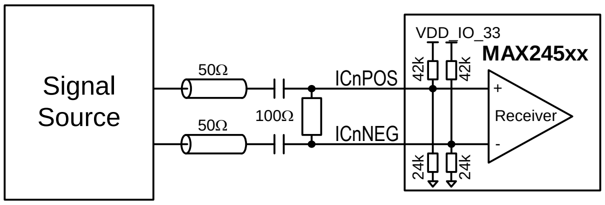


Table 7-5. Electrical Characteristics: CML Clock Outputs

(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, VDDOx = 3.3V±5% (x=A|B|C|D); T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	f_{OCML}		<1Hz[2]		750	MHz
Output High Voltage (OCPOS or OCNEG, Singled-Ended)	$V_{OH,S}$	Standard Swing (OCCR2.OCSF=1), AC coupled to 50Ω termination		VDDOx – 0.2		V
Output Low Voltage (OCPOS or OCNEG, Singled-Ended)	$V_{OL,S}$			VDDOx – 0.6		V
Output Common Mode Voltage	$V_{CM,S}$			VDDOx – 0.4		V
Differential Output Voltage	$\|V_{OD,S}\|$		320	400	500	mV
Differential Output Voltage Peak-to-Peak	$\|V_{OD,S,PP}\|$		640	800	1000	mV_{P-P}
Output High Voltage (OCPOS or OCNEG, Singled-Ended)	$V_{OH,N}$	Narrow Swing (half the power) (OCCR2.OCSF=2), AC coupled to 50Ω termination		VDDOx – 0.1		V
Output Low Voltage (OCPOS or OCNEG, Singled-Ended)	$V_{OL,N}$			VDDOx – 0.3		V
Output Common Mode Voltage	$V_{CM,N}$			VDDOx – 0.2		V
Differential Output Voltage	$\|V_{OD,N}\|$		160	200	250	mV
Differential Output Voltage Peak-to-Peak	$\|V_{OD,N,PP}\|$		320	400	500	mV_{P-P}
Difference in Magnitude of Differential Voltage for Complementary States	V_{DOS}				50	mV
Output Rise/Fall Time	t_R, t_F	20%-80%		150		ps
Output Duty-Cycle		Notes 2	45	50	55	%
Output Duty-Cycle		Notes 3	40		60	%
Output Impedance	R_{OUT}	Single Ended, to VDDOx		50		Ω
Mismatch in a pair	ΔR_{OUT}				10	%

Note 1: The differential CML outputs can easily be interfaced to LVDS, LVPECL, and CML outputs on neighboring ICs using a few external passive components. See Figure 7-2 and App Note HFAN-1.0 for details.

Note 2: For all HSDIV, MSDIV and OCDIV combinations other than those specified in Note 3.

Note 3: For the case when APLLCR1.HSDIV specifies a half divide and OCCR1.MSDIV=0 and OCDIV=0.

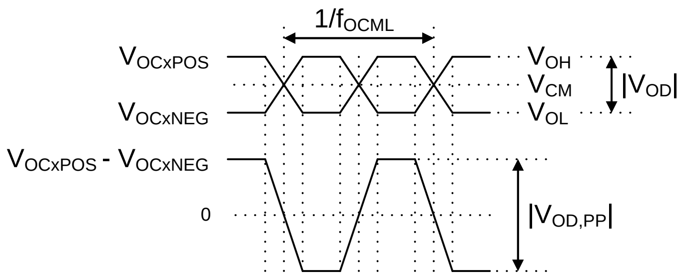


Figure 7-2. Recommended External Components for Interfacing to CML Outputs

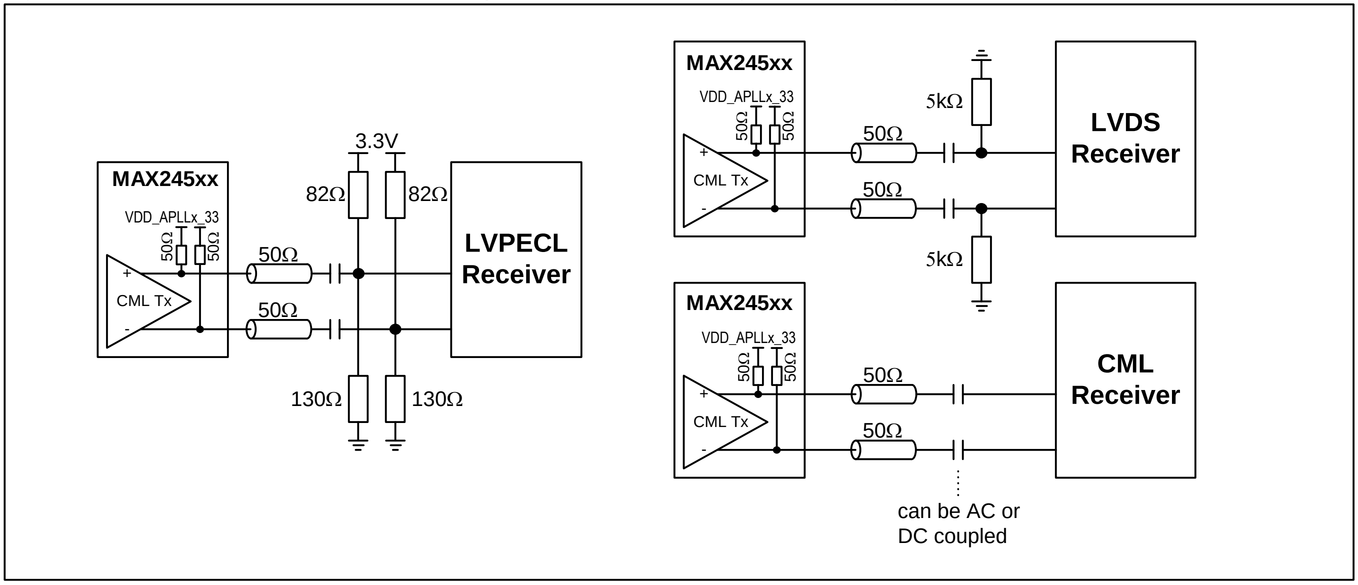


Table 7-6. Electrical Characteristics: CMOS and HSTL (Class I) Clock Outputs

(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, VDDOx = 1.425V to 3.465V (x=A|B|C|D);T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	f_{OCML}		<<1Hz[1]		160	MHz
Output High Voltage	V_{OH}	Notes 3, 4	VDDOx –0.4		VDDOx	V
Output Low Voltage	V_{OL}	Notes 3, 4	0		0.4	V
Output Rise/Fall Time, VDDOx=1.8V, OCCR2.DRIVE=4x	t_R, t_F	2pF load		0.4		ns
Output Rise/Fall Time, VDDOx=1.8V, OCCR2.DRIVE=4x	t_R, t_F	15pF load		1.2		ns
Output Rise/Fall Time, VDDOx=3.3V, OCCR2.DRIVE=1x	t_R, t_F	2pF load		0.7		ns
Output Rise/Fall Time, VDDOx=3.3V, OCCR2.DRIVE=1x	t_R, t_F	15pF load		2.2		ns
Output Duty-Cycle			45	50	55	%
Output Current When Output Disabled		OCCR2.OCSF=0		10		µA

Note 1: Guaranteed by design.

Note 2: Measured with a series resistor of 33Ω and a 10pF load capacitance unless otherwise specified.

Note 3: For HSTL Class I, V_{OH} and V_{OL} apply for both unterminated loads and for symmetrically terminated loads, i.e. 50Ω to VDDOx/2.

Note 4: For VDDOx=3.3V and OCCR2.DRIVE=1x, I_O=4mA. For VDDOx=1.5V and OCCR2.DRIVE=4x, I_O=8mA.

Interfacing to HCSL Components

Outputs in HSTL mode with VDDOx=1.5V or VDDOx=1.8V can provide an HCSL signal (V_{OH} typ. 0.75V) to a neighboring component when configured as shown in Figure 7-3 For VDDOx=1.5V the value of R_S should be set to 30Ω and OCCR2.DRIVE should be set to 4x. For VDDOx=1.8V the value of R_S should be set to 20Ω and OCCR2.DRIVE should be set to 2x.

Figure 7-3. Recommended Confguration for Interfacing to HCSL Components

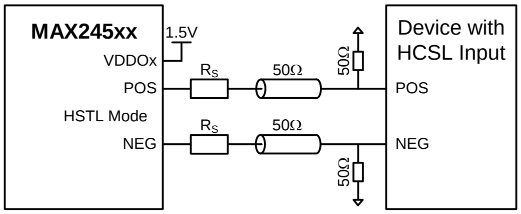


Table 7-7. Electrical Characteristics: Clock Output Timing

(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
APLL VCO Frequency Range	f_{VCO}		3715		4180	MHz
APLL Phase-Frequency Detector Compare Frequency	t_{PFD}		9.72		102.4	MHz

Table 7-8. Electrical Characteristics: Jitter Specifications

(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Jitter, 622.08MHz		Notes 1, 3		0.19	0.35	ps RMS
Jitter Transfer Bandwidth		Note 2		400		kHz

Note 1: Jitter calculated from integrated phase noise from 12kHz to 20MHz.

Note 2: APLL bandwidth and damping factor can be field configured over a limited range. Contact the factory for details.

Note 3: Tested with 77.76MHz from production tester, 3732.48MHz VCO frequency.

Table 7-9. Electrical Characteristics: Typical Output Jitter Performance

APLL Locked to External 78.125MHz XO (Vectron VCC1-1540-78M12500)			
APLL1 Output Frequency	**Output Jitter ps RMS**	**APLL2 Output Frequency**	**Output Jitter ps RMS**
625MHz	0.18	APLL2 Disabled	
156.25MHz	0.23		
125MHz	0.27		
25MHz CMOS	0.34		
622.08MHz	0.28		
155.52MHz	0.35		
622.08MHz * 255/237	0.30		
155.52MHz * 255/237	0.36		
614.4MHz	0.29		
153.6MHz	0.33		
625MHz	0.19	622.08MHz	0.27
156.25MHz	0.24	155.52MHz	0.38
156.25MHz	0.23	156.25MHz * 66/64	0.38

Note: All signals in Table 7-9 are differential unless otherwise stated. Jitter is integrated 12kHz to 5MHz for 25MHz output frequency and 12kHz to 20MHz for all other output frequencies.

Table 7-10. Electrical Characteristics: Typical Input-to-Output Clock Delay

(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

MODE	DELAY, INPUT CLOCK EDGE TO OUTPUT CLOCK EDGE
All Modes	non-deterministic but constant as long as the APLL remains locked and alignment is not changed by the APLLCR1.DALIGN and OCCR3.DALEN bits.

Table 7-11. Electrical Characteristics: Typical Output-to-Output Clock Delay

(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

MODE	DELAY, OUTPUT CLOCK EDGE TO OUTPUT CLOCK EDGE
All Modes	<100ps Requires use of APLLCR1.DALIGN and OCCR3.DALEN bits. See the register field descriptions for details.

Table 7-12. Electrical Characteristics: SPI Interface Timing

(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C) (See Figure 7-4.)

PARAMETER (Note 1, 2)	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{BUS}				4	MHz
SCLK Cycle Time	t_{CYC}		250			ns
CS_N Setup to First SCLK Edge	t_{SUC}		125			ns
CS_N Hold Time After Last SCLK Edge	t_{HDC}		125			ns
SCLK High Time	t_{CLKH}		100			ns
SCLK Low Time	t_{CLKL}		100			ns
SDI Data Setup Time	t_{SUI}		30			ns
SDI Data Hold Time	t_{HDI}		40			ns
SDO Enable Time (High-Impedance to Output Active)	t_{EN}		0			ns
SDO Disable Time (Output Active to High-Impedance)	t_{DIS}				25	ns
SDO Data Valid Time	t_{DV}				100	ns
SDO Data Hold Time After Update SCLK Edge	t_{HDO}		5			ns

Note 1: All timing is specified with 100pF load on all SPI pins.
Note 2: All parameters in this table are guaranteed by design.

Figure 7-4. SPI Interface Timing Diagram

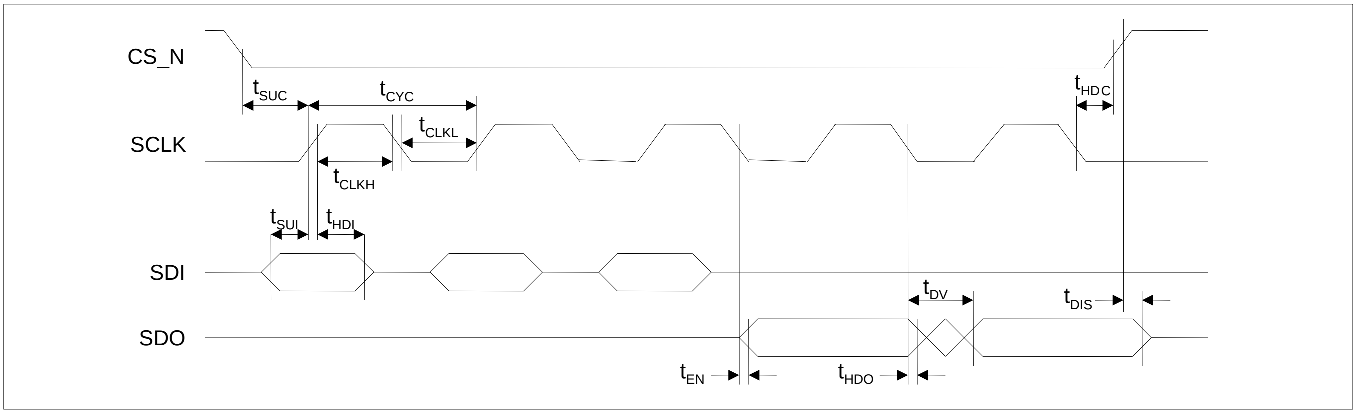


Table 7-13. Electrical Characteristics: JTAG Interface Timing

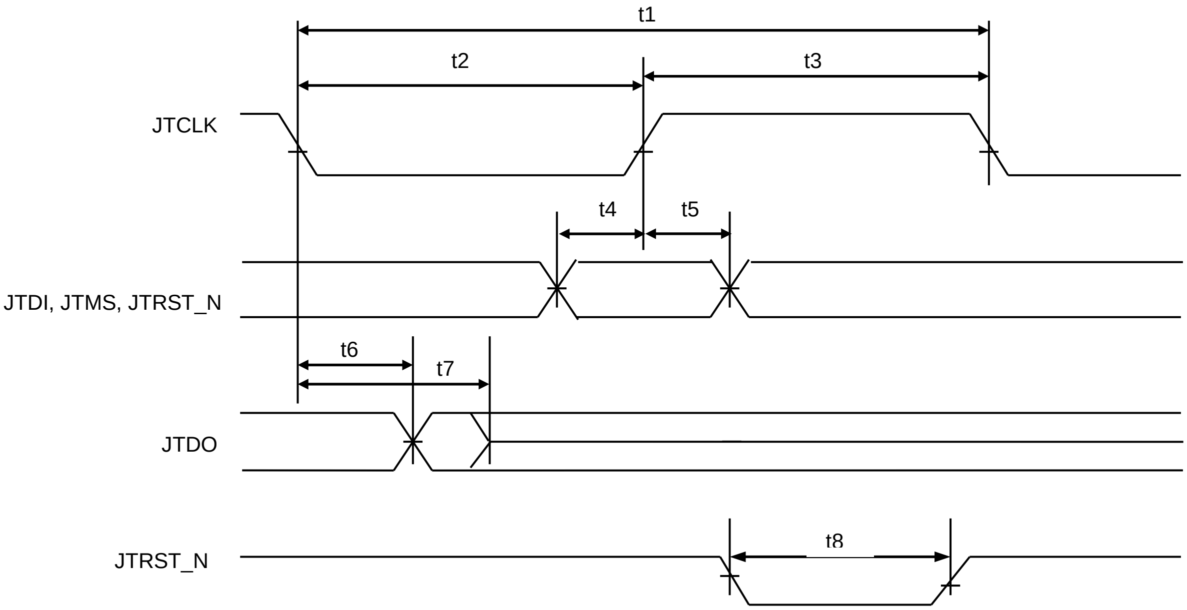
(1.8V Supplies: 1.8V ±5%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C) (See Figure 7-5.)

PARAMETER (Note 1)	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JTCLK Clock Frequency	f_{JTAG}				15.625	MHz
JTCLK Clock Period	t1		64			ns
JTCLK Clock High/Low Time	t2/t3	Note 2	32			ns
JTCLK to JTDI, JTMS Setup Time	t4		16			ns
JTCLK to JTDI, JTMS Hold Time	t5		16			ns
JTCLK to JTDO Delay	t6		2		16	ns
JTCLK to JTDO High-Impedance Delay	t7		2		16	ns
JTRST_N Width Low Time	t8		100			ns

Note 1: All parameters in this table are guaranteed by design.

Note 2: Clock can be stopped high or low.

Figure 7-5. JTAG Timing Diagram



8. Pin Assignments

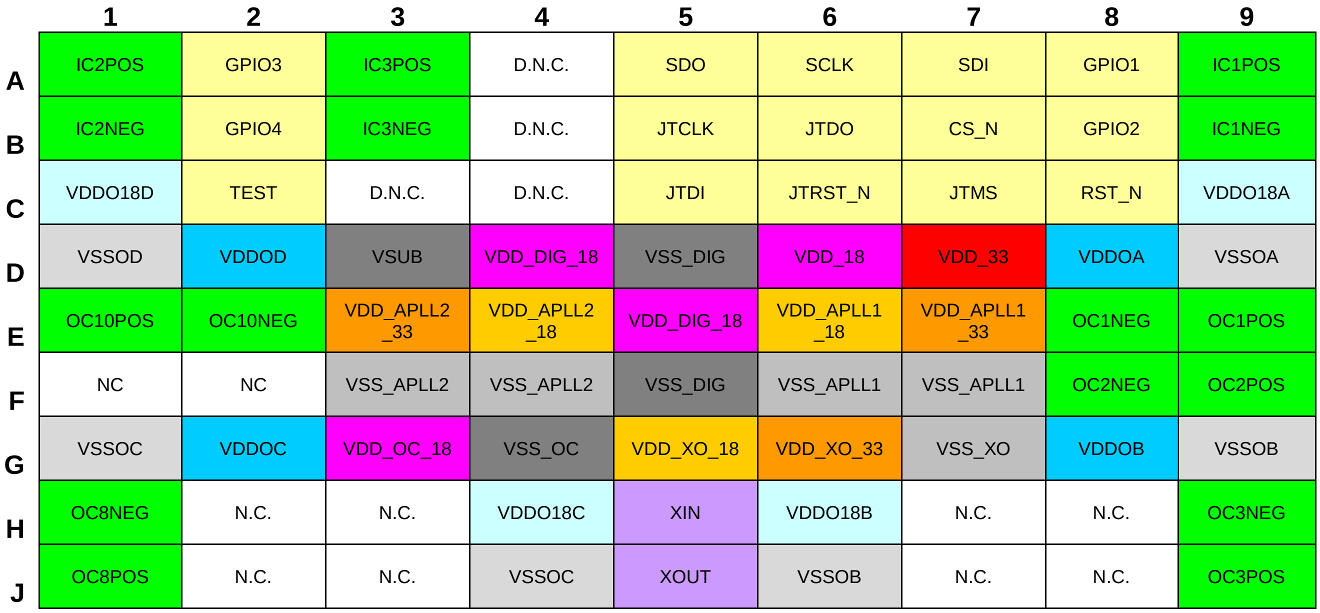
8.1 MAX24505 Pin Asssignment

Table 8-1 below lists pin assignments sorted in alphabetical order by pin name. Figure 8-1 shows pin assignments arranged by pin number.

Table 8-1. MAX24505 Pin Assignments Sorted by Signal Name

PIN NAME	PIN NUMBERS
CS_N	B7
GPIO1	A8
GPIO2	B8
GPIO3	A2
GPIO4	B2
IC1NEG	B9
IC1POS	A9
IC2NEG	B1
IC2POS	A1
IC3NEG	B3
IC3POS	A3
JTCLK	B5
JTDI	C5
JTDO	B6
JTMS	C7
JTRST_N	C6
OC1NEG	E8
OC1POS	E9
OC2NEG	F8
OC2POS	F9
OC3NEG	H9
OC3POS	J9
OC8NEG	H1
OC8POS	J1
OC10NEG	E2
OC10POS	E1
RST_N	C8
SCLK	A6
SDI	A7
SDO	A5
TEST	C2
VDD_18	D6
VDD_33	D7
VDD_APLL1_18	E6
VDD_APLL1_33	E7
VDD_APLL2_18	E4
VDD_APLL2_33	E3
VDD_DIG_18	D4, E5
VDD_OC_18	G3
VDD_XO_18	G5
VDD_XO_33	G6
VDDO18A	C9
VDDO18B	H6
VDDO18C	H4
VDDO18D	C1
VDDOA	D8
VDDOB	G8
VDDOC	G2
VDDOD	D2
VSS_APLL1	F6, F7
VSS_APLL2	F3, F4
VSS_DIG	D5, F5
VSS_OC	G4
VSS_XO	G7
VSSOA	D9
VSSOB	G9, J6
VSSOC	G1, J4
VSSOD	D1
VSUB	D3
XIN	H5
XOUT	J5
N.C.	F1, F2, H2, H3, H7, H8, J2, J3, J7, J8
D.N.C.	A4, B4, C3, C4

Figure 8-1. MAX24505 Pin Assignment Diagram



	1	2	3	4	5	6	7	8	9
A	IC2POS	GPIO3	IC3POS	D.N.C.	SDO	SCLK	SDI	GPIO1	IC1POS
B	IC2NEG	GPIO4	IC3NEG	D.N.C.	JTCLK	JTDO	CS_N	GPIO2	IC1NEG
C	VDDO18D	TEST	D.N.C.	D.N.C.	JTDI	JTRST_N	JTMS	RST_N	VDDO18A
D	VSSOD	VDDOD	VSUB	VDD_DIG_18	VSS_DIG	VDD_18	VDD_33	VDDOA	VSSOA
E	OC10POS	OC10NEG	VDD_APLL2_33	VDD_APLL2_18	VDD_DIG_18	VDD_APLL1_18	VDD_APLL1_33	OC1NEG	OC1POS
F	NC	NC	VSS_APLL2	VSS_APLL2	VSS_DIG	VSS_APLL1	VSS_APLL1	OC2NEG	OC2POS
G	VSSOC	VDDOC	VDD_OC_18	VSS_OC	VDD_XO_18	VDD_XO_33	VSS_XO	VDDOB	VSSOB
H	OC8NEG	N.C.	N.C.	VDDO18C	XIN	VDDO18B	N.C.	N.C.	OC3NEG
J	OC8POS	N.C.	N.C.	VSSOC	XOUT	VSSOB	N.C.	N.C.	OC3POS

🟩 Differential I/O (up to 750MHz)
🟨 Low-Speed Digital I/O (≤10MHz)
🟥 VDD 3.3V
🟪 VDD 1.8V
⬛ VSS
🟧 APLL or XO VDD 3.3V
🟨 APLL or XO VDD 1.8V
▩ APLL or XO VSS
🟦 Output VDD 1.5-3.3V
▢ Output VDD 1.8V
▒ Output VSS
🟪 Crystal I/O
⬜ N.C. = No Connection. Lead is not connected to anything inside the device
D.N.C. = Do Not Connect. Lead is internally connected. Do not connect anything to this lead.

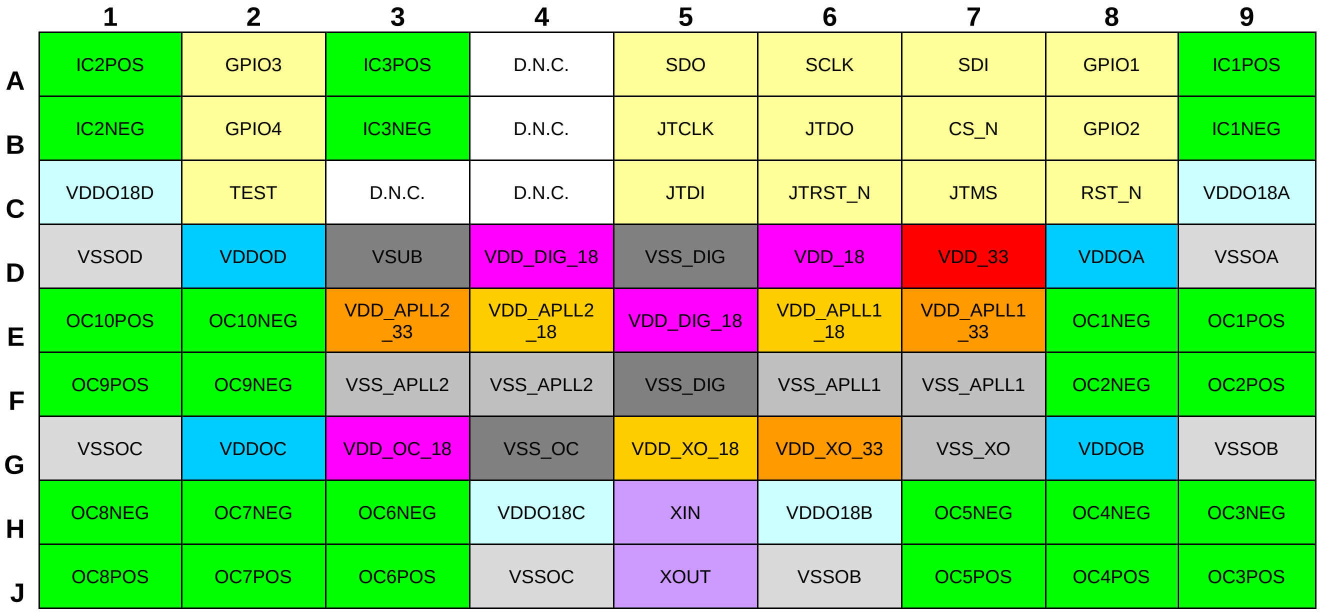
8.2 MAX24510 Pin Asssignment

Table 8-2 below lists pin assignments sorted in alphabetical order by pin name. Figure 8-2 shows pin assignments arranged by pin number.

Table 8-2. MAX24510 Pin Assignments Sorted by Signal Name

PIN NAME	PIN NUMBERS
CS_N	B7
GPIO1	A8
GPIO2	B8
GPIO3	A2
GPIO4	B2
IC1NEG	B9
IC1POS	A9
IC2NEG	B1
IC2POS	A1
IC3NEG	B3
IC3POS	A3
JTCLK	B5
JTDI	C5
JTDO	B6
JTMS	C7
JTRST_N	C6
OC1NEG	E8
OC1POS	E9
OC2NEG	F8
OC2POS	F9
OC3NEG	H9
OC3POS	J9
OC4NEG	H8
OC4POS	J8
OC5NEG	H7
OC5POS	J7
OC6NEG	H3
OC6POS	J3
OC7NEG	H2
OC7POS	J2
OC8NEG	H1
OC8POS	J1
OC9NEG	F2
OC9POS	F1
OC10NEG	E2
OC10POS	E1
RST_N	C8
SCLK	A6
SDI	A7
SDO	A5
TEST	C2
VDD_18	D6
VDD_33	D7
VDD_APLL1_18	E6
VDD_APLL1_33	E7
VDD_APLL2_18	E4
VDD_APLL2_33	E3
VDD_DIG_18	D4, E5
VDD_OC_18	G3
VDD_XO_18	G5
VDD_XO_33	G6
VDDO18A	C9
VDDO18B	H6
VDDO18C	H4
VDDO18D	C1
VDDOA	D8
VDDOB	G8
VDDOC	G2
VDDOD	D2
VSS_APLL1	F6, F7
VSS_APLL2	F3, F4
VSS_DIG	D5, F5
VSS_OC	G4
VSS_XO	G7
VSSOA	D9
VSSOB	G9, J6
VSSOC	G1, J4
VSSOD	D1
VSUB	D3
XIN	H5
XOUT	J5
D.N.C.	A4, B4, C3, C4
N.C.	none

Figure 8-2. MAX24510 Pin Assignment Diagram



	1	2	3	4	5	6	7	8	9
A	IC2POS	GPIO3	IC3POS	D.N.C.	SDO	SCLK	SDI	GPIO1	IC1POS
B	IC2NEG	GPIO4	IC3NEG	D.N.C.	JTCLK	JTDO	CS_N	GPIO2	IC1NEG
C	VDDO18D	TEST	D.N.C.	D.N.C.	JTDI	JTRST_N	JTMS	RST_N	VDDO18A
D	VSSOD	VDDOD	VSUB	VDD_DIG_18	VSS_DIG	VDD_18	VDD_33	VDDOA	VSSOA
E	OC10POS	OC10NEG	VDD_APLL2_33	VDD_APLL2_18	VDD_DIG_18	VDD_APLL1_18	VDD_APLL1_33	OC1NEG	OC1POS
F	OC9POS	OC9NEG	VSS_APLL2	VSS_APLL2	VSS_DIG	VSS_APLL1	VSS_APLL1	OC2NEG	OC2POS
G	VSSOC	VDDOC	VDD_OC_18	VSS_OC	VDD_XO_18	VDD_XO_33	VSS_XO	VDDOB	VSSOB
H	OC8NEG	OC7NEG	OC6NEG	VDDO18C	XIN	VDDO18B	OC5NEG	OC4NEG	OC3NEG
J	OC8POS	OC7POS	OC6POS	VSSOC	XOUT	VSSOB	OC5POS	OC4POS	OC3POS

🟩 Differential I/O (up to 750MHz)
🟨 Low-Speed Digital I/O (≤10MHz)
🟥 VDD 3.3V
🟪 VDD 1.8V
⬛ VSS
🟧 APLL or XO VDD 3.3V
🟨 APLL or XO VDD 1.8V
▨ APLL or XO VSS
🟦 Output VDD 1.5-3.3V
🟦 Output VDD 1.8V
▨ Output VSS
🟪 Crystal I/O
☐ N.C. = No Connection. Lead is not connected to anything inside the device
D.N.C. = Do Not Connect. Lead is internally connected. Do not connect anything to this lead.

9. Package and Thermal Information

For the latest package outline information and land patterns contact Microsemi timing products technical support.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN
81 CSBGA	X8100M+4	21-0360	See IPC-7351

9.1 Package Top Mark Format

Figure 9-1. Non-Customized Device Top Mark

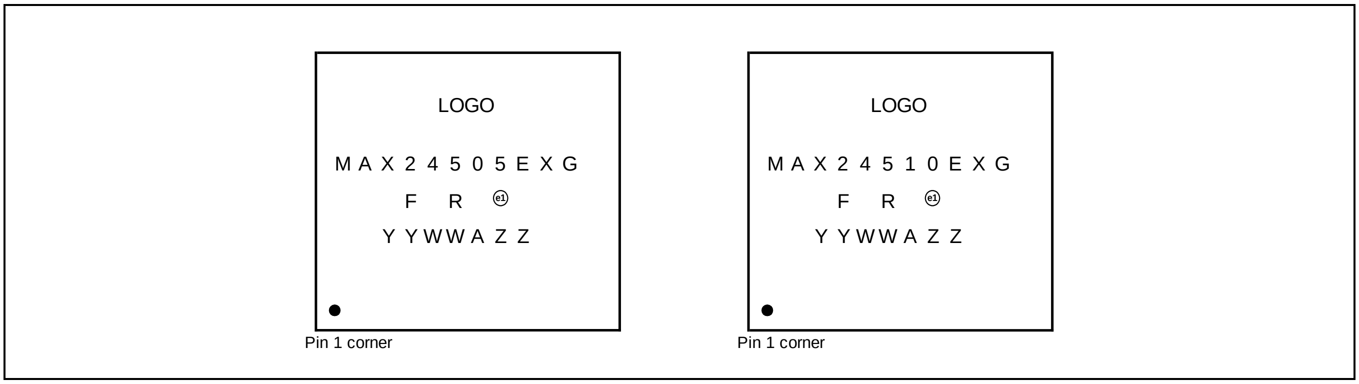


Figure 9-2. Custom Factory-Programmed Device Top Mark

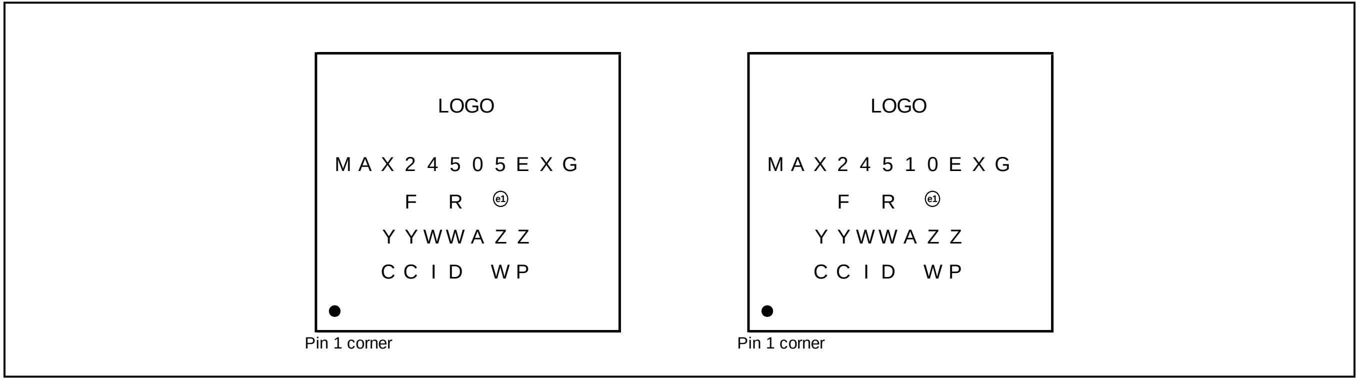


Table 9-1. Package Top Mark Legend

Line	Characters	Description
1	MAX24505EXG or MAX24510EXG	Part Number
2	F	Fab Code
2	R	Product Revision Code
2	e1	Denotes Pb-Free Package
3	YY	Last Two Digits of the Year of Encapsulation
3	WW	Work Week of Assembly
3	A	Assembly Location Code
3	ZZ	Assembly Lot Sequence Code
4	CCID	Custom Programming Identification Code
4	WP	Work Week of Programming

9.2 Thermal Specifications

Table 9-2. CSBGA Package Thermal Properties

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Minimum Ambient Temperature	T_A		-40	°C
Maximum Ambient Temperature	T_A		85	°C
Minimum Junction Temperature	T_J		-40	°C
Maximum Junction Temperature	T_J		125	°C
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	still air,	24.9	°C/W
		1m/s airflow	22.7	
		2m/s airflow	21.9	
Junction to Board Thermal Resistance	θ_{JB}		14.1	°C/W
Junction to Case Thermal Resistance	θ_{JC}		4.1	°C/W
Junction to Top-Center Thermal Characterization Parameter	ψ_{JT}	still air,	0.3	°C/W
		1m/s airflow	0.4	
		2m/s airflow	0.4	

Note 1: Theta-JA (θ_{JA}) is the junction to ambient thermal resistance when the package is mounted on a six-layer JEDEC standard test board and dissipating maximum power.

If the maximum ambient temperature seen by the device in the application is greater than 70°C then care must be taken to keep the device's junction temperature below the 125°C max specification. In this case CML outputs should be configured for half-swing mode whenever possible, and air flow may be required, depending on which blocks in the device are enabled in the application. Microsemi offers the MAX24xxx Power and Thermal Calculator spreadsheet to calculate typical and worst-case power consumption and device junction temperature. Contact Microsemi applications support to request this spreadsheet.

10. Acronyms and Abbreviations

APLL	analog phase locked loop
CML	current mode logic
EEC	Ethernet equipment clock
GbE	gigabit Ethernet
I/O	input/output
LVDS	low-voltage differential signal
LVPECL	low-voltage positive emitter-coupled logic
PFD	phase/frequency detector
PLL	phase locked loop
ppb	parts per billion
ppm	parts per million
pk-pk	peak-to-peak
RMS	root-mean-square
RO	read-only
R/W	read/write
SDH	synchronous digital hierarchy
SEC	SDH equipment clock
SONET	synchronous optical network
STM	synchronous transport module
TCXO	temperature-compensated crystal oscillator
UI	unit interval
UI_{PP} or UI_{P-P}	unit interval, peak to peak
XO	crystal oscillator

11. Data Sheet Revision History

REVISION DATE	DESCRIPTION
2012-05	Initial Release
2012-06	Updated page 1 and section 2.1 statements about output jitter to say 0.35-0.5ps RMS typical.
2012-07	Corrected several typos (no effect on electrical specs or behavior).
2012-08	Change Note 1 below Figure 4-1 to discuss final R1 and R2 values. Changed Table 7-7 to show final VCO range rather than rev A1 VCO range.
2012-11	Updated Table 9-2 to latest θ_{JA} numbers and added θ_{JB}, θ_{JC}, and ψ_{JT} numbers.
2013-02	On page 1 and in section 2.1, reduced jitter numbers from “0.35 to 0.5ps and as low as 0.24ps” to “typically 0.18 to 0.3ps RMS for an integer multiply and 0.25 to 0.4ps RMS for a fractional multiply” In section 2.3, deleted “Internal compensation for local oscillator frequency error” bullet. In section Table 7-8 changed typical APLL jitter transfer bandwidth from 200kHz to 400kHz. In Table 7-7 changed VCO range from 3700MHz min, 4200MHz max to 3715MHz min, 4180MHz max. In Table 7-8, changed output jitter max from 0.5 to 0.35ps RMS and changed VCO frequency in Note 3 from 4043.52MHz to 3732.48MHz. In Table 7-9 revised all numbers lower and specified XO used for rev B jitter measurement. Added 49.152MHz to Note 1 of Table 4-1.
2013-05	In section 9 replaced the land pattern hyperlink with the recommendation to see IPC-7351.
2013-07	In Table 7-8 reduced the output jitter spec from “0.23 typ, 0.48 max” to “0.19 typ, 0.35 max.” In the heading of Table 7-9 changed “50MHz” to “78.125MHz.” The old values were typos.
2014-08	In the JTRST_N pin description in Table 3-5 specified that JTRST_N should be held low during device power-up. Changed title to Any-to-Any. In Table 7-5 changed differential output voltage symbols (regular and peak-to-peak) to have abosolute value bars and added definition figure below the table.
2014-10	In Table 7-6 corrected typo: changed VCCOx to VDDOx. Added section 9.1 to document package top mark.
2015-06	Above Table 7-7 in the *Interfacing to HCSL Components* paragraph, added component values and settings for VDDOx=1.8V. In Table 7-5 deleted the max rise/fall time number. This was erroneously left in this data sheet but should not have been there from first data sheet release as is the case in other MAX24xxx family data sheets.
2016-11	In Table 7-13 updated JTAG interface timing from 1MHz to 15.625MHz.
2019-04	Change "+" to "2" in ordering part numbers.

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