Rail-to-Rail High Output Current Operational Amplifiers

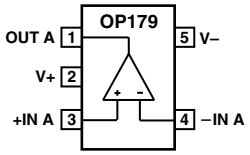
OP179/OP279

FEATURES
Rail-to-Rail Inputs and Outputs
High Output Current: ±60 mA
Single Supply: 5 V to 12 V
Wide Bandwidth: 5 MHz
High Slew Rate: 3 V/μs
Low Distortion: 0.01%
Unity-Gain Stable
No Phase Reversal
Short-Circuit Protected
Drives Capacitive Loads: 10 nF

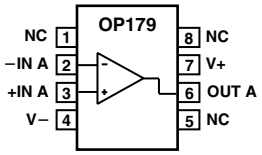
APPLICATIONS
Multimedia
Telecom
DAA Transformer Driver
LCD Driver
Low Voltage Servo Control
Modems
FET Drivers

PIN CONFIGURATIONS

5-Lead SOT-23-5
(RT-5)

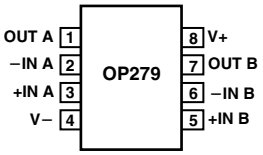


8-Lead SOIC
(S Suffix)



NC = NO CONNECT

8-Lead SOIC and TSSOP
SO-8 (S) and RU-8



GENERAL DESCRIPTION

The OP179 and OP279 are rail-to-rail, high output current, single-supply amplifiers. They are designed for low voltage applications that require either current or capacitive load drive capability. The OP179/OP279 can sink and source currents of ±60 mA (typical) and are stable with capacitive loads to 10 nF.

Applications that benefit from the high output current of the OP179/OP279 include driving headphones, displays, transformers and power transistors. The powerful output is combined with a unique input stage that maintains very low distortion with wide common-mode range, even in single supply designs.

The OP179/OP279 can be used as a buffer to provide much greater drive capability than can usually be provided by CMOS outputs. CMOS ASICs and DAC often have outputs that can swing to both the positive supply and ground, but cannot drive more than a few milliamps.

Bandwidth is typically 5 MHz and the slew rate is 3 V/μs, making these amplifiers well suited for single supply applications that require audio bandwidths when used in high gain configurations. Operation is guaranteed from voltages as low as 4.5 V, up to 12 V.

Very good audio performance can be attained when using the OP179/OP279 in 5 volt systems. THD is below 0.01% with a 600 Ω load, and noise is a respectable 21 nV/$\sqrt{\text{Hz}}$. Supply current is less than 3.5 mA per amplifier.

The single OP179 is available in the 5-lead SOT-23-5 package. It is specified over the industrial (–40°C to +85°C) temperature range.

The OP279 is available in 8-lead TSSOP and SO-8 surface mount packages. They are specified over the industrial (–40°C to +85°C) temperature range.

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OP179/OP279–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = 5.0 V, V_{CM} = 2.5 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
OP179	V_{OS}	V_{OUT} = 2.5 V			±5	mV
OP279	V_{OS}	V_{OUT} = 2.5 V			±4	mV
Input Bias Current	I_B	V_{OUT} = 2.5 V, T_A = 25°C			±300	nA
		V_{OUT} = 2.5 V			±700	nA
Input Offset Current	I_{OS}	V_{OUT} = 2.5 V, T_A = 25°C			±50	nA
		V_{OUT} = 2.5 V			±100	nA
Input Voltage Range	V_{CM}		0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	56	66		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, 0.3 V ≤ V_{OUT} ≤ 4.7 V	20			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA Source	+4.8			V
Output Voltage Low	V_{OL}	I_L = 10 mA Sink, T_A = 25°C			75	mV
		I_L = 10 mA Sink			100	mV
Short-Circuit Limit	I_{SC}	T_A = 25°C	±40			mA
Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		22		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to 12 V	70	88		dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 2.5 V			3.5	mA
Supply Voltage Range	V_S		+4.5		+12	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 kΩ, 1 nF		3		V/µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			60		Degrees
Capacitive Load Drive		No Oscillation		10		nF
AUDIO PERFORMANCE						
Total Harmonic Distortion	THD			0.01		%
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz

ELECTRICAL SPECIFICATIONS (@ V_S = ±5.0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
OP179	V_{OS}	V_{OUT} = 0			±5	mV
OP279	V_{OS}	V_{OUT} = 0			±4	mV
Input Bias Current	I_B	T_A = 25°C			±300	nA
					±700	nA
Input Offset Current	I_{OS}	T_A = 25°C			±50	nA
					±100	nA
Input Voltage Range	V_{CM}		–5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –5 V to +5 V	56	66		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, –4.7 V ≤ V_{OUT} ≤ 4.7 V	20			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA Source	+4.8			V
Output Voltage Low	V_{OL}	I_L = 10 mA Sink			–4.85	V
Short Circuit Limit	I_{SC}	T_A = 25°C	±50			mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		22		Ω
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	V_S = ±6 V, V_{OUT} = 0 V			3.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 kΩ, 1 nF		3		V/µs
Full-Power Bandwidth	BW_p	1% Distortion				kHz
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			69		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz
Current Noise Density	i_n			1		pA/√Hz

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . 16 V
Input Voltage . . . . . 16 V
Differential Input Voltage[1] . . . . . ±1 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
S, RT, RU Package . . . . . –65°C to +150°C
Operating Temperature Range
OP179G/OP279G . . . . . –40°C to +85°C
Junction Temperature Range
S, RT, RU Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

Package Types	θ_{JA}[2]	θ_{JC}	Unit
5-Lead SOT-23 (RT)	256	81	°C/W
8-Lead SOIC (S)	158	43	°C/W
8-Lead TSSOP (RU)	240	43	°C/W

NOTES
[1]The inputs are clamped with back-to-back diodes. If the differential input voltage exceeds 1 volt, the input current should be limited to 5 mA.
[2]θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for SOIC packages.

ORDERING GUIDE

Package	Temperature Range	Package Description	Package Option	Brand Code
OP179GRT	–40°C to +85°C	5-Lead SOT-23	RT-5	A2G
OP279GS	–40°C to +85°C	8-Lead SOIC	SO-8	
OP279GRU	–40°C to +85°C	8-Lead TSSOP	RU-8	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP179/OP279 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OP179/OP279 Spice Macro Model

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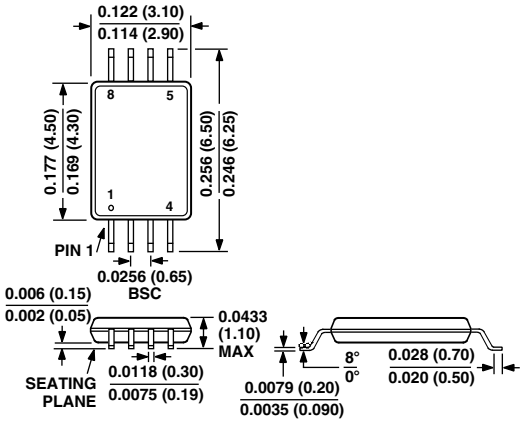
* OP179/OP279 SPICE Macro Model                Rev. A, 5/94
*                                ARG / ADI
*
* Copyright 1994 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of
* this model indicates your acceptance of the terms and pro-
* visions in the License Statement.
*
* Node assignments
*                          noninverting input
*                          |    inverting input
*                          |    |    positive supply
*                          |    |    |    negative supply
*                          |    |    |    |    output
*                          |    |    |    |    |
.SUBCKT OP179/OP279  3    2    99   50   45
*
* INPUT STAGE AND POLE AT 6 MHz
*
I1      1       50      60.2E-6
Q1      5       2       7 QN
Q2      6       4       8 QN
D1      4       2       DX
D2      2       4       DX
R1      1       7       1.628E3
R2      1       8       1.628E3
R3      5       99      2.487E3
R4      6       99      2.487E3
C1      5       6       5.333E-12
EOS     4       3       POLY(1) (16,39) 0.25E-3 50.118
IOS     2       3       5E-9
GB1     2       98      (24,98) 100E-9
GB2     4       98      (24,98) 100E-9
CIN     2       3       1E-12
*
* GAIN STAGE AND DOMINANT POLE AT 16 Hz
*
EREF    98      0       (39,0) 1
G1      98      9       (5,6) 402.124E-6
R7      9       98      497.359E6
C2      9       98      20E-12
V1      99      10      0.58
V2      11      50      0.47
D5      9       10      DX
D6      11      9       DX
*
* COMMON-MODE STAGE WITH ZERO AT 10 kHz
*
ECM     15      98      POLY(2) (3,39) (2,39) 0 0.5 0.5
R9      15      16      1E6
R10     16      98      10
C3      15      16      15.915E-12
*
* ZERO AT 1.5 MHz
*
E1      14      98      (9,39) 1E6
R5      14      18      1E6
R6      18      98      1
C4      14      18      106.103E-15
*
* BIAS CURRENT-VS-COMMON-MODE VOLTAGE
*
EP      97      0       (99,0) 1
EN      51      0       (50,0) 1
V3      20      21      1.6
V4      22      23      2.8
R12     97      20      530
R13     23      51      1E3
D13     15      21      DX
D14     22      15      DX
FIB     98      24      POLY(2) V3 V4 0 –1 1
RIB     24      98      10E3
E3      97      25      POLY(1) (99,39) –1.63 1
E4      26      51      POLY(1) (39,50) –2.73 1
D15     24      25      DX
D16     26      24      DX
*
* POLE AT 6 MHz
*
G6      98      40      (18,39)      1E      6
R20     40      98      1E6
C10     40      98      26.526E-15
*
* OUTPUT STAGE
*
RS1     99      39      6.0345E3
RS2     39      50      6.0345E3
RO1     99      45      40
RO2     45      50      40
G7      45      99      (99,40) 25E-3
G8      50      45      (40,50) 25E-3
G9      98      60      (45,40) 25E-3
D9      60      61      DX
D10     62      60      DX
V7      61      98      DC      0
V8      98      62      DC 0
FSY     99      50      POLY(2) V7 V8 1.711E-3   1   1
D11     41      45      DZ
D12     45      42      DZ
V5      40      41      1.54
V6      42      40      1.54
.MODEL          DX      D()
.MODEL          DZ      D(IS=1E-6)
.MODEL          QN NPN(BF=300)
.ENDS
```

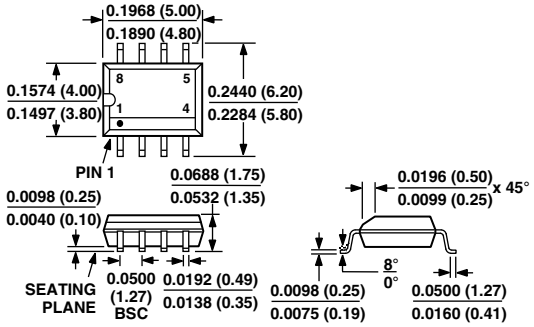
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

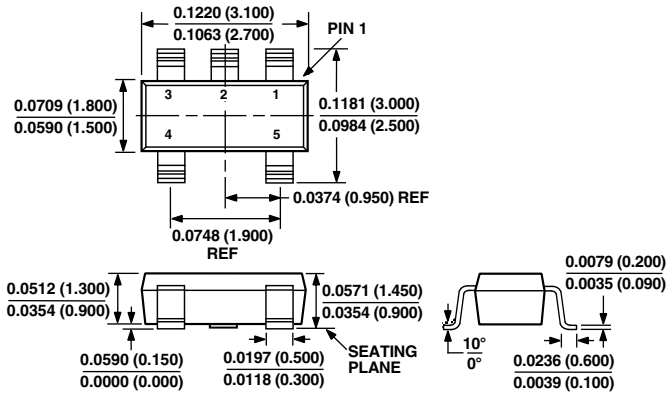
8-Lead TSSOP (RU-8)



8-Lead Narrow-Body SO (SO-8)



5-Lead SOT-23 (RT-5)



NOTE:
PACKAGE OUTLINE INCLUSIVE AS SOLDER PLATING.

C00290–0–1/02(G)

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