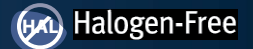


EPC2215 – Enhancement Mode Power Transistor

 V_{DS} , 200 V $R_{DS(on)}$, 8 mΩ I_D , 32 A

Revised December 18, 2023

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5–5.25 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions:
Ask a GaN
Expert



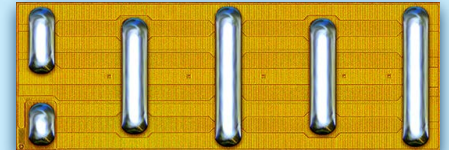
Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
I_D	Continuous ($T_A = 25^\circ\text{C}$)	32	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	162	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	2.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	52	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 0.6 \text{ mA}$	200			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$, $V_{DS} = 160 \text{ V}$		0.15	0.48	mA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.03	3.8	
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5 \text{ V}$, $T_J = 125^\circ\text{C}$		0.5	8.7	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		0.15	0.48	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 6 \text{ mA}$	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 20 \text{ A}$		6	8	mΩ
V_{SD}	Source-Drain Forward Voltage [#]	$I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.6		V

[#] Defined by design. Not subject to production test.



Die size: 4.6 x 1.6 mm

EPC2215 eGaN® FETs are supplied only in passivated die form with solder bars.

Applications

- DC-DC converters
- BLDC motor drives
- Sync rectification for AC/DC and DC-DC
- Multi-level AC/DC power supplies
- Wireless power
- Solar micro-inverters
- Robotics
- Class-D audio

Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2215>

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{ISS}	Input Capacitance	V _{DS} = 100 V, V _{GS} = 0 V		1356	1790	pF
C _{RSS}	Reverse Transfer Capacitance			2.0		
C _{OSS}	Output Capacitance			390	585	
C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 2)	V _{DS} = 0 to 100 V, V _{GS} = 0 V		556		
C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 3)			699		
R _G	Gate Resistance			0.4		Ω
Q _G	Total Gate Charge	V _{DS} = 100 V, V _{GS} = 5 V, I _D = 20 A		13.6	17.7	nC
Q _{GS}	Gate-to-Source Charge	V _{DS} = 100 V, I _D = 20 A		3.3		
Q _{GD}	Gate-to-Drain Charge			2.1		
Q _{G(TH)}	Gate Charge at Threshold			2.4		
Q _{OSS}	Output Charge	V _{DS} = 100 V, V _{GS} = 0 V		69	104	
Q _{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Note 3: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

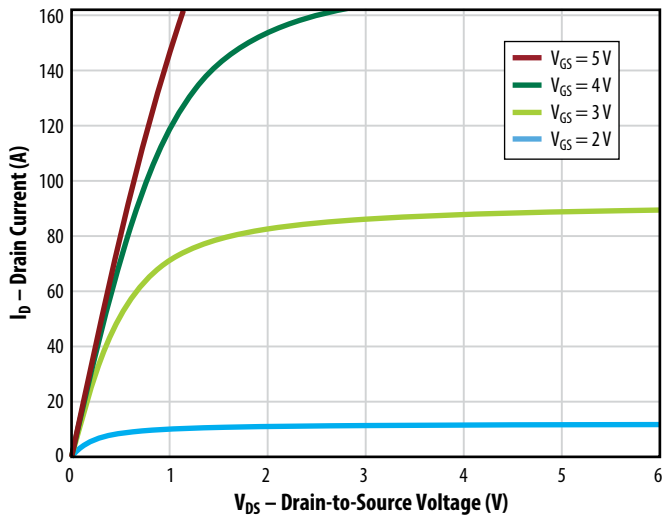


Figure 2: Typical Transfer Characteristics

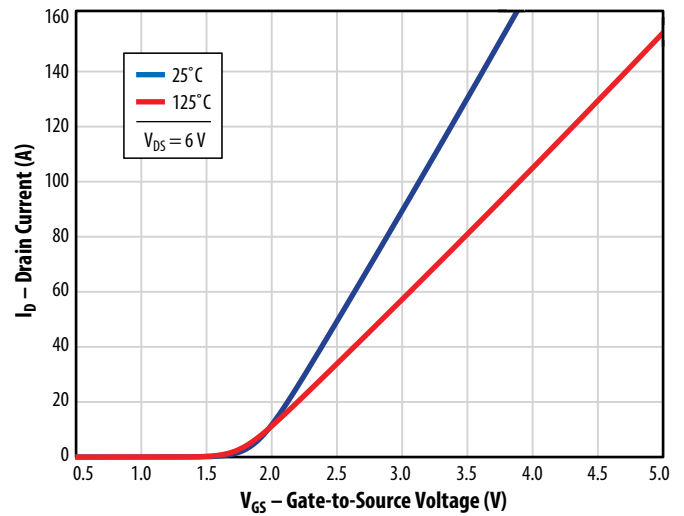


Figure 3: Typical R_{DS(on)} vs. V_{GS} for Various Drain Currents

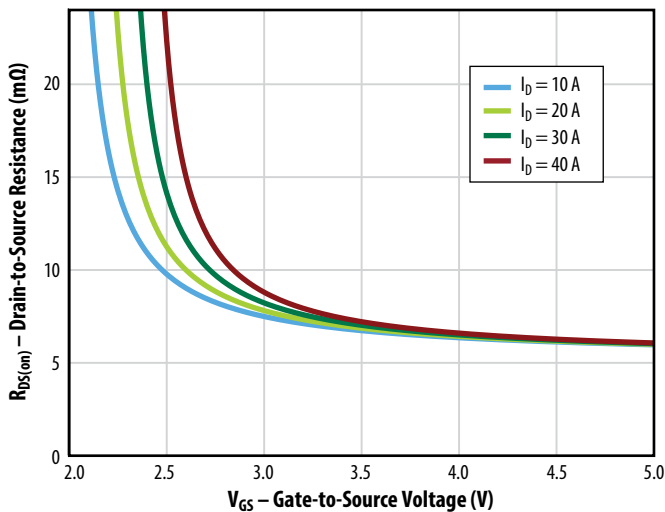


Figure 4: Typical R_{DS(on)} vs. V_{GS} for Various Temperatures

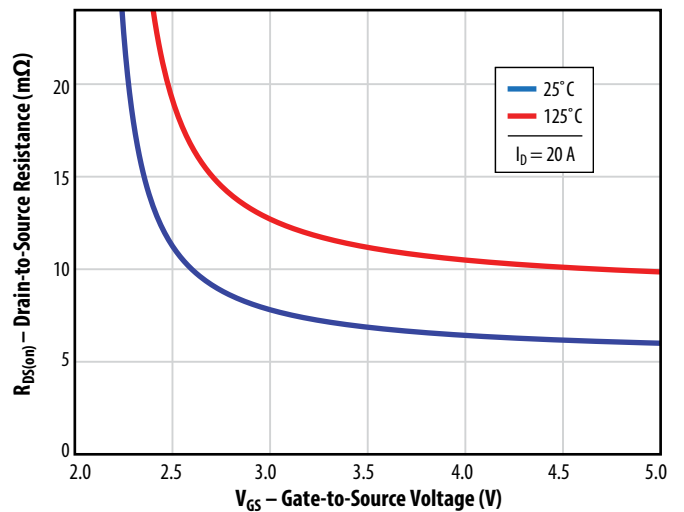


Figure 5a: Typical Capacitance (Linear Scale)

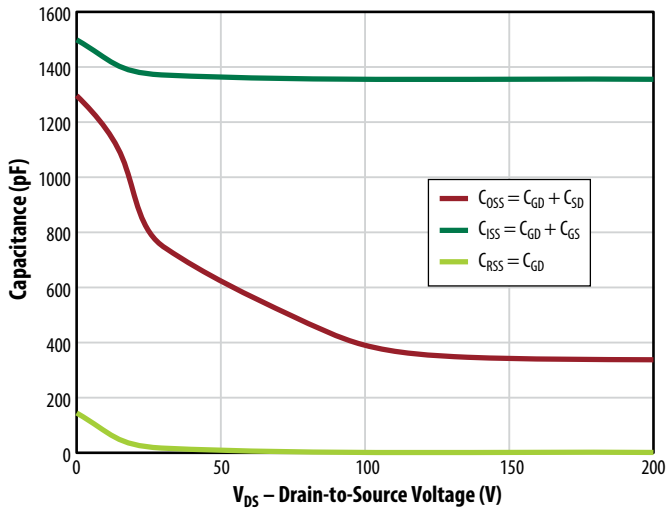


Figure 5b: Typical Capacitance (Log Scale)

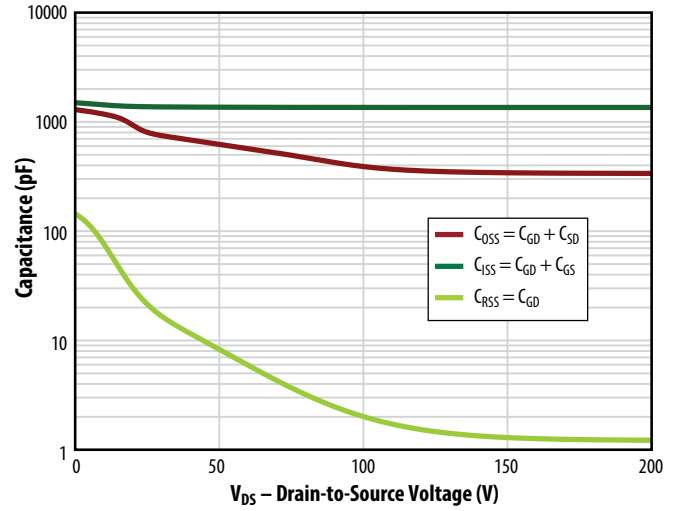


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

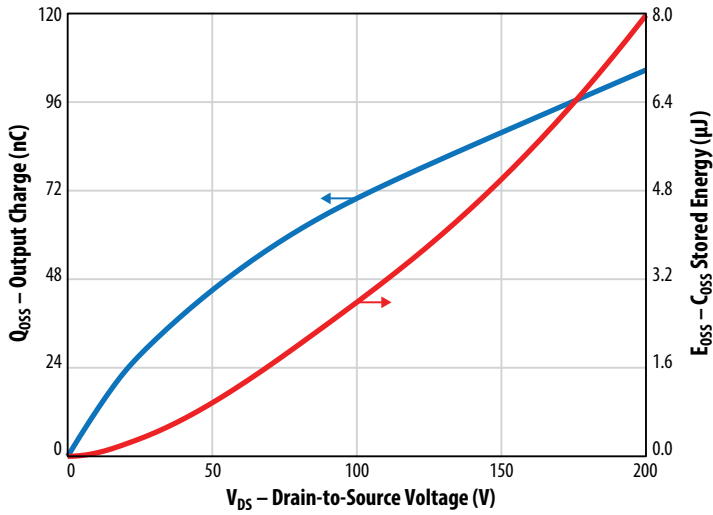


Figure 7: Typical Gate Charge

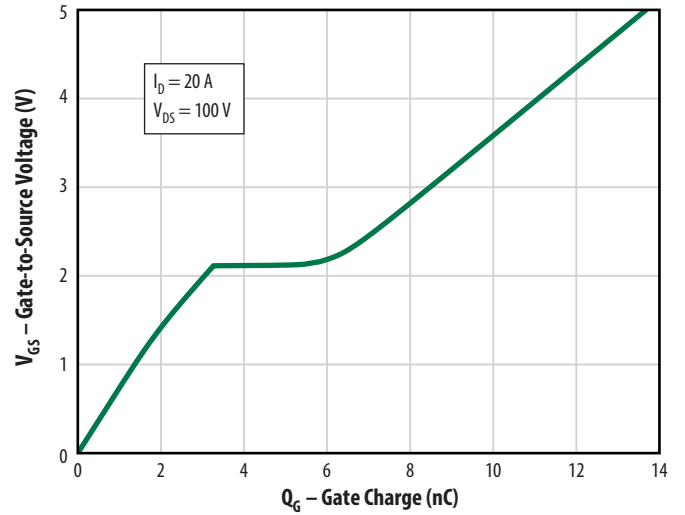


Figure 8: Typical Reverse Drain-Source Characteristics

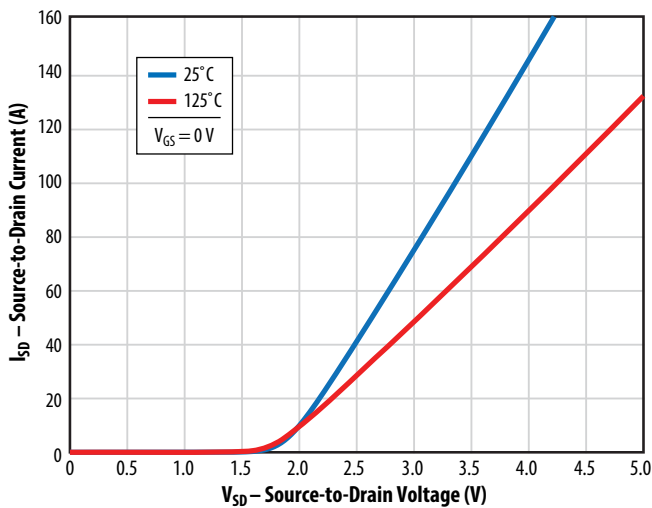
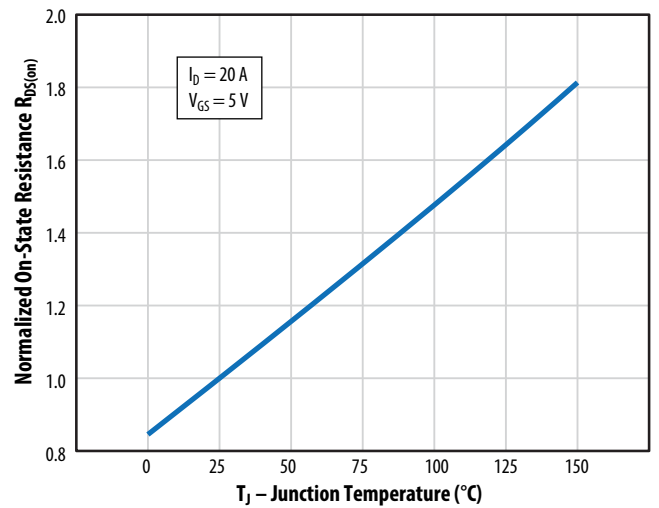


Figure 9: Typical Normalized On-State Resistance vs. Temp.



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 10: Typical Normalized Threshold Voltage vs. Temp.

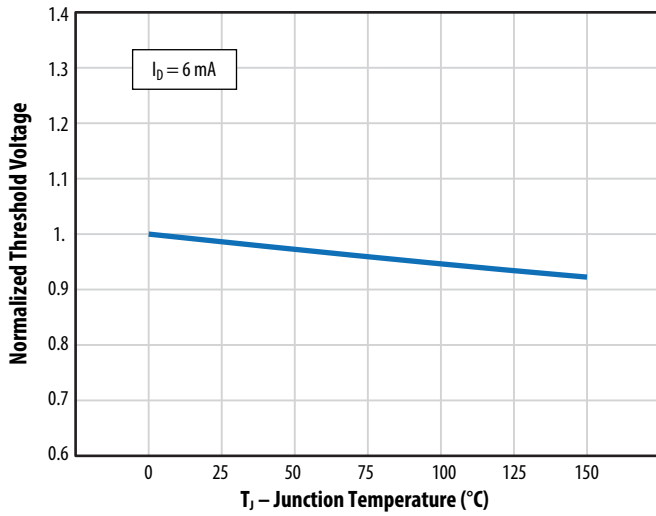


Figure 11: Safe Operating Area

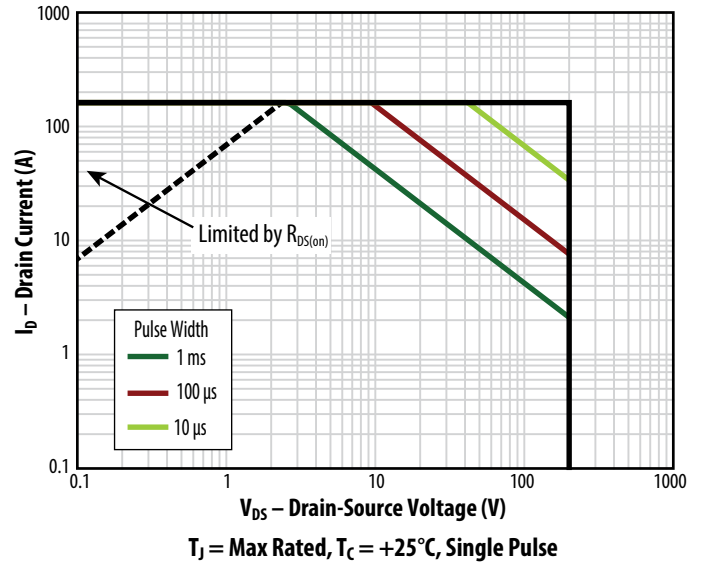
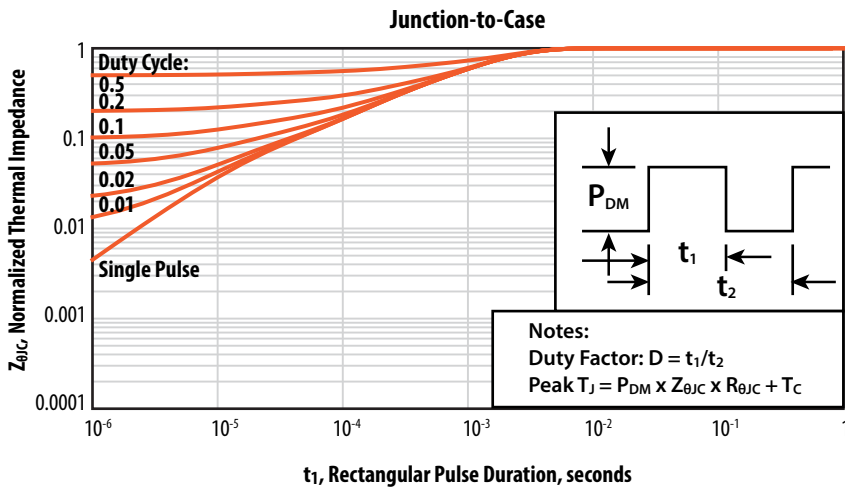
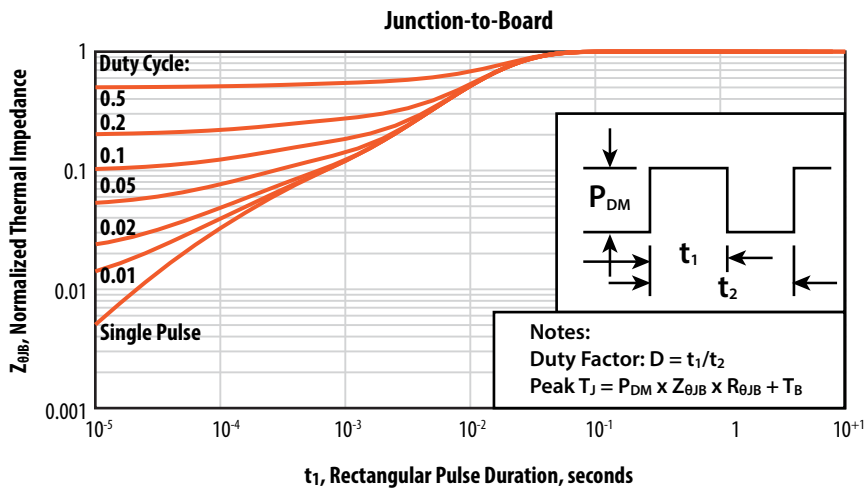
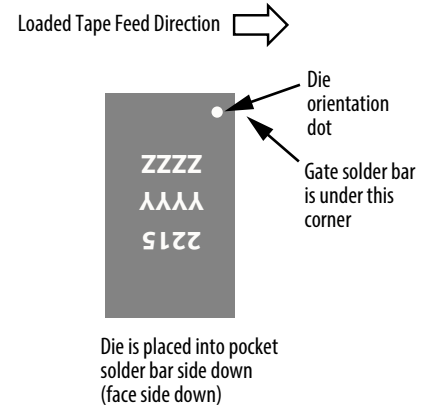
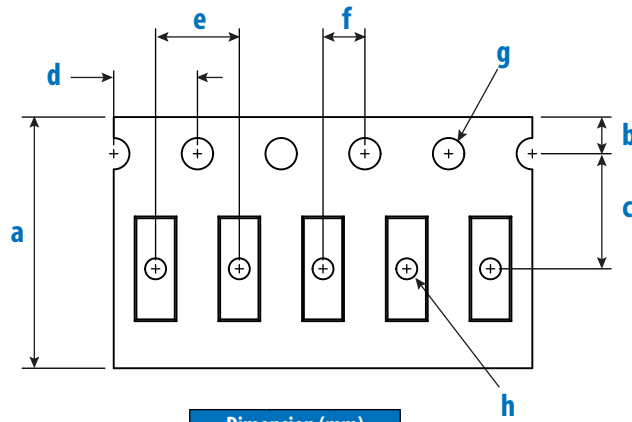
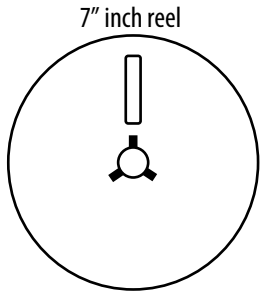


Figure 12: Typical Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

4 mm pitch, 12 mm wide tape on 7" reel

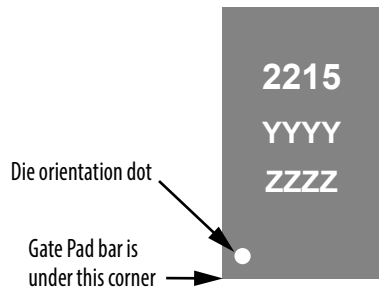


EPC2215 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	0.95	1.05

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

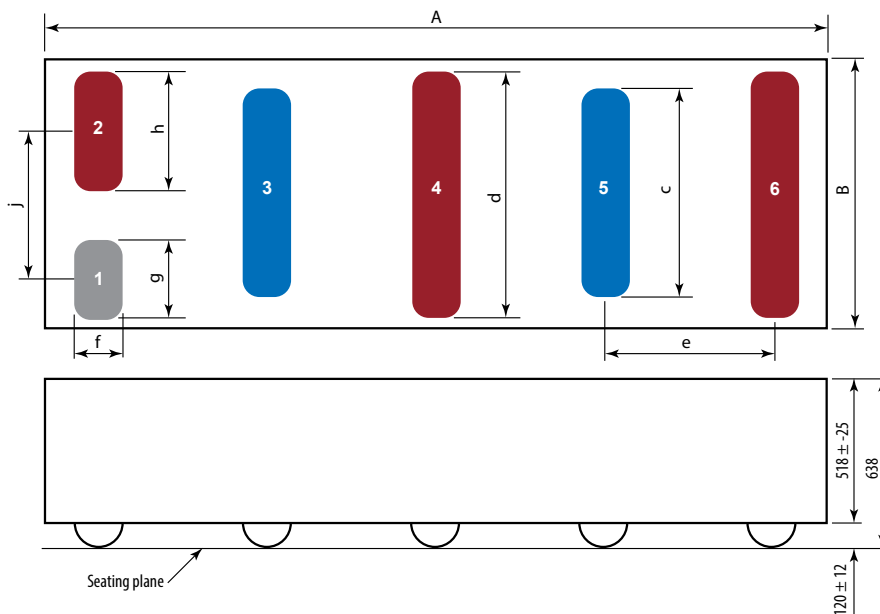
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2215	2215	YYYY	ZZZZ

DIE OUTLINE

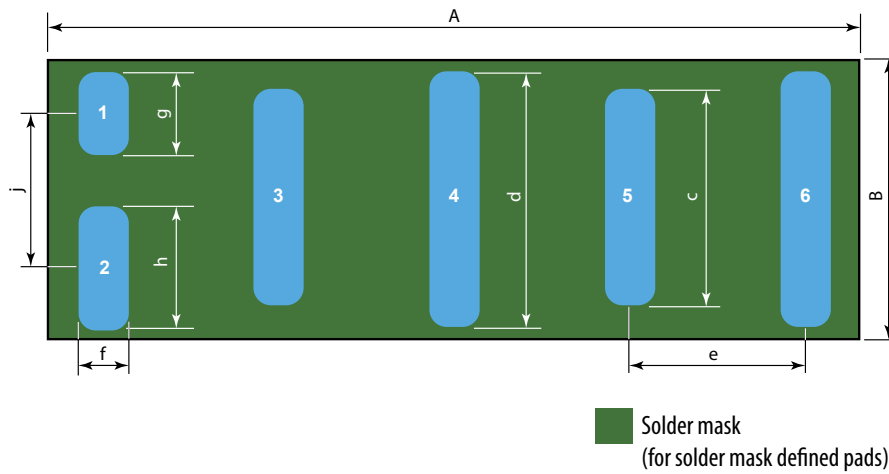
Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	4570	4600	4630
B	1570	1600	1630
c		1210	
d		1450	
e		1000	
f		275	
g		450	
h		700	
j		875	

Pad 1 is Gate;
 Pads 2, 4, 6 are Source;
 Pads 3, 5 are Drain

RECOMMENDED LAND PATTERN
(units in μm)

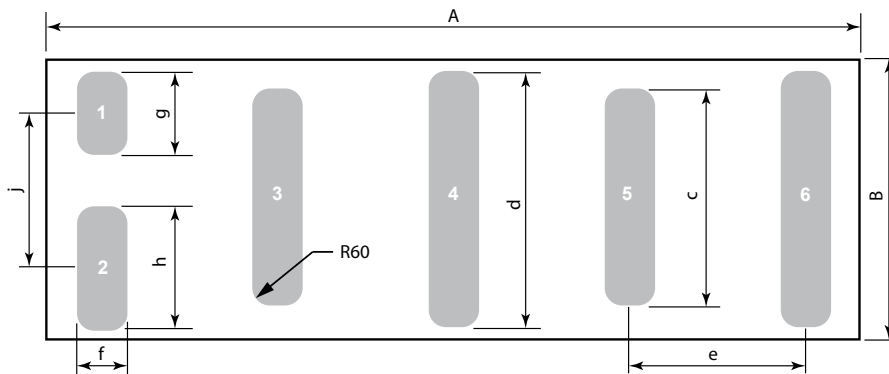


Land pattern is solder mask defined.

Pad 1 is Gate;
Pads 2, 4, 6
are Source;
Pads 3, 5 are Drain

DIM	Nominal
A	4600
B	1600
c	1210
d	1450
e	1000
f	275
g	450
h	700
j	875

RECOMMENDED STENCIL DRAWING
(units in μm)



DIM	Nominal
A	4600
B	1600
c	1210
d	1450
e	1000
f	275
g	450
h	700
j	875

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

TYPICAL THERMAL CONCEPT

The EPC2215 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. **Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.**

Recommended best practice thermal solutions are covered in detail in [How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf](#).

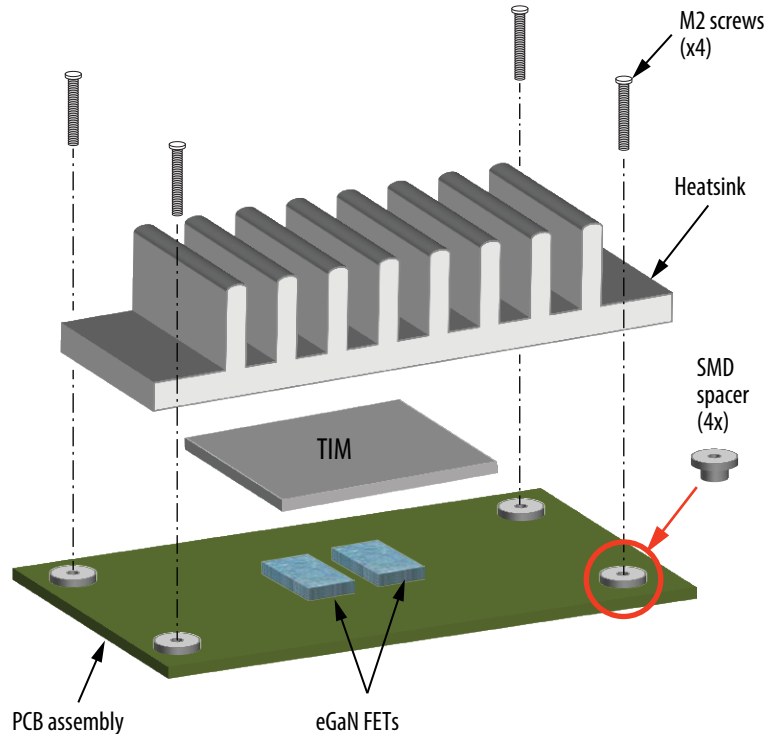


Figure 13: Exploded view of heatsink assembly using screws

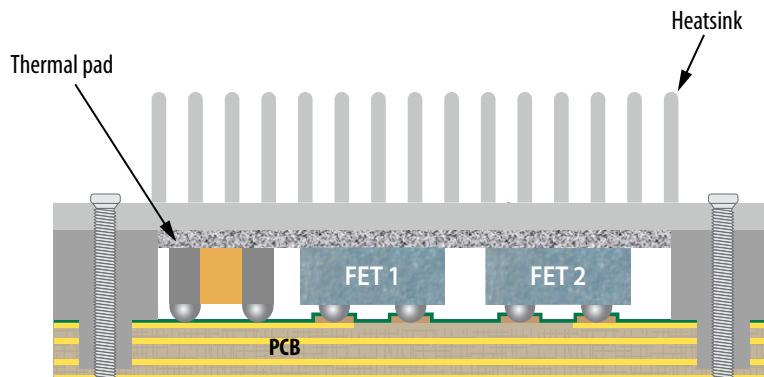


Figure 14: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the [GaN FET Thermal Calculator](#) on EPC's website.

Solder mask defined pads are recommended for best reliability.

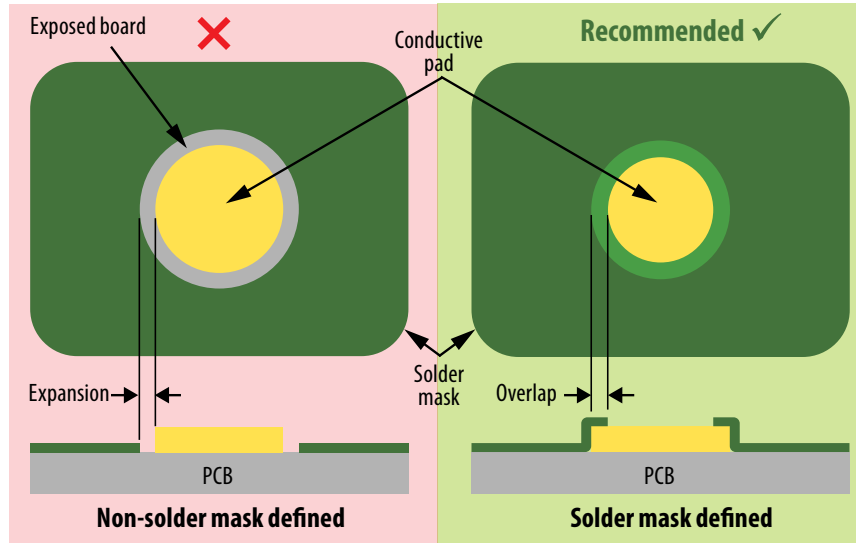


Figure 15: Solder mask defined versus non-solder mask defined pad

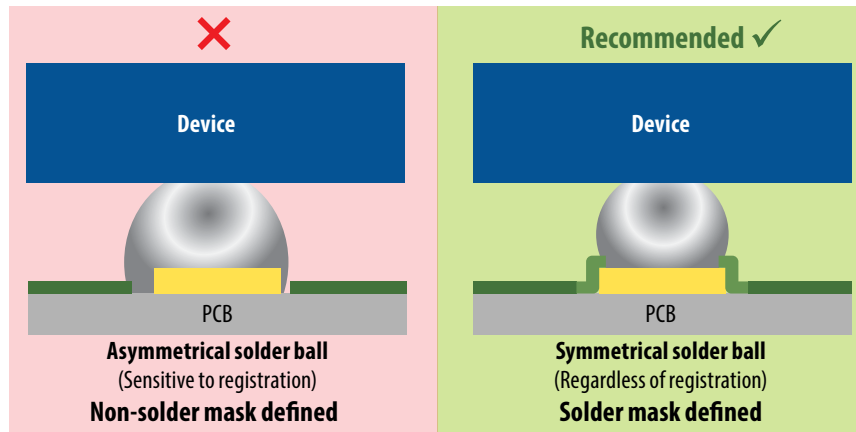


Figure 16: Effect of solder mask design on the solder ball symmetry

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip>
(for preliminary device Altium footprints, contact EPC)

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