TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS044C – Revised September 2003

CD4047B Types

CMOS Low-Power Monostable/Astable Multivibrator

High Voltage Types (20-Volt Rating)

■ CD4047B consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, −TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are $\overline{Q}$, Q, and OSCILLATOR. In all modes of operation, and external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input or a low level on the $\overline{\text{ASTABLE}}$ input, or both. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

The CD4047B triggers in the monostable mode when a positive-going edge occurs on the +TRIGGER-input while the -TRIGGER is held low. Input pulses may be of any duration relative to the output pulse.

If retrigger capability is desired, the RETRIGGER input is pulsed. The retriggerable mode of operation is limited to positive-going edge. The CD4047B will retrigger as long as the RETRIGGER-input is high, with or without transitions (See Fig. 34).

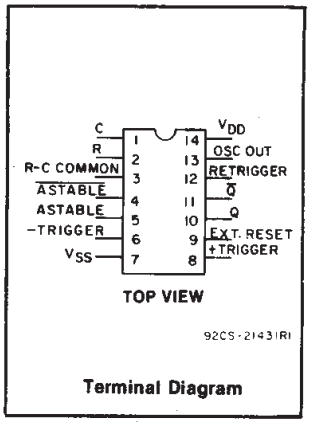
An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator.

A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. For monostable operation, whenever V_{DD} is applied, an internal power-on reset circuit will clock the Q output low within one output period (t_M).

The CD4047B-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- *Low power consumption: special CMOS oscillator configuration*
- *Monostable (one-shot) or astable (free-running) operation*
- *True and complemented buffered outputs*
- *Only one external R and C required*
- *Buffered inputs*
- *100% tested for quiescent current at 20 V*
- *Standardized, symmetrical output characteristics*
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*



Terminal Diagram

Monostable Multivibrator Features:

- *Positive- or negative-edge trigger*
- *Output pulse width independent of trigger pulse duration*
- *Retriggerable option for pulse width expansion*
- *Internal power-on reset circuit*
- *Long pulse widths possible using small RC components by means of external counter provision*
- *Fast recovery time essentially independent of pulse width*
- *Pulse-width accuracy maintained at duty cycles approaching 100%*

Astable Multivibrator Features:

- *Free-running or gatable operating modes*
- *50% duty cycle*
- *Oscillator output available*
- *Good astable frequency stability:*
  Frequency deviation:
  = ±2% + 0.03%/°C @ 100 kHz
  = ±0.5% + 0.015%/°C @ 10 kHz
  (circuits "trimmed" to frequency V_{DD} = 10 V ± 10%)

Applications:

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- *Envelope detection*
- *Frequency multiplication*
- *Frequency division*
- *Frequency discriminators*
- *Timing circuits*
- *Time-delay applications*

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V
NOTE: IF AT 15 V OPERATION A 10 MΩ RESISTOR IS USED THE OPERATING TEMPERATURE SHOULD BE BETWEEN −25°C and 100°C			

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

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CD4047B FUNCTIONAL TERMINAL CONNECTIONS
NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT TO		
Astable Multivibrator:					
Free Running	4,5,6,14	7,8,9,12	—	10,11,13	t_A (10,11) = 4.40 RC
True Gating	4,6,14	7,8,9,12	5	10,11,13	t_A (13) = 2.20 RC#
Complement Gating	6,14	5,7,8,9,12	4	10,11,13	
Monostable Multivibrator:					
Positive-Edge Trigger	4,14	5,6,7,9,12	8	10,11	
Negative-Edge Trigger	4,8,14	5,7,9,12	6	10,11	t_M (10,11) = 2.48 RC
Retriggerable	4,14	5,6,7,9	8,12	10,11	
External Countdown*	14	5,6,7,8,9,12	—	10,11	

▲ See Text.

First positive ½ cycle pulse-width = 2.48 RC, see Note on Page 3-134.

* Input Pulse to Reset of External Counting Chip External Counting Chip Output To Terminal 4

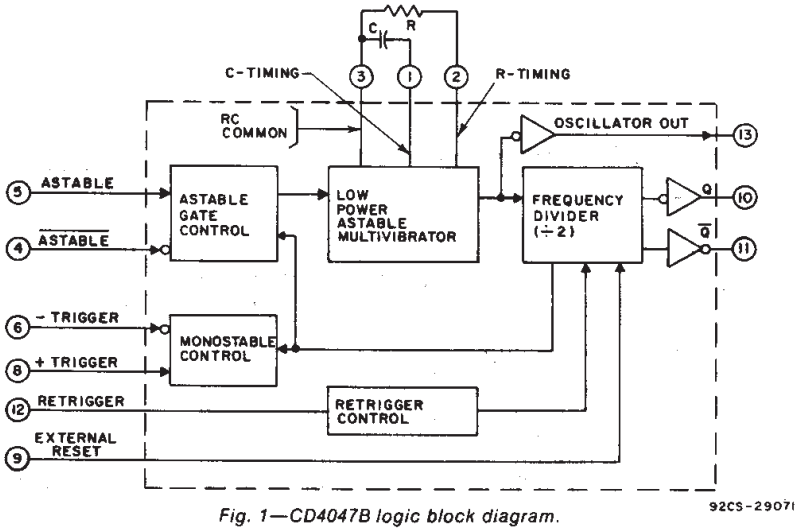


Fig. 1—CD4047B logic block diagram.

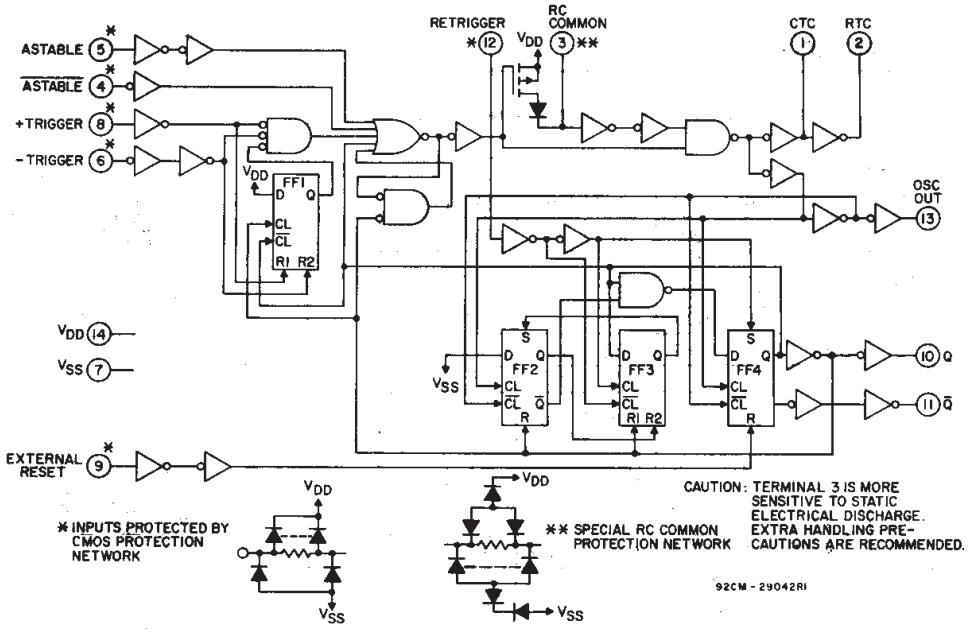


Fig. 2—CD4047B logic diagram.

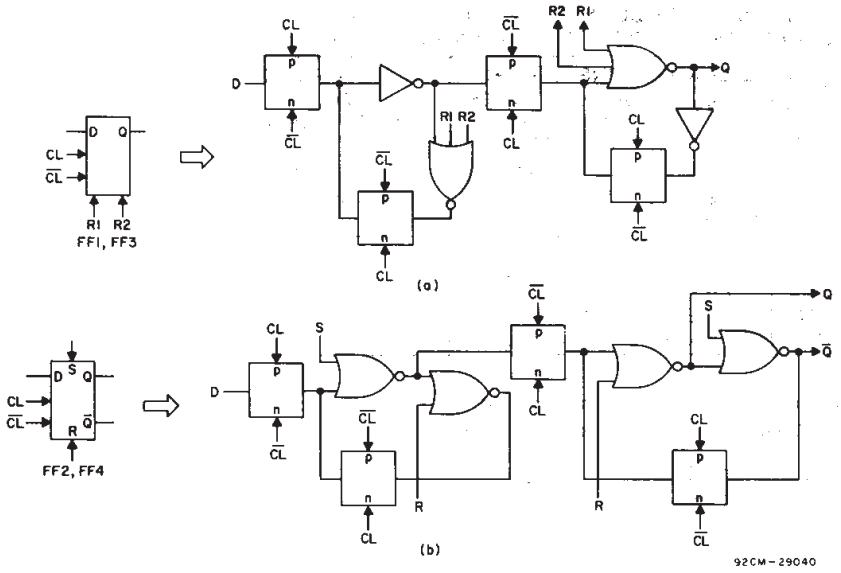


Fig. 3—Detail logic diagram for flip-flops FF1 and FF3 (a) and for flip-flops FF2 and FF4 (b).

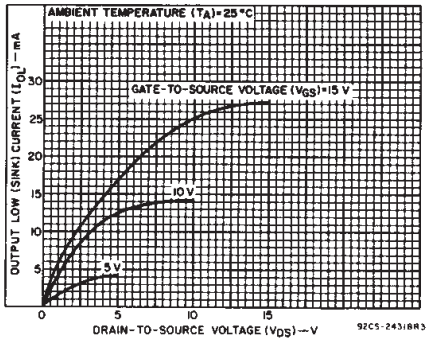


Fig. 4—Typical output low (sink) current characteristics.

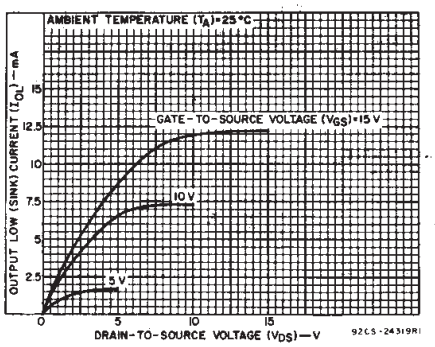


Fig. 5—Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	

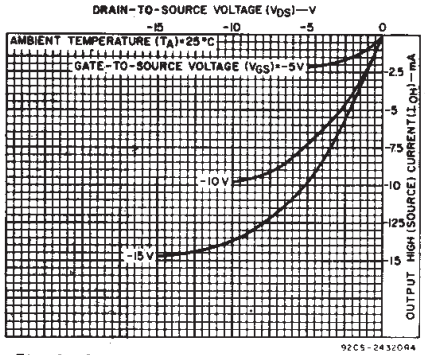


Fig. 6—Typical output high (source) current characteristics.

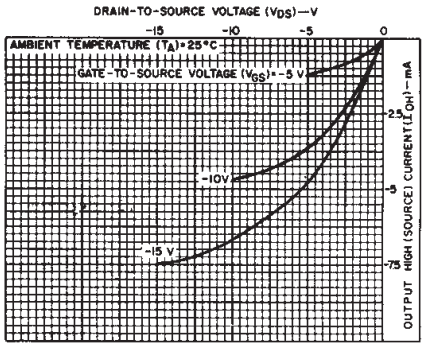


Fig. 7—Minimum output high (source) current characteristics.

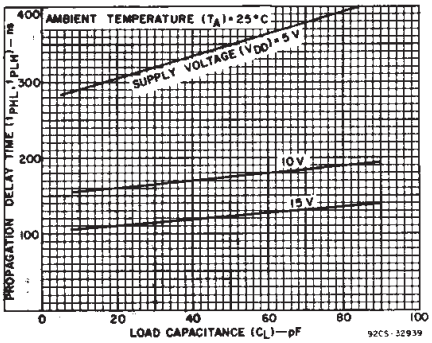


Fig. 8—Typical propagation delay time as a function of load capacitance (Astable, Astable to Q, $\overline{Q}$).

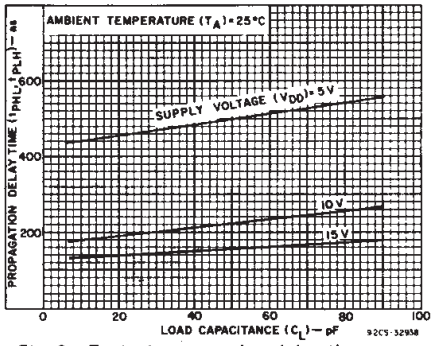


Fig. 9—Typical propagation delay time as a function of load capacitance (+ or − trigger to Q, $\overline{Q}$).

STATIC ELECTRICAL CHARACTERISTICS (CONTINUED)

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1.9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$\pm 10^5$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ*

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH}					
Astable, $\overline{\text{Astable}}$ to Osc. Out	5	—	200	400	ns
	10	—	100	200	
	15	—	80	160	
Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$	5	—	350	700	
	10	—	175	350	
	15	—	125	250	
+ or − Trigger to Q, $\overline{Q}$	5	—	500	1000	
	10	—	225	450	
	15	—	150	300	
Retrigger to Q, $\overline{Q}$	5	—	300	600	
	10	—	150	300	
	15	—	100	200	
External Reset to Q, $\overline{Q}$	5	—	250	500	
	10	—	100	200	
	15	—	70	140	
Transition Time, t_{THL}, t_{TLH}					
Osc. Out, Q, $\overline{Q}$	5	—	100	200	
	10	—	50	100	
	15	—	40	80	
Minimum Input Pulse Width, t_W					
+ Trigger, − Trigger	5	—	200	400	
	10	—	80	160	
	15	—	50	100	
Reset	5	—	100	200	
	10	—	50	100	
	15	—	30	60	
Retrigger	5	—	300	600	
	10	—	115	230	
	15	—	75	150	
Input Rise and Fall Time, t_r, t_f					
All Trigger Inputs					
For + Trigger: t_r					
t_r only is unlimited	5	—	270	—	
	10	—	18	—	
	15	—	9	—	μs
For − Trigger: t_r	5	—	325	—	
t_f only is unlimited	10	—	9	—	
	15	—	4	—	
Q or $\overline{Q}$ Deviation from 50% Duty Factor	5	—	±0.5	±1	
	10	—	±0.5	±1	%
	15	—	±0.1	±0.5	
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

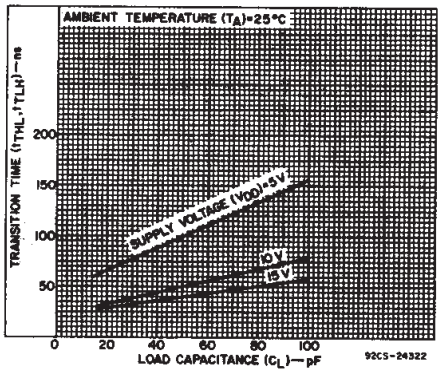


Fig. 10—Typical transition time as a function of load capacitance.

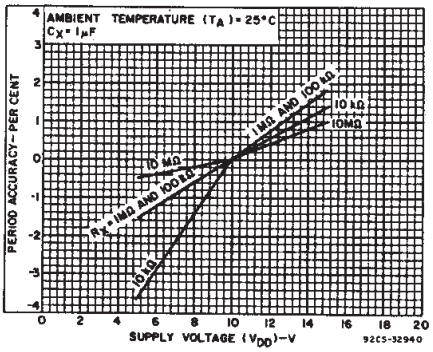


Fig. 11—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. supply voltage.

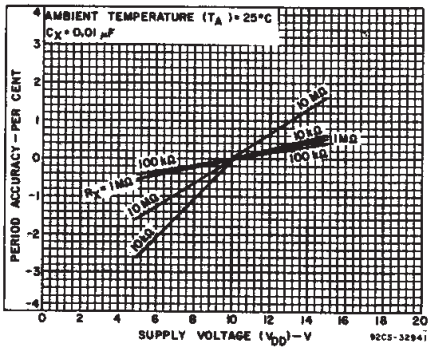


Fig. 12—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. supply voltage.

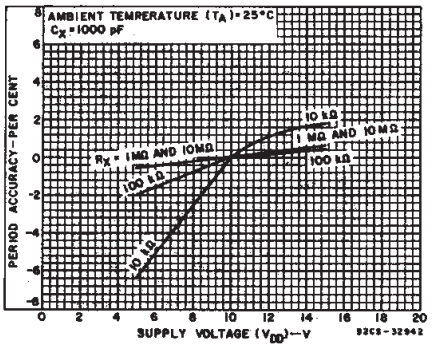


Fig. 13—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. supply voltage.

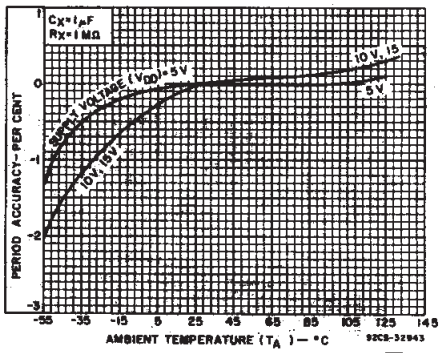


Fig. 14—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (ultra-low frequency).

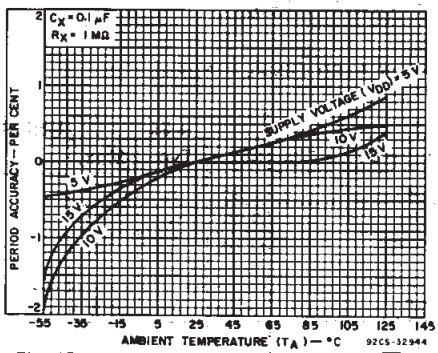


Fig. 15—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (low frequency).

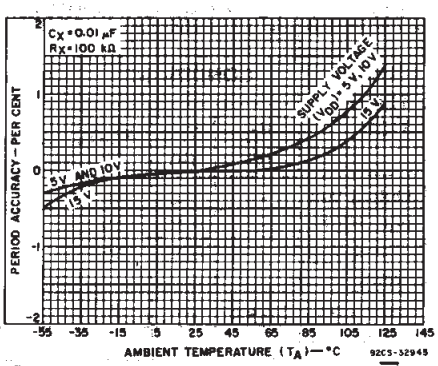


Fig. 16—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (medium frequency).

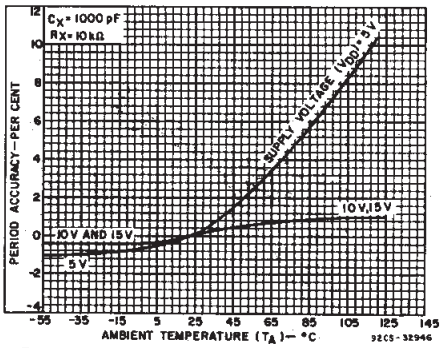


Fig. 17—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (high-frequency).

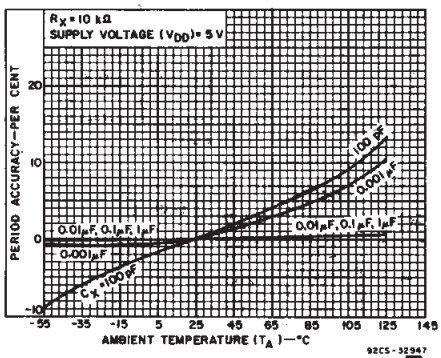


Fig. 18—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature.

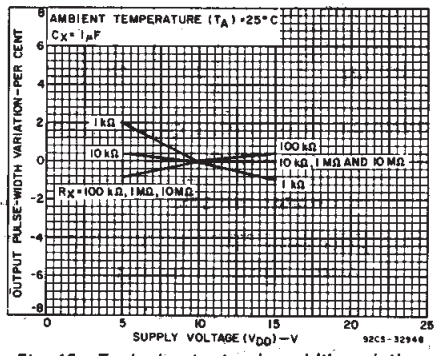


Fig. 19—Typical output pulse-width variations vs. supply voltage.

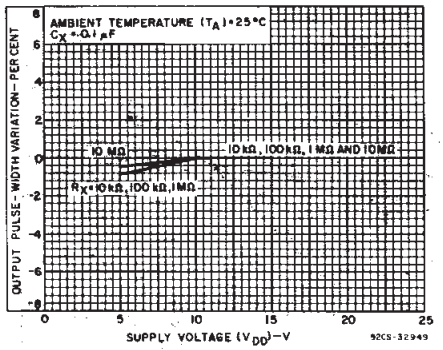


Fig. 20—Typical output pulse-width variations vs. supply voltage.

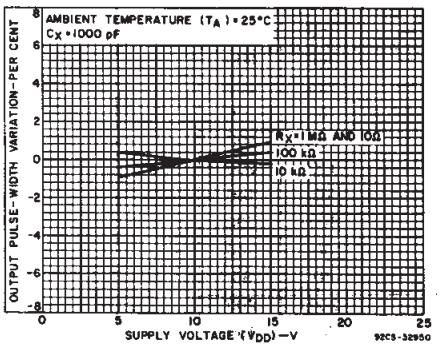


Fig. 21—Typical output pulse-width variations vs. supply voltage.

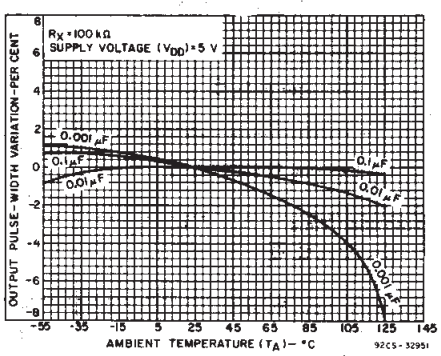


Fig. 22—Typical output pulse-width variations vs. ambient temperature.

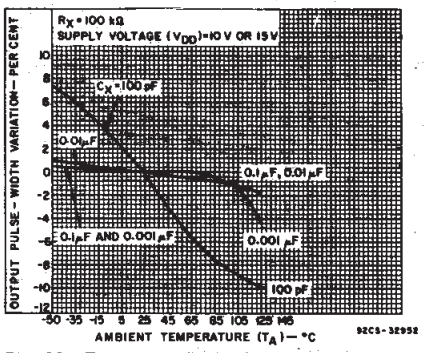


Fig. 23—Typical output pulse-width variations vs. ambient temperature.

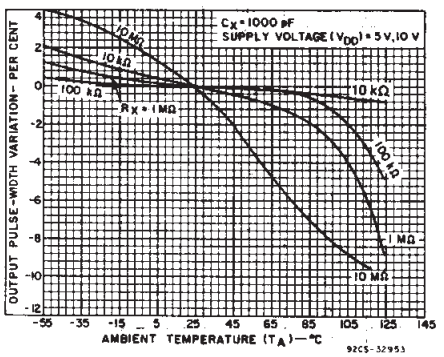


Fig. 24—Typical output-pulse-width variations vs. ambient temperature.

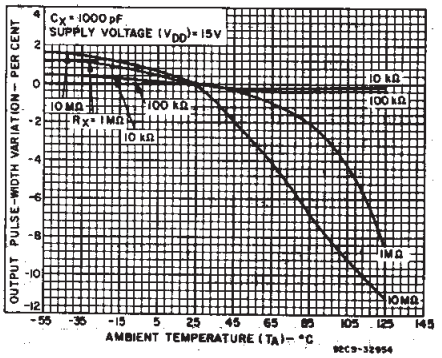


Fig. 25—Typical output pulse-width variations vs. ambient temperature.

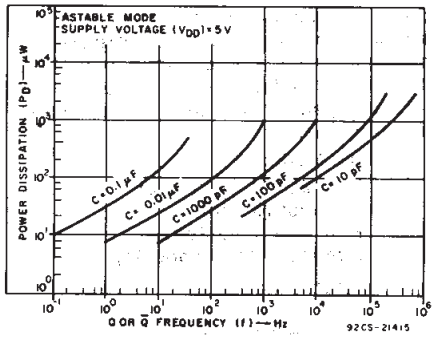


Fig. 26—Typical power dissipation vs. output frequency (V_{DD} = 5 V).

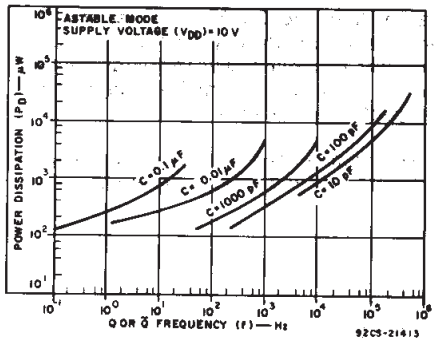


Fig. 27—Typical power dissipation vs. output frequency (V_{DD} = 10 V).

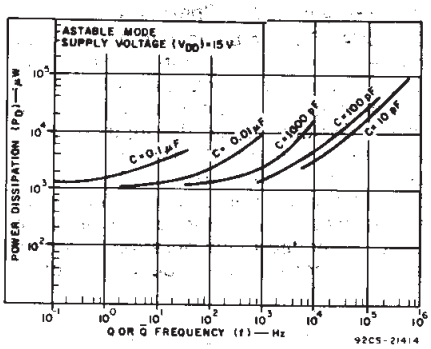


Fig. 28—Typical power dissipation vs. output frequency (V_{DD} = 15 V).

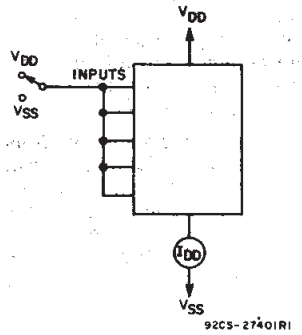


Fig. 29—Quiescent device current test circuit.

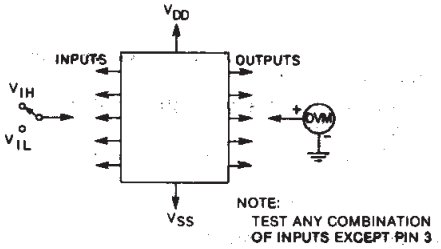


Fig. 30—Input-voltage test circuit.

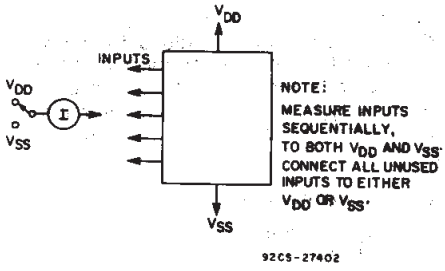


Fig. 31—Input-leakage-current test circuit.

1. Astable Mode Design Information

A. Unit-to-Unit Transfer-Voltage Variations — The following analysis presents variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33%—67% V_{DD}) for free-running (astable) operation.

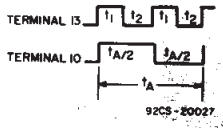


Fig. 32—Astable mode waveforms.

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}};$$

typically, $t_1 = 1.1\ RC$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}};$$

typically, $t_2 = 1.1\ RC$

$$t_A = 2(t_1 + t_2)$$

$$= -2\ RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_A = 4.40\ RC$
Min: $V_{TR} = 0.33\ V_{DD}$ $t_A = 4.62\ RC$
Max: $V_{TR} = 0.67\ V_{DD}$ $t_A = 4.62\ RC$

thus if $\boxed{t_A = 4.40\ RC}$ is used, the variation will be +5%, −0% due to variations in transfer voltage.

B. Variations Due to V_{DD} and Temperature Changes — In addition to variations from unit to unit, the astable period varies with V_{DD} and temperature. Typical variations are presented in graphical form in Figs. 11 to 18 with 10 V as reference for voltage variations curves and 25°C as reference for temperature variations curves.

II. Monostable Mode Design Information

The following analysis presents variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33% — 67% V_{DD}) for one-shot (monostable) operation.

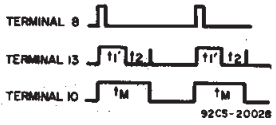


Fig. 33—Monostable waveforms.

$$t_1' = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

typically, $t_1' = 1.38\ RC$

$$t_M = (t_1' + t_2)$$

$$t_M = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where t_M = Monostable mode pulse width. Values for t_M are as follows:

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48\ RC$
Min: $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71\ RC$
Max: $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48\ RC$

thus if $\boxed{t_M = 2.48\ RC}$ is used, the variation will be +9.3%, −0% due to variations in transfer voltage.

Note:

In the astable mode, the first positive half cycle has a duration of t_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width varies with V_{DD} and temperature. These variations are presented in graphical form in Fig. 19 to 26 with 10 V as reference for voltage-variation curves and 25°C as reference for temperature-variation curves.

III. Retrigger Mode Operation

The CD4047B can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminal 12, and the output is taken from terminal 10 or 11. As shown in Fig. 34 normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied.

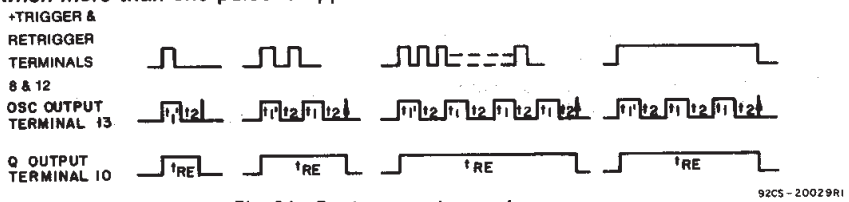


Fig. 34—Retrigger-mode waveforms.

For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, the output pulse width is an integral number of time periods, with the first time period being $t_1' + t_2$, typically, 2.48RC, and all subsequent time periods being $t_1 + t_2$, typically, 2.2RC.

IV. External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 35. The pulse duration at the output is

$$t_{ext} = (N - 1)(t_A) + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

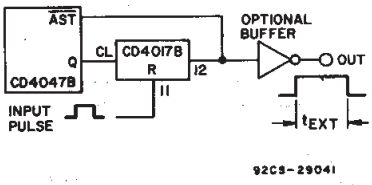


Fig. 35—Implementation of external counter option.

V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be at least an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the CMOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geq 100$ pF, up to any practical value, for astable modes;

$C \geq 1000$ pF, up to any practical value for monostable modes.

$10\ k\Omega \leq R \leq 1\ M\Omega$

VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode:

$P = 2CV^2f$. (Output at terminal No. 13)

$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

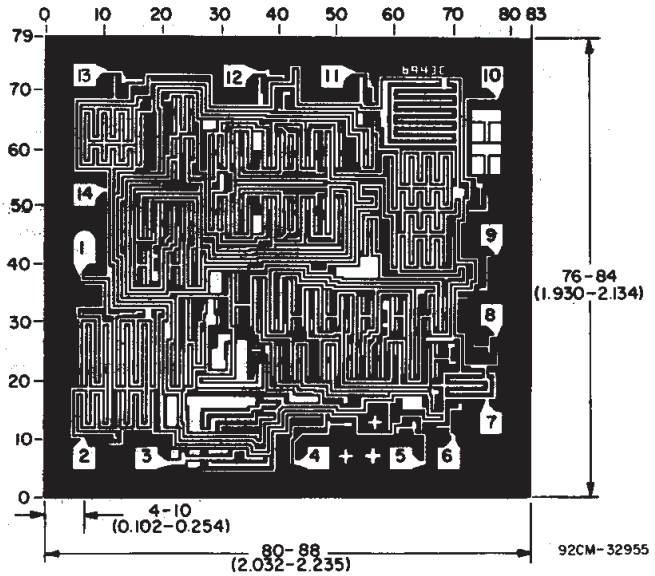
Monostable Mode:

$$P = \frac{(2.9CV^2)\,(\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 27, 28, and 29 for typical power consumption in astable mode.



Chip dimensions and pad layout for CD4047B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
8102001CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102001CA CD4047BF3A
CD4047BD3	Active	Production	CDIP SB (JD) | 14	24 | TUBE	No	AU	N/A for Pkg Type	-55 to 125	CD4047BD/3
CD4047BD3.A	Active	Production	CDIP SB (JD) | 14	24 | TUBE	No	AU	N/A for Pkg Type	-55 to 125	CD4047BD/3
CD4047BE	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4047BE
CD4047BE.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4047BE
CD4047BEE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4047BE
CD4047BF	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4047BF
CD4047BF.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4047BF
CD4047BF3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102001CA CD4047BF3A
CD4047BF3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8102001CA CD4047BF3A
CD4047BM	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	CD4047BM
CD4047BM96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4047BM
CD4047BM96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4047BM
CD4047BM96G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4047BM
CD4047BMT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	CD4047BM
CD4047BNSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4047B
CD4047BNSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4047B
CD4047BPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-55 to 125	CM047B
CD4047BPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CM047B
CD4047BPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM047B
CD4047BPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM047B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4047B, CD4047B-MIL :

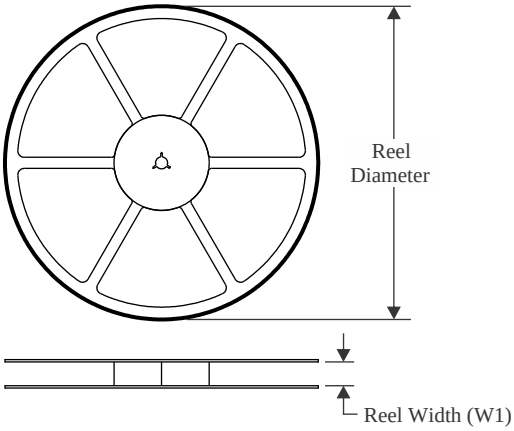
- Catalog : CD4047B
- Military : CD4047B-MIL

NOTE: Qualified Version Definitions:

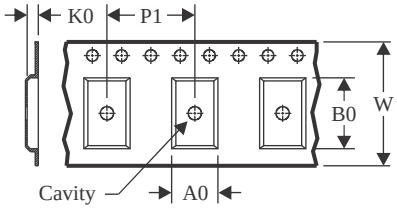
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

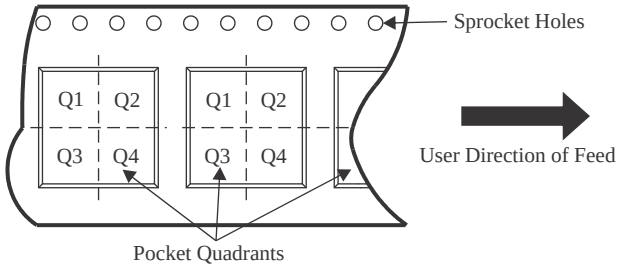


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

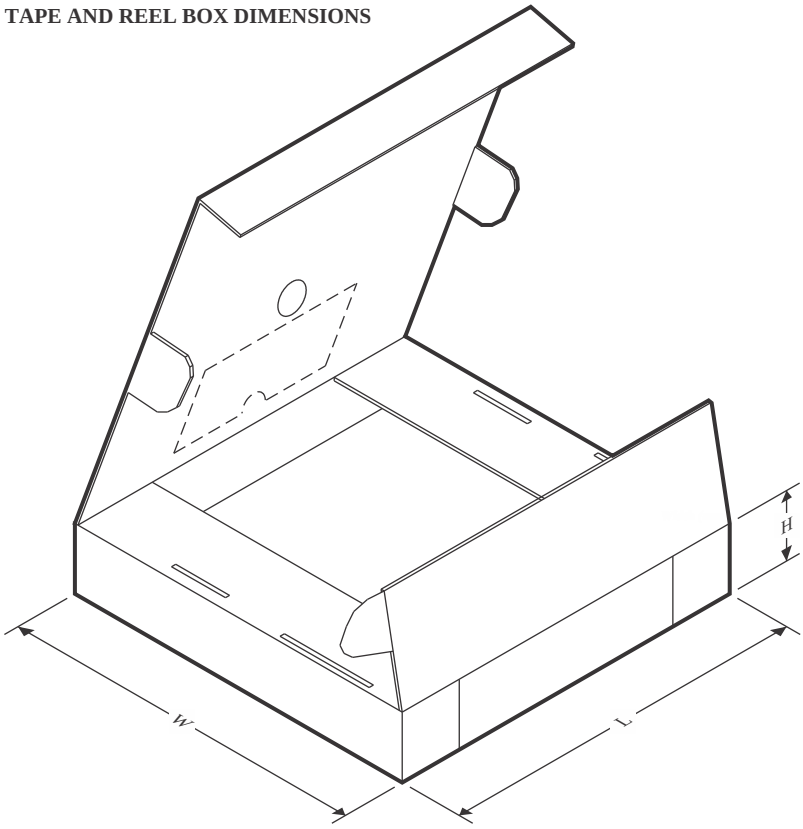
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4047BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4047BNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4047BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4047BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4047BPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

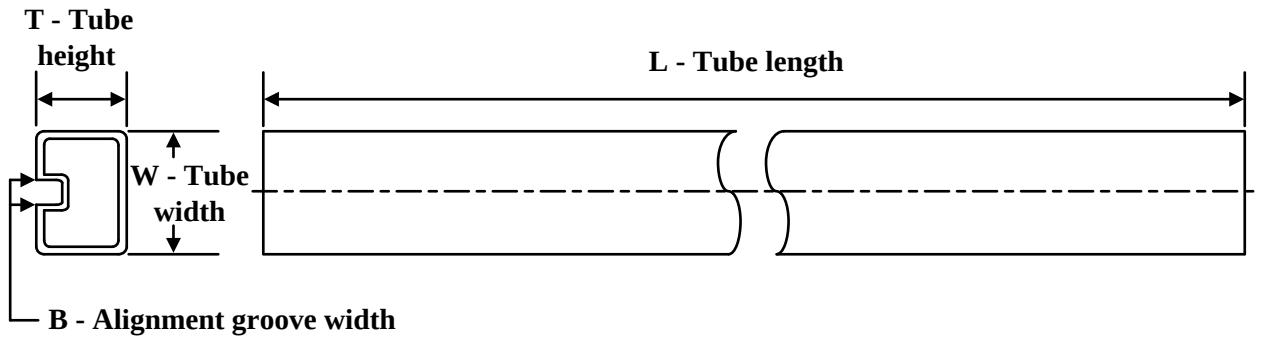
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4047BM96	SOIC	D	14	2500	353.0	353.0	32.0
CD4047BNSR	SOP	NS	14	2000	353.0	353.0	32.0
CD4047BPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
CD4047BPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
CD4047BPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

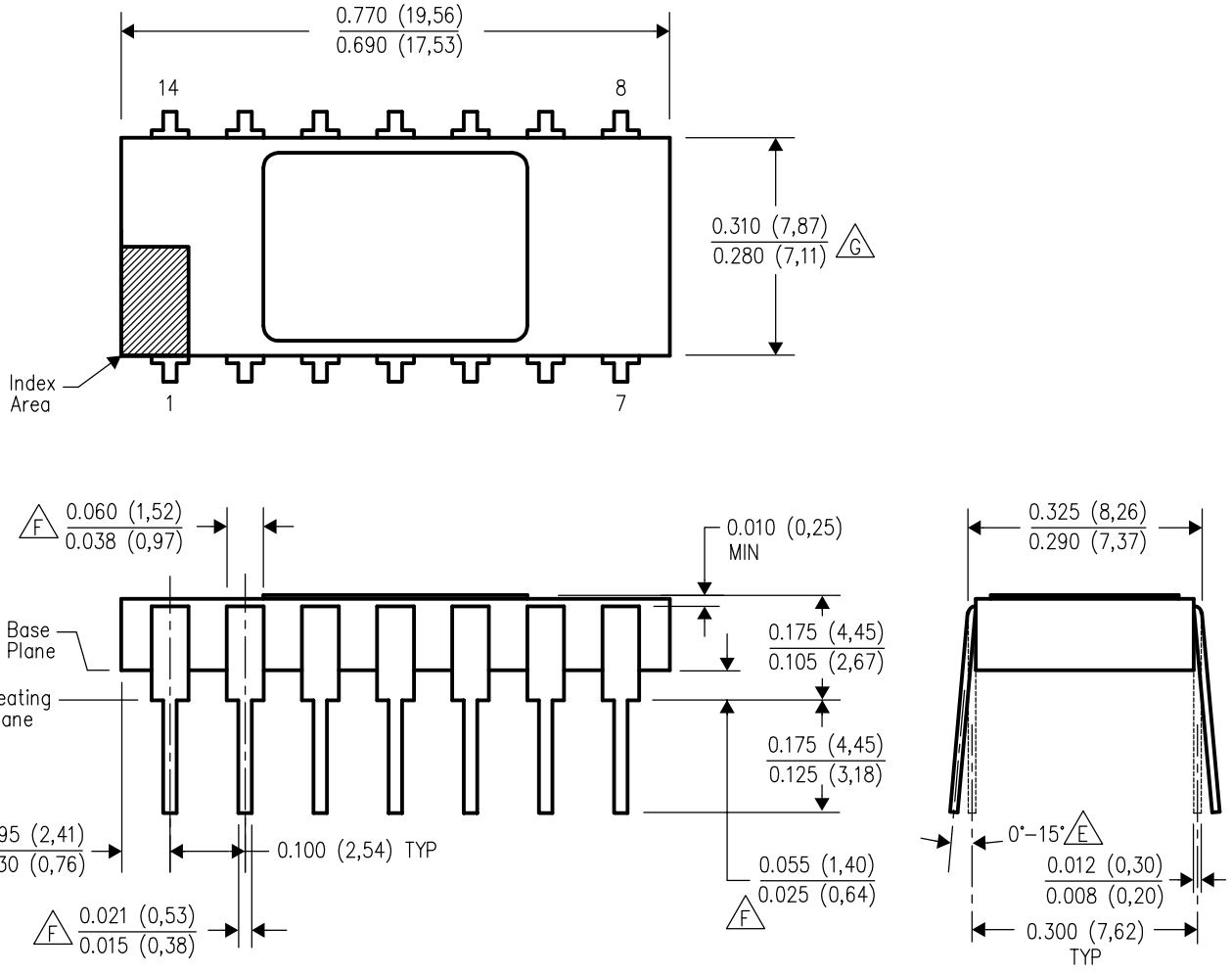
TUBE



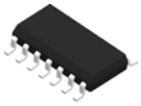
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4047BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4047BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4047BEE4	N	PDIP	14	25	506	13.97	11230	4.32

JD (R–CDIP–T14) CERAMIC SIDE–BRAZE DUAL–IN–LINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension: inch.
- D. Leads within 0.005 (0,13) radius of true position (TP) at gage plane with maximum material condition and unit installed.
- E Angle applies to spread leads prior to installation.
- F Outlines on which the seating plane is coincident with the plane (standoff = 0), terminals lead standoffs are not required, and lead shoulder may equal lead width along any part of the lead above the seating/base plane.
- G Body width does not include particles of packing materials.
- H. A visual index feature must be located within the cross–hatched area.

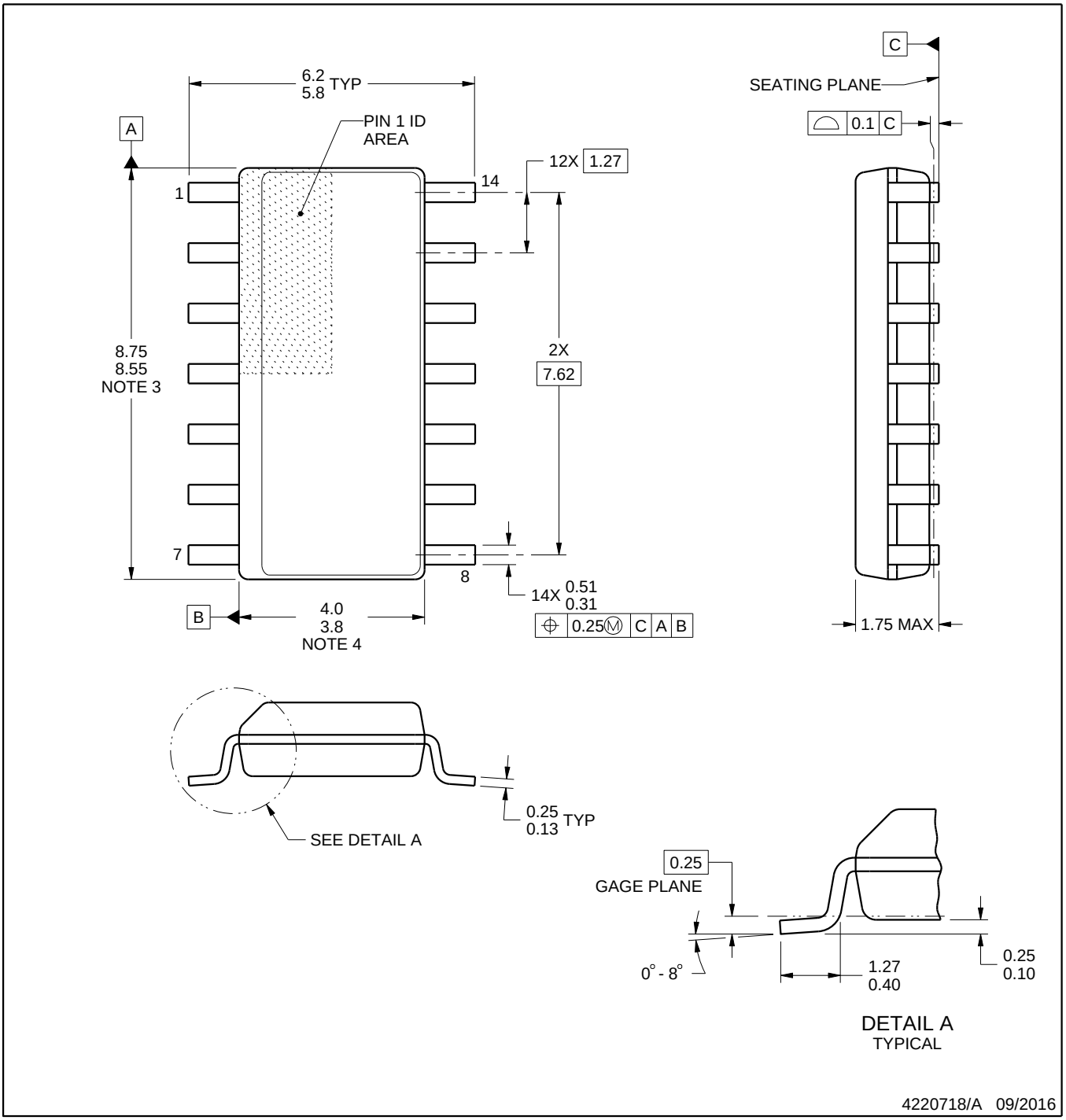


PACKAGE OUTLINE

D0014A

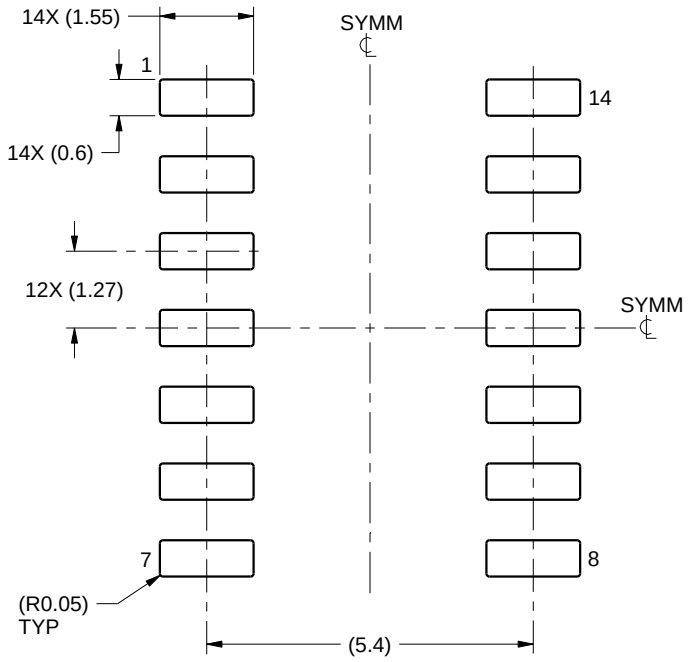
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

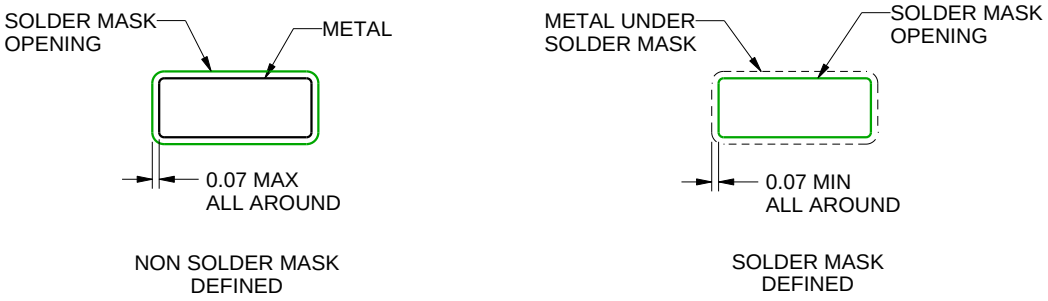


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

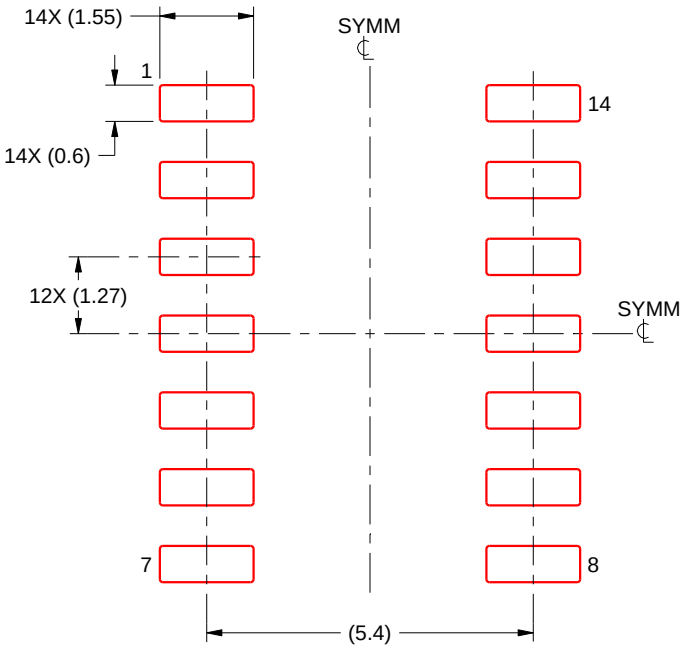
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

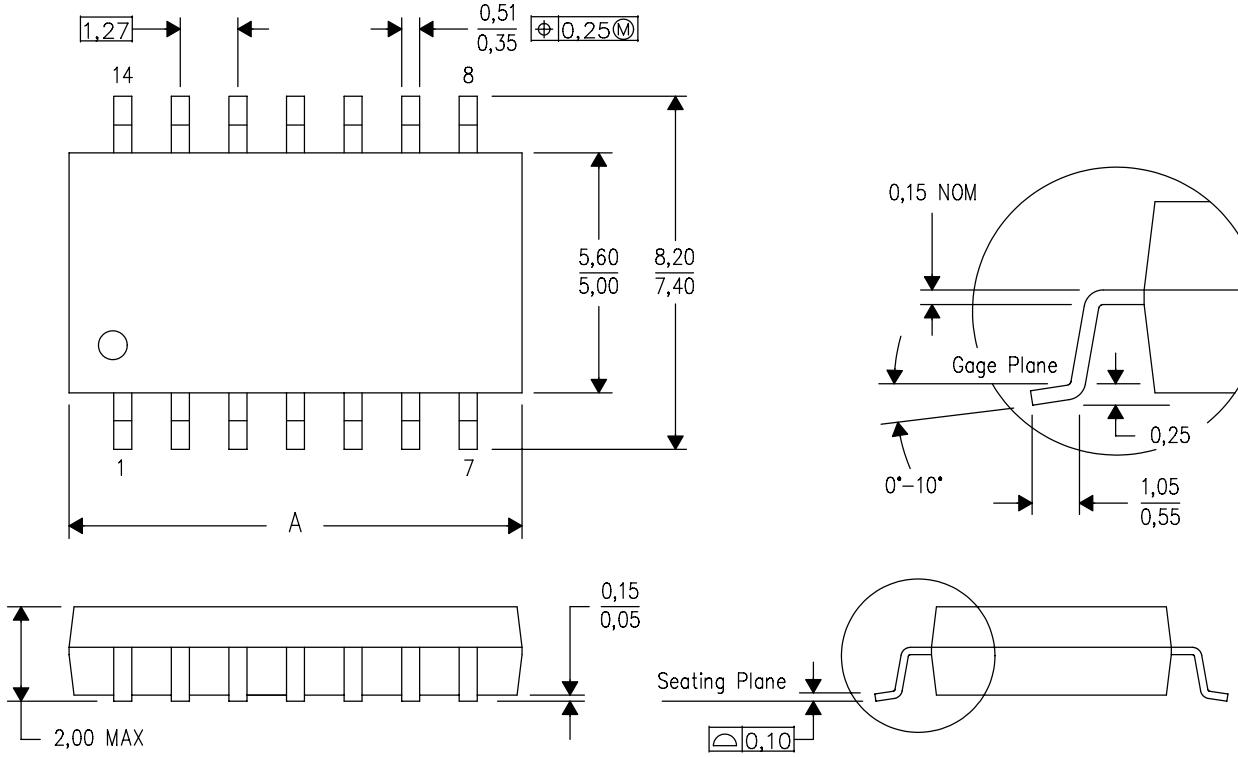
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

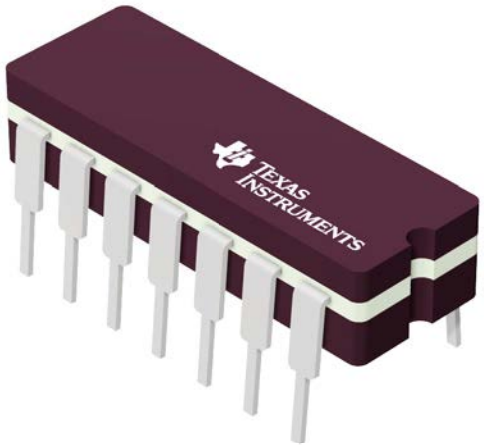
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

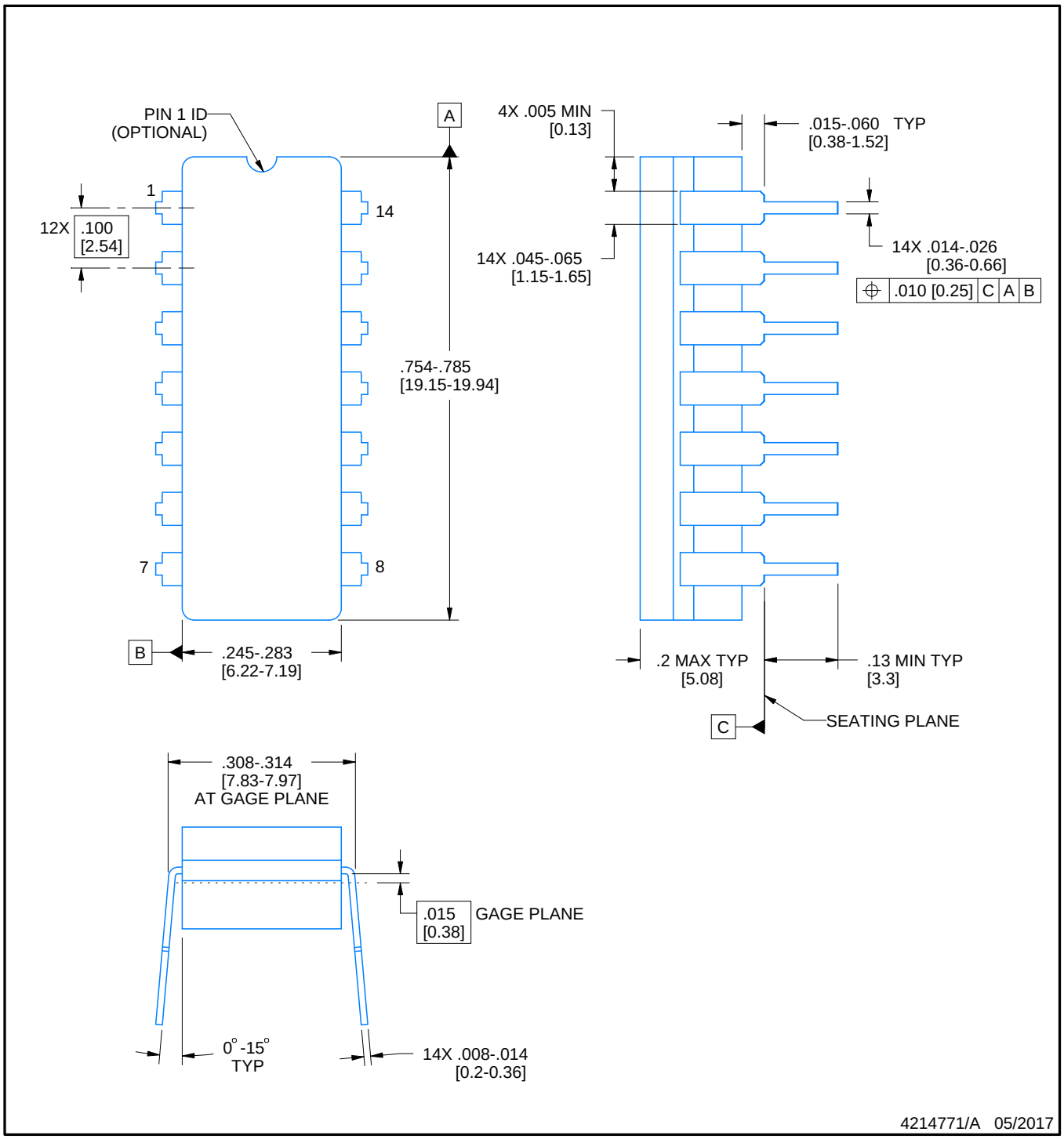


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

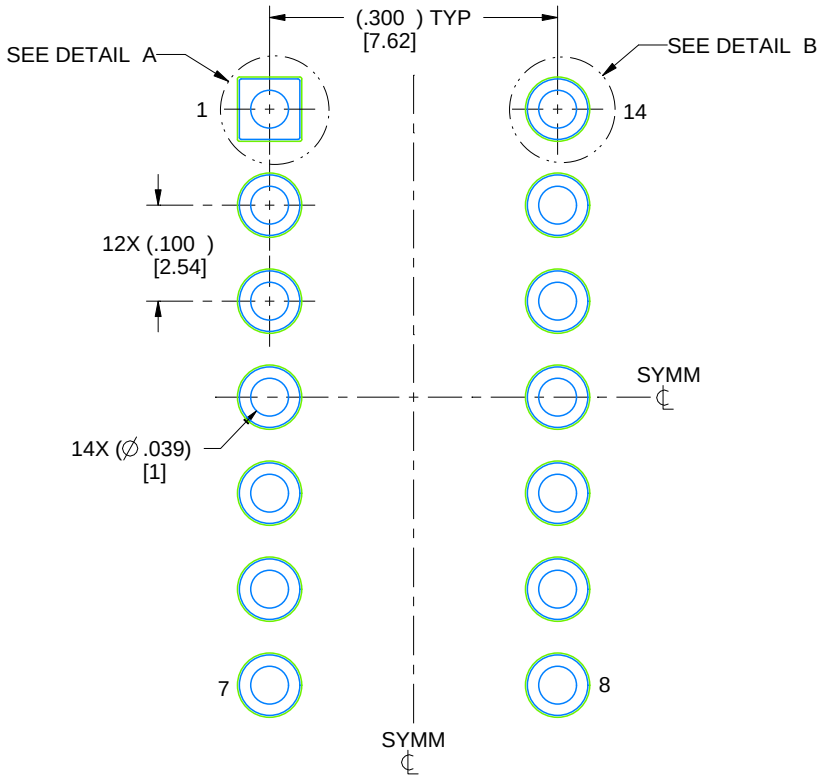
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

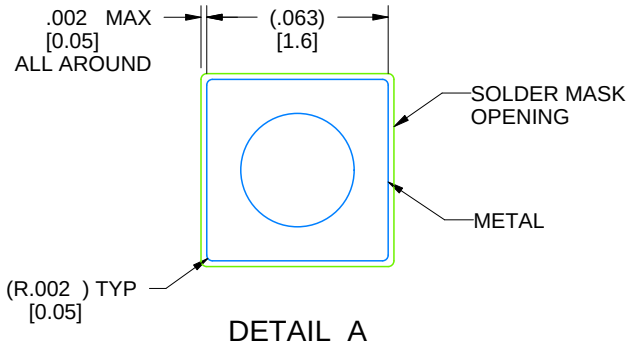
J0014A

CDIP - 5.08 mm max height

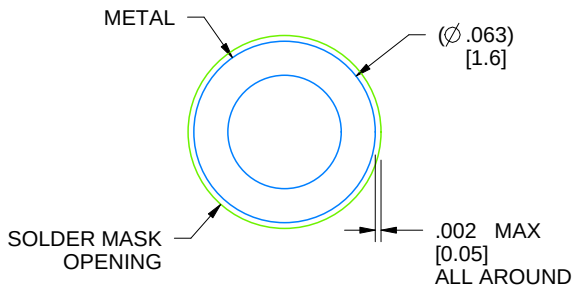
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



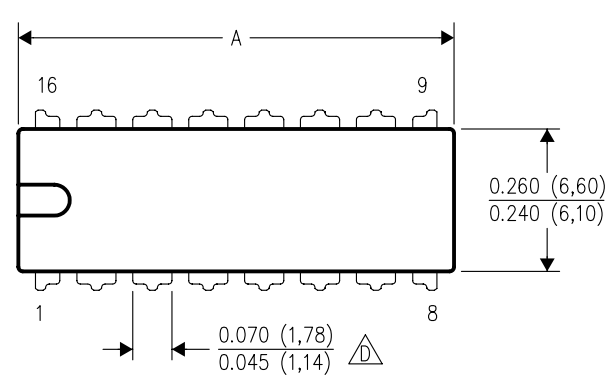
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

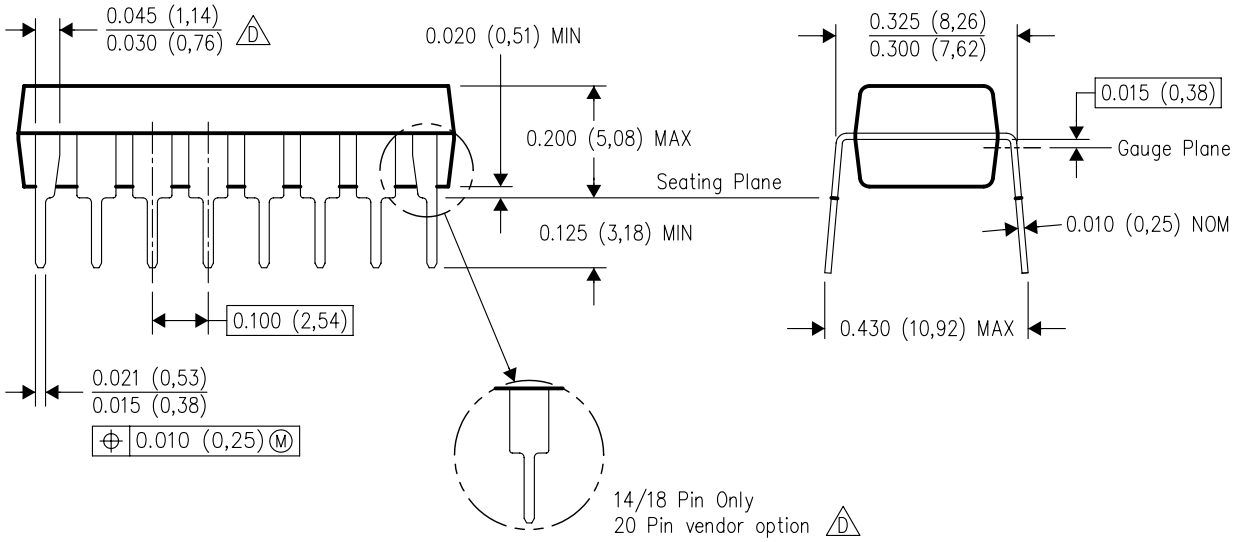
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

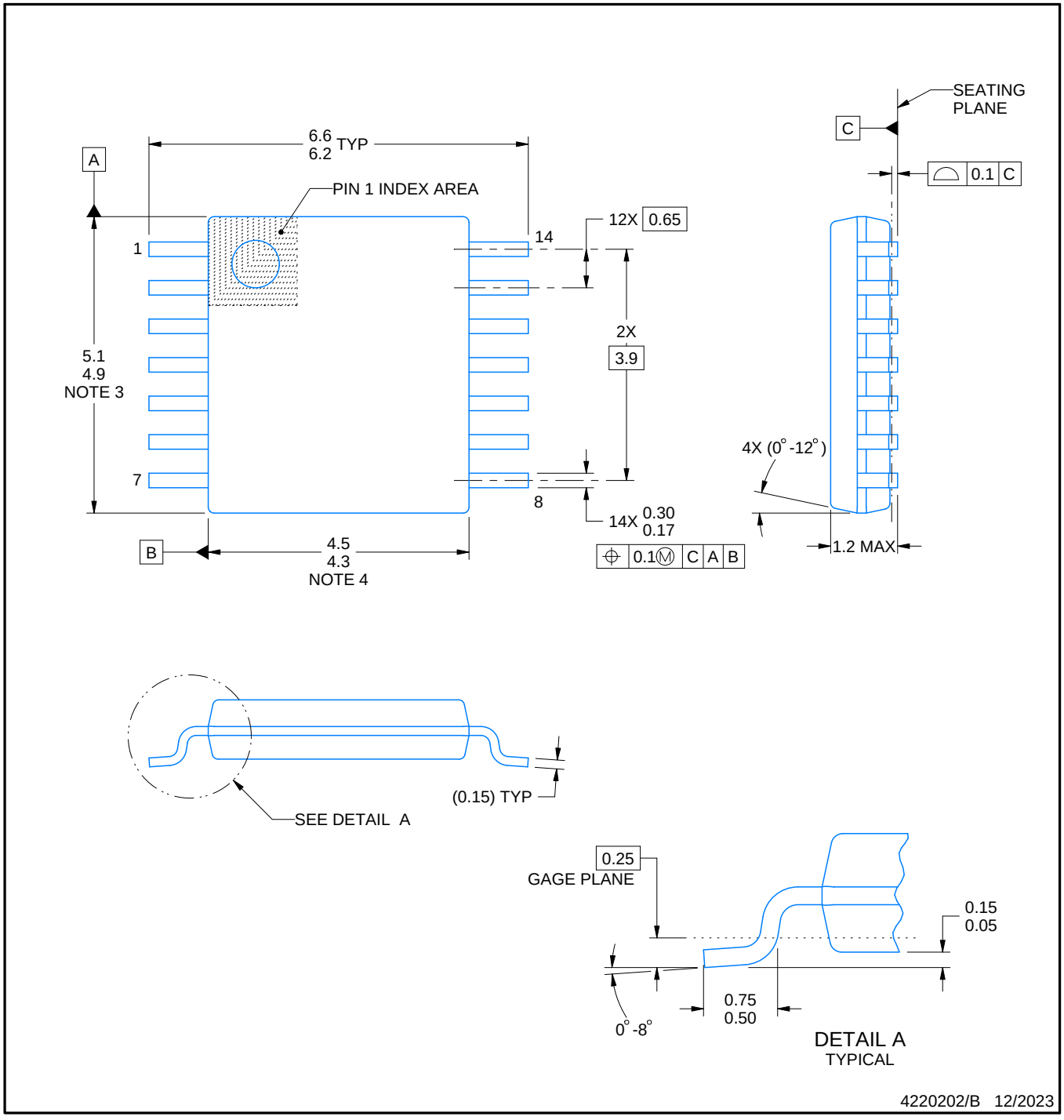
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

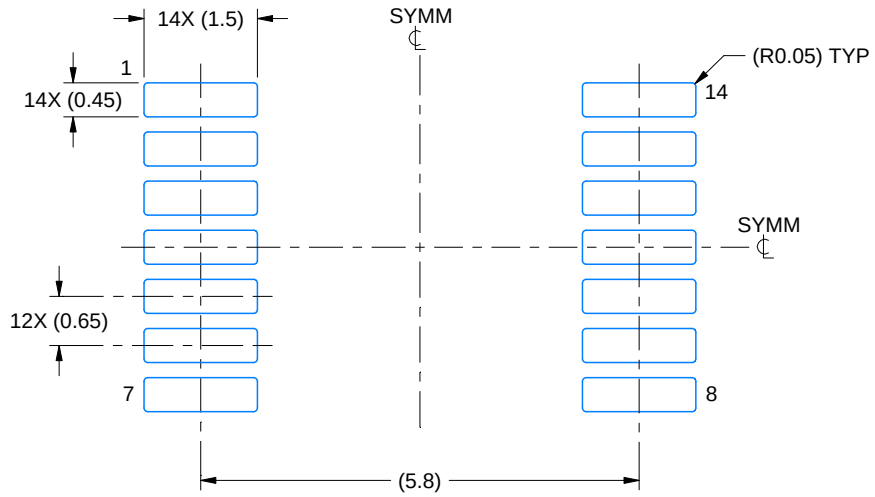
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

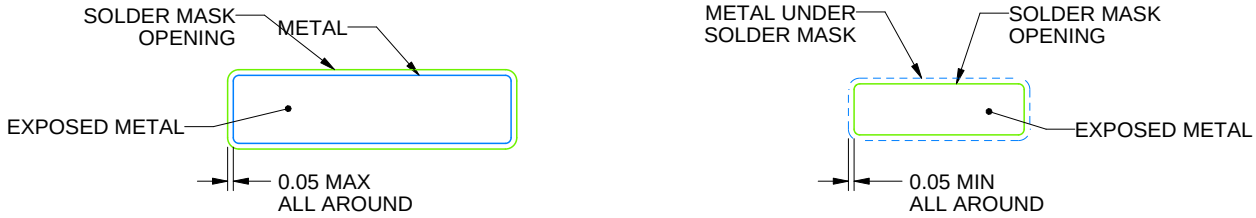


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

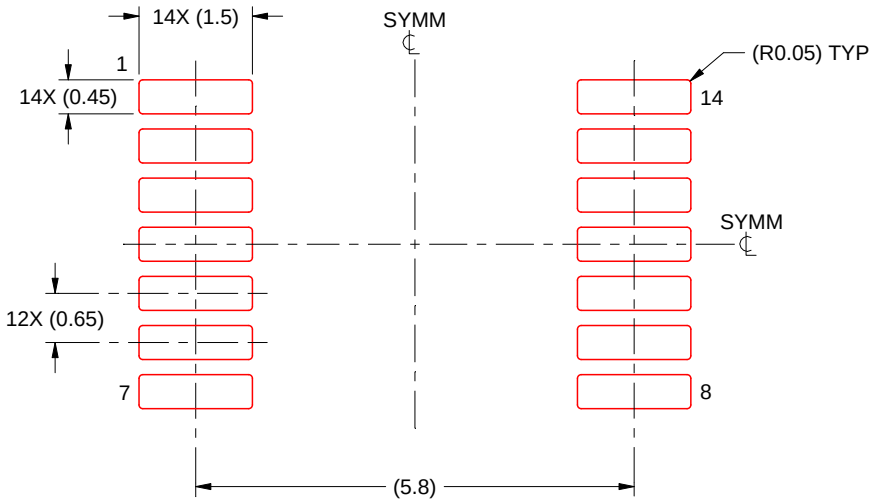


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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