Data Sheet July 1999 File Number 2275.5

75A, 50V, 0.008 Ohm, N-Channel Power MOSFET

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09821.

Ordering Information

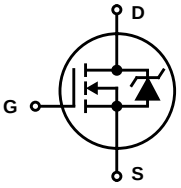
PART NUMBER	PACKAGE	BRAND
RFG75N05E	TO-247	RFG75N05E

NOTE: When ordering, include the entire part number.

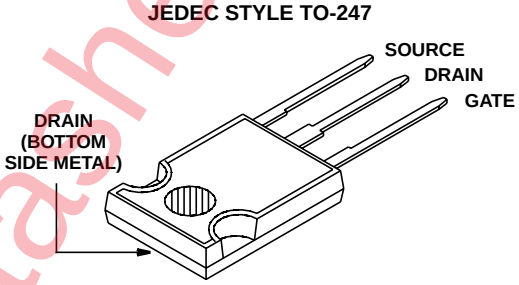
Features

- 75A, 50V
- $r_{DS(ON)} = 0.008\Omega$
- Electrostatic Discharge Rated
- UIS Rating Curve (Single Pulse)
- 175^{o}C Operating Temperature
- Temperature Compensated PSPICE® Model Provided

Symbol



Packaging



www.datasheet.live

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD Handling Procedures.
PSPICE® is a registered trademark of MicroSim Corporation.
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Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFG75N05E	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	50	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	50	V
Continuous Drain Current (Current Limited by Package)	I_D	75	A
Pulsed Drain Current (Note 3)	I_{DM}	200	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	240	W
Linear Derating Factor		1.6	$W/^oC$
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	E_{SD}	2	kV
Single Pulse Avalanche Rating (Note 4)		Refer to UIS SOA Curves	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA (Figure 9)		50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 8)		2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 150^oC$		-	-	25	μA
Gate to Source Leakage	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source on Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 75A (Figure 7)		-	-	0.008	Ω
Turn On Time	$t_{(ON)}$	V_{DD} = 25V, $I_D \approx$ 37.5A, R_L = 0.67Ω, R_G = 1.67Ω, V_{GS} = 10V, (Figure 11)		-	-	125	ns
Turn On Delay Time	$t_{d(ON)}$			-	17	-	ns
Rise Time	t_r			-	75	-	ns
Turn Off Delay Time	$t_{d(OFF)}$			-	70	-	ns
Fall Time	t_f			-	17	-	ns
Turn Off Time	$t_{(OFF)}$			-	-	125	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 0, 20V	V_{DD} = 40V, I_D = 75A, R_L = 0.53Ω $I_{G(REF)}$ = 3.44mA (Figure 11)	-	-	400	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0, 10V		-	-	220	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0, 2V		-	-	15	nC
Junction to Case	$R_{\theta JC}$			-	-	0.625	$^oC/W$
Junction to Ambient	$R_{\theta JA}$			-	-	80	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 75A	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 75A, dI_{SD}/dt = 100A/μs	-	-	125	ns

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive pulse: pulse width is limited by maximum junction temperature.
4. Refer to Intersil Application Notes AN9321 and AN9322. See Figure 4.

Typical Performance Curves Unless Otherwise Specified

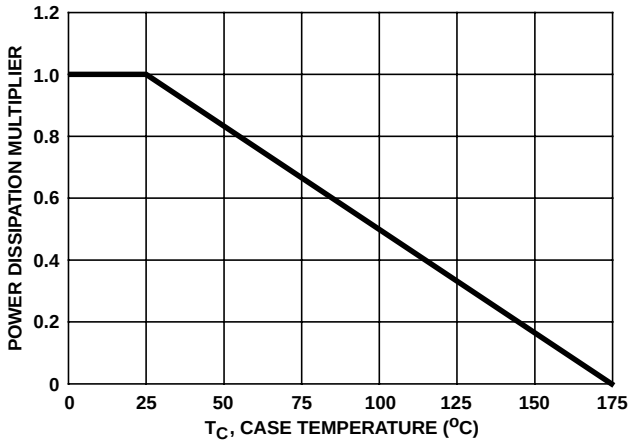


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

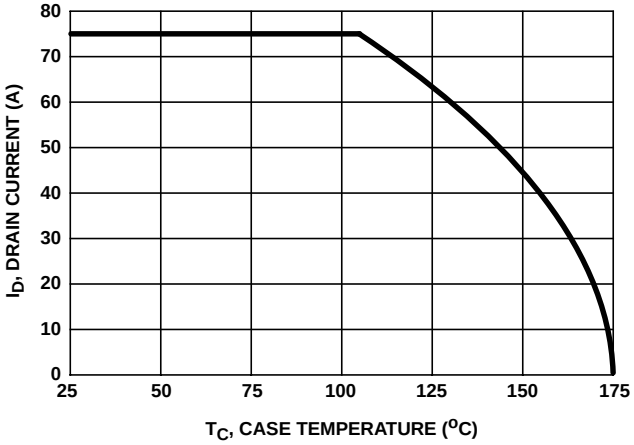


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

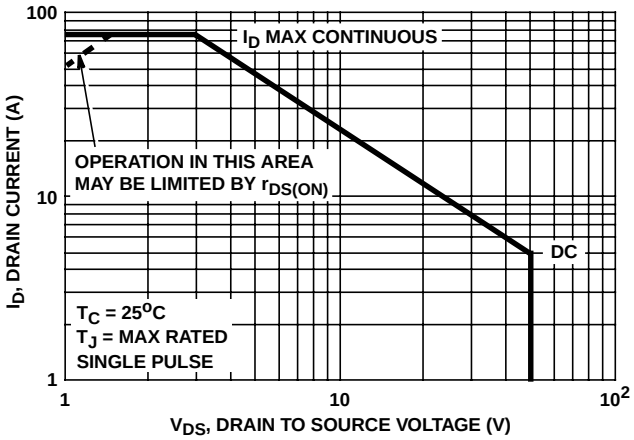


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

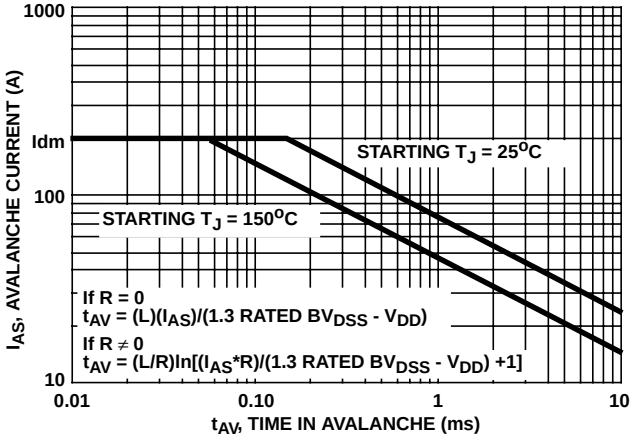


FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING SOA (SINGLE PULSE UIS SOA)

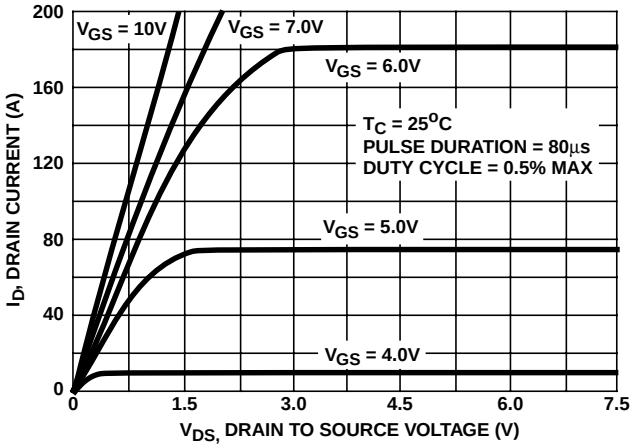


FIGURE 5. SATURATION CHARACTERISTICS

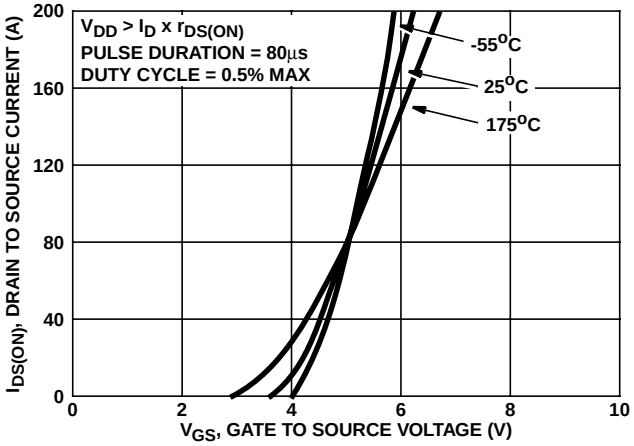


FIGURE 6. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

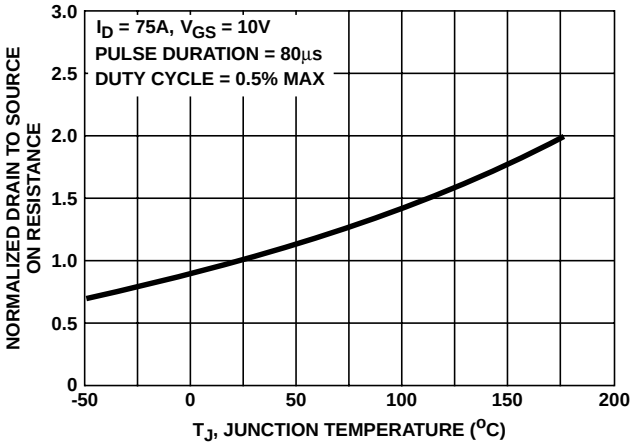


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

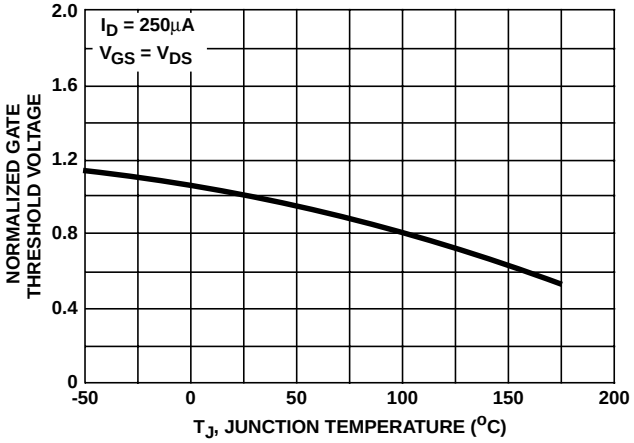


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

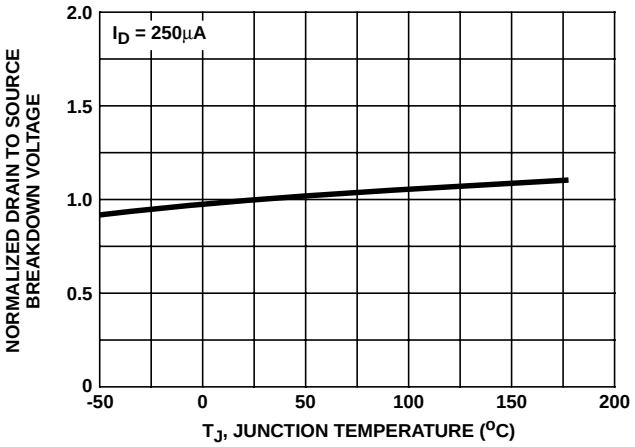


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

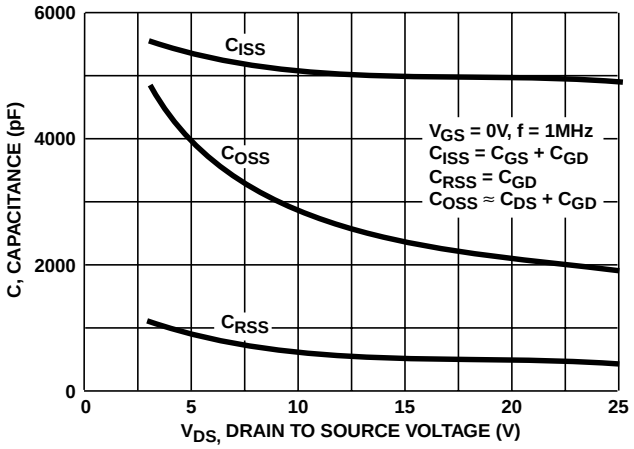
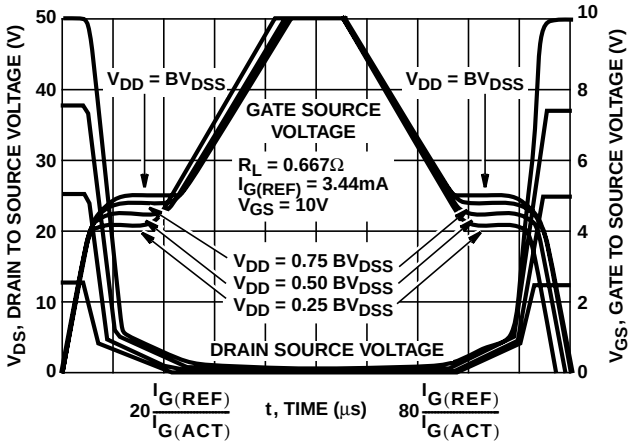


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

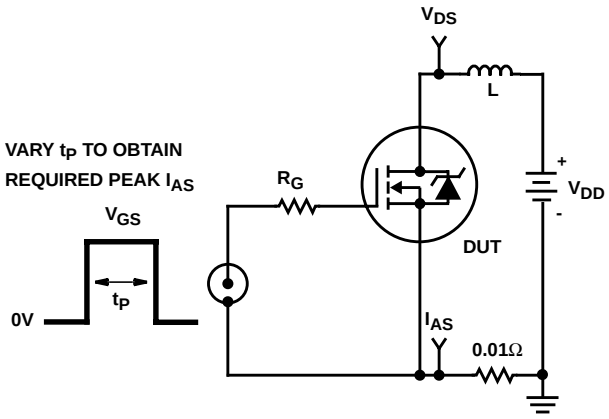


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

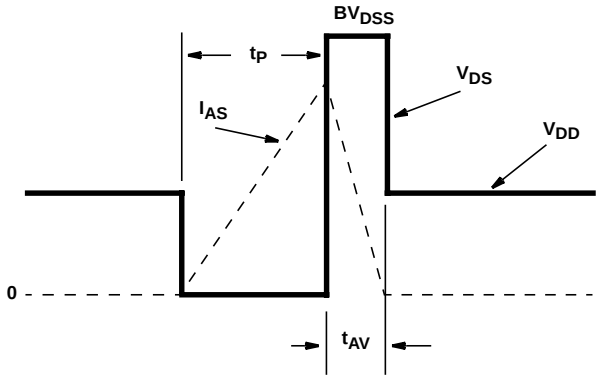


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

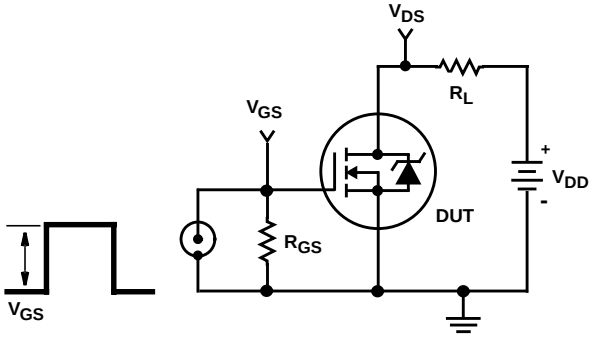


FIGURE 14. SWITCHING TIME TEST CIRCUIT

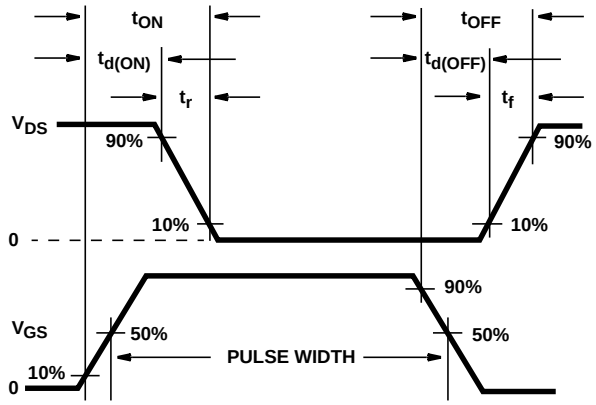


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

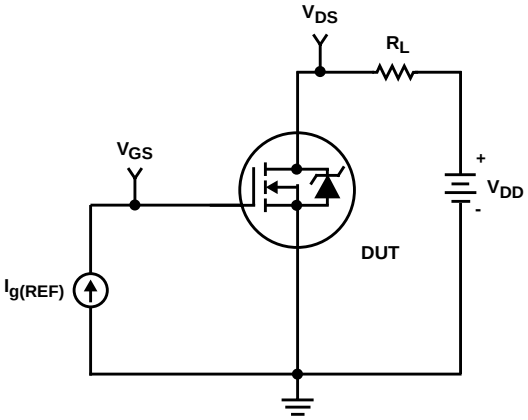


FIGURE 16. GATE CHARGE TEST CIRCUIT

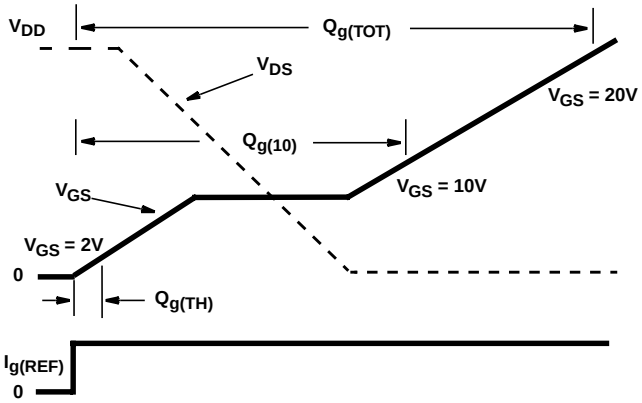
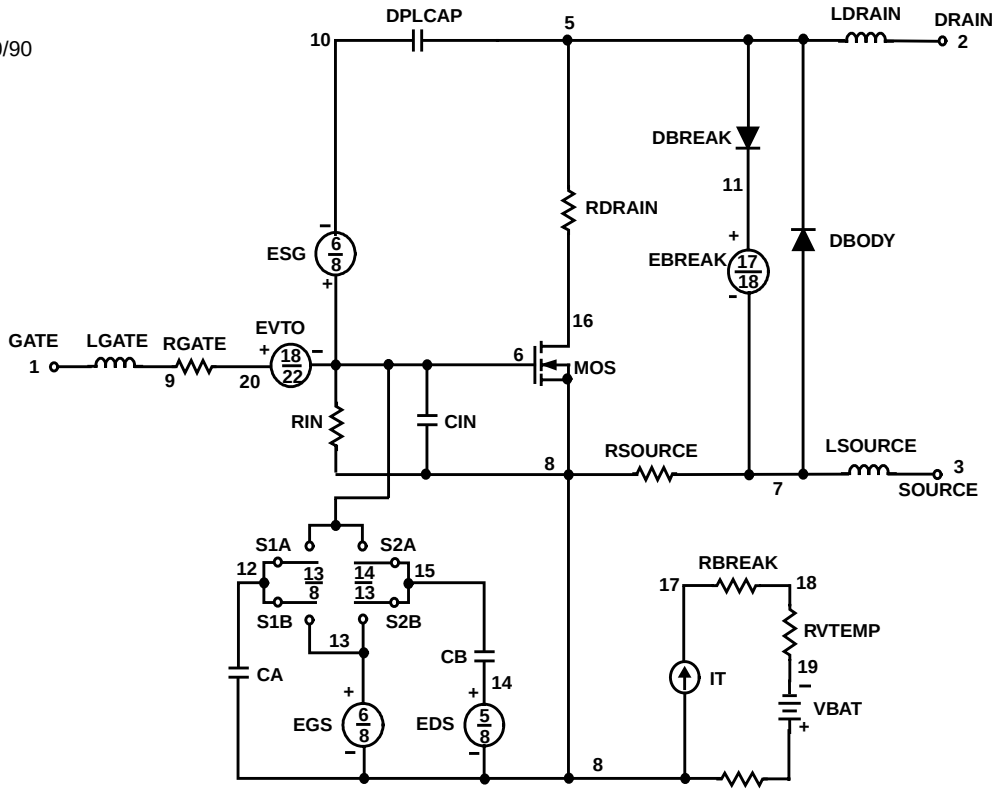


FIGURE 17. GATE CHARGE WAVEFORM

PSpice Electrical Model




```
.SUBCKT RFG75N05 2 1 3 ; rev 10/30/90
*Nominal Temperature = 25°C
CA 12 8 8.98e-9
CB 15 14 8.81e-9
Cin 6 8 4.48e-9
DPLCAP 10 5 DPLCAPMOD
Dbody 7 5 DBODYMOD
Dbreak 5 11 DBREAKMOD
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Ebreak 11 7 17 18 58.4
EVTEMP 20 6 18 8 1
IT 8 17 1
Ldrain 2 5 e-10
Lgate 1 9 5e-9
Lsource 3 7 3e-9
Mos 16 6 8 8 MODMOD
Rbreak 17 18 RBREAKMOD 1
Rdrain 5 16 RSOURCEMOD 3.07e-3
Rgate 9 20 1.2
Rin 6 8 1e9
Rsource 8 7 RSOURCEMOD 2.e-3
RVTEMP 18 19 RVTONEGMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2AMOD
Vbat 8 19 DC 1
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.48 VOFF=-0.48)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.48 VOFF=-2.48)
.MODEL S2AMOD VSWITCH (RON=1e=5 ROFF=0.1 VON=-2.25 VOFF=2.75)
.MODEL S2ABMOD VSWITCH (RON=1e-5 ROFF=0.1 VON =2.75 VOFF=-2.25)
.MODEL DBODYMOD D (IS=2.23e-12 RS=249e-3 TRS1=2.5e-3 CJO=7.55e-9 TT=4e-8)
.MODEL DBREAKMOD D (RS=8e-2 TRS1=2.5e-3)
.MODEL DPLCAPMOD D (IS=1e-30 N=10 CJO=2.14e-9)
.MODEL RBREAKMOD RES (TC1=9.5e-4 TC2=-1.17e-6)
.MODEL RSOURCEMOD RES (TC1=5.2e-3 TC2=1.37e-5)
.MODEL RVTONEGMOD RES (TC1=-3.78e-3 TC2=-7.51e-7)
.MODEL MODMOD NMOS (VTO=3.48 N=10 IS=1e-30 KP=78.5 TOX=1 L=1u W1u)
.ENDS
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