

MOSFET - N-Channel, Shielded Gate PowerTrench 120 V, 2.95 mΩ, 181 A

FDP2D9N12C

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)} = 2.95 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 181 \text{ A}$
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- 100% UIL Tested
- These Devices are Pb-Free, Halogen-Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	120	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Note 2)	Steady State	T _C = 25°C	I _D	181	A
Power Dissipation R _{θJC} (Note 2)			P _D	179	W
Continuous Drain Current R _{θJA} (Notes 1, 2)	Steady State	T _A = 25°C	I _D	19.5	A
Power Dissipation R _{θJA} (Notes 1, 2)			P _D	2.0	W
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		I _{DM}	933	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Source Current (Body Diode)			I _S	172	A
Single Pulse Drain-to-Source Avalanche Energy (I _{AV} = 99 A _{pk} , L = 0.1 mH)			E _{AS}	490	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T _L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

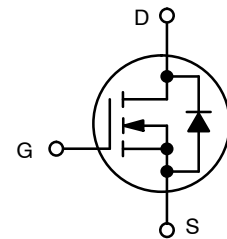
1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



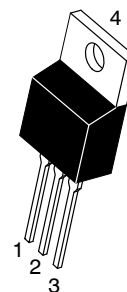
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
120 V	2.95 mΩ @ 10 V	181 A

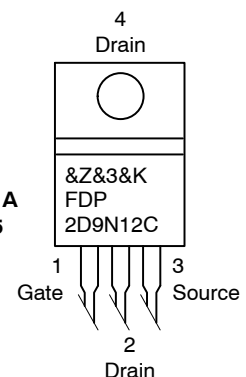


N-CHANNEL MOSFET



TO-220
CASE 221A
STYLE 5

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Date Code (Year & Week)
&K = Lot

ORDERING INFORMATION

Device	Package	Shipping†
FDP2D9N12C	TO-220 (Pb-Free)	50 / Tube, 800 / Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.7	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	62.5	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	120			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		46		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 96\text{ V}$			1	μA
		$T_J = 150^\circ\text{C}$			100	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 664\text{ }\mu\text{A}$	2.0	3.1	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 664\text{ }\mu\text{A}$, ref to 25°C		-8.6		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 95\text{ A}$		2.7	2.95	m Ω
		$V_{GS} = 6\text{ V}, I_D = 57\text{ A}$		3.5	5.1	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 10\text{ V}, I_D = 50\text{ A}$		215		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 60\text{ V}$		7910	12883	pF
Output Capacitance	C_{OSS}			3825		
Reverse Transfer Capacitance	C_{RSS}			32		
Gate-Resistance	R_G			0.78	1.9	Ω
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 60\text{ V}; I_D = 95\text{ A}$		98	137	nC
Threshold Gate Charge	$Q_{G(TH)}$			23		
Gate-to-Source Charge	Q_{GS}			35		
Gate-to-Drain Charge	Q_{GD}			15		
Plateau Voltage	V_{GP}			5.0		
Output Charge	Q_{OSS}	$V_{DD} = 60\text{ V}, V_{GS} = 0\text{ V}$		325		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 60\text{ V}, I_D = 95\text{ A}, R_G = 6.0\text{ }\Omega$		43		ns
Rise Time	t_r			31		
Turn-Off Delay Time	$t_{d(OFF)}$			72		
Fall Time	t_f			24		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 95\text{ A}$	$T_J = 25^\circ\text{C}$		0.9	1.3	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, V_{DD} = 60\text{ V}$ $dI_S/dt = 300\text{ A}/\mu\text{s}, I_S = 100\text{ A}$			88		ns
Charge Time	t_a				48		
Discharge Time	t_b				40		
Reverse Recovery Charge	Q_{RR}				500		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

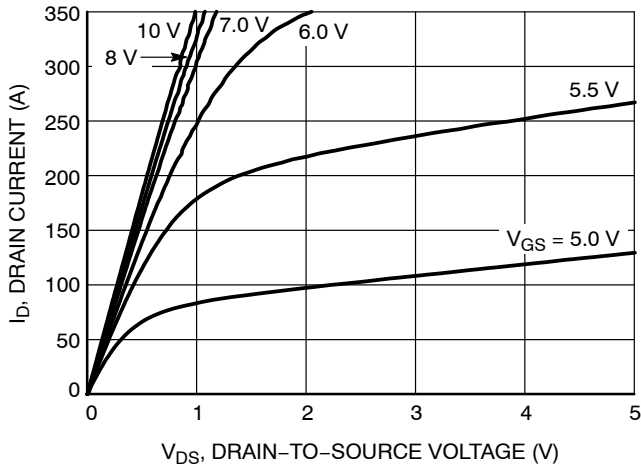


Figure 1. On-Region Characteristics

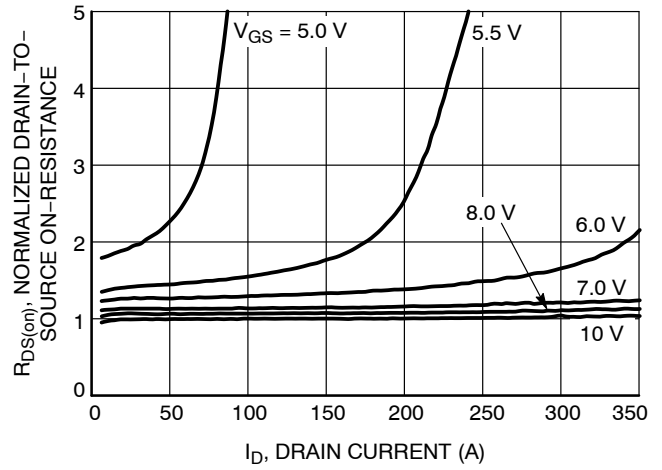


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

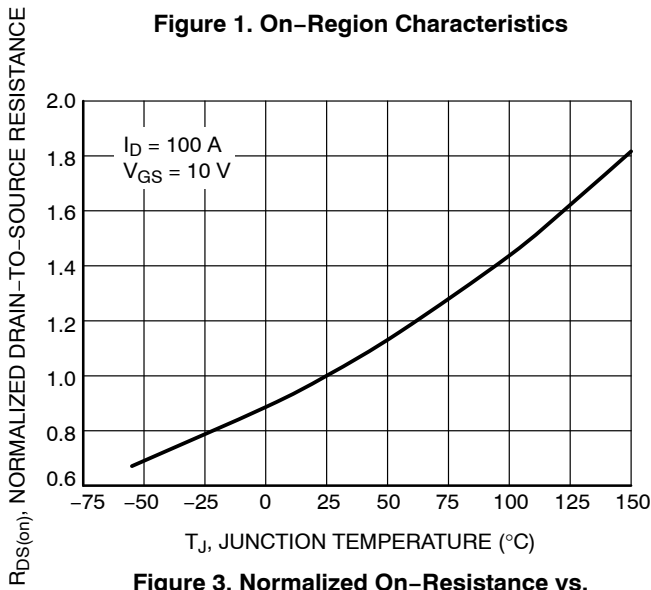


Figure 3. Normalized On-Resistance vs. Junction Temperature

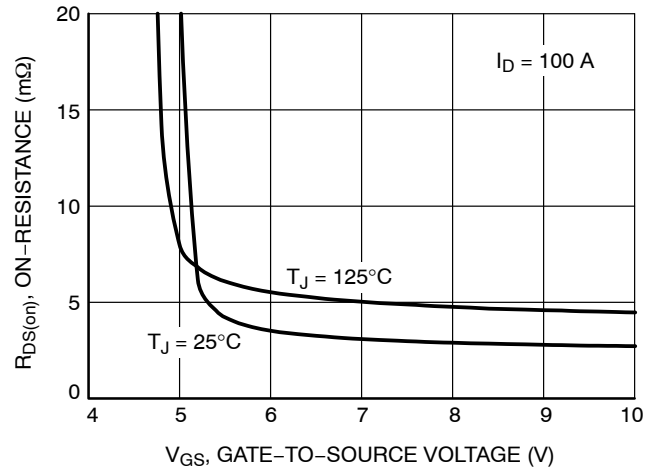


Figure 4. On-Resistance vs. Gate-to-Source Voltage

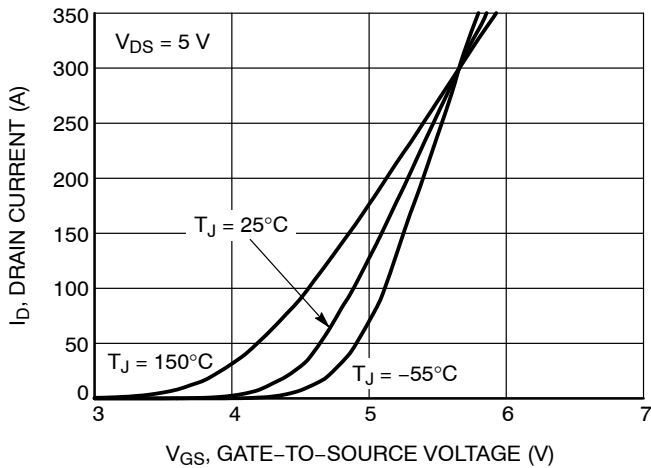


Figure 5. Transfer Characteristics

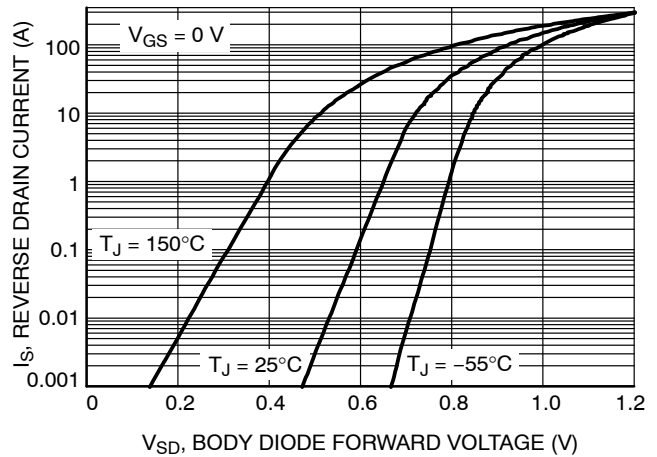


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS

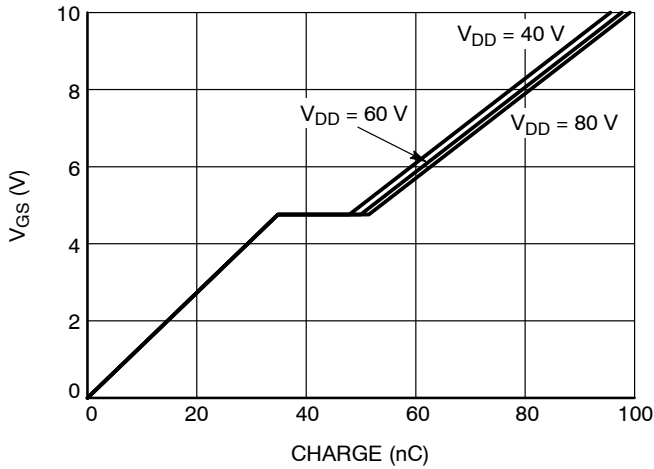


Figure 7. Gate Charge Characteristics

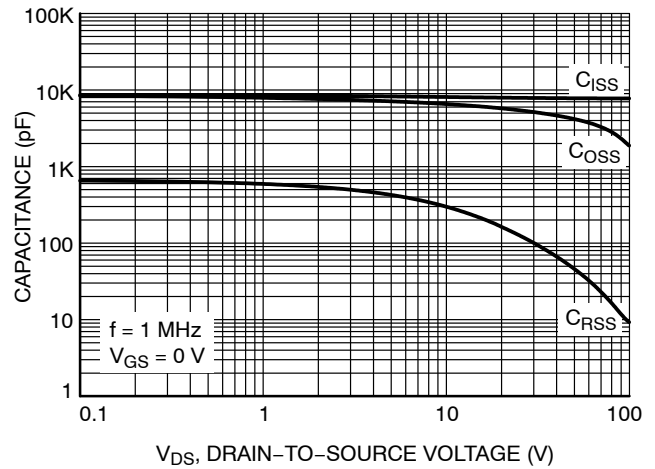


Figure 8. Capacitance vs. Drain-to-Source Voltage

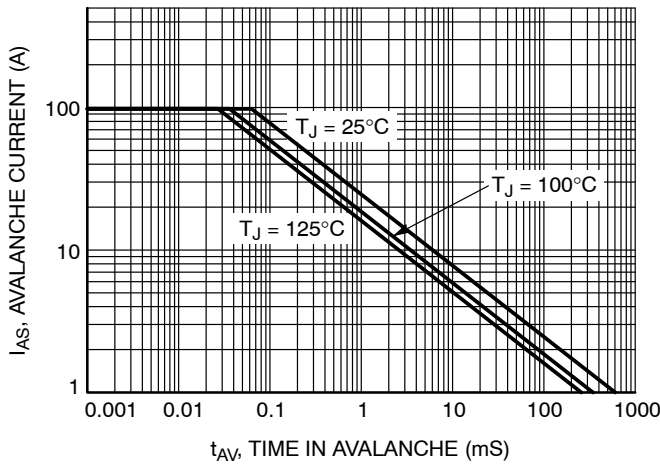


Figure 9. Unclamped Inductive Switching Capability

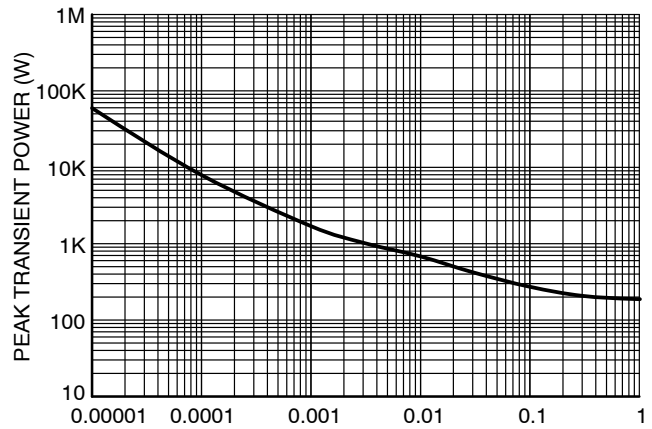


Figure 10. Peak Power

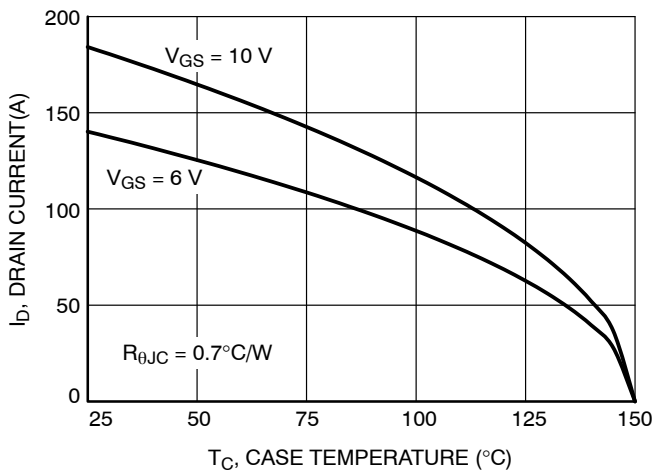


Figure 11. Drain Current vs. Case Temperature

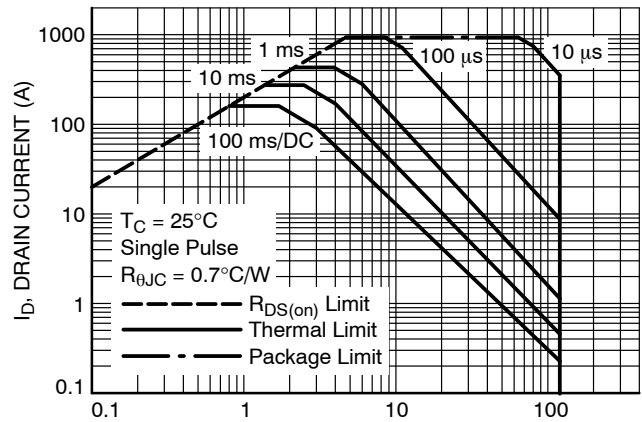


Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS

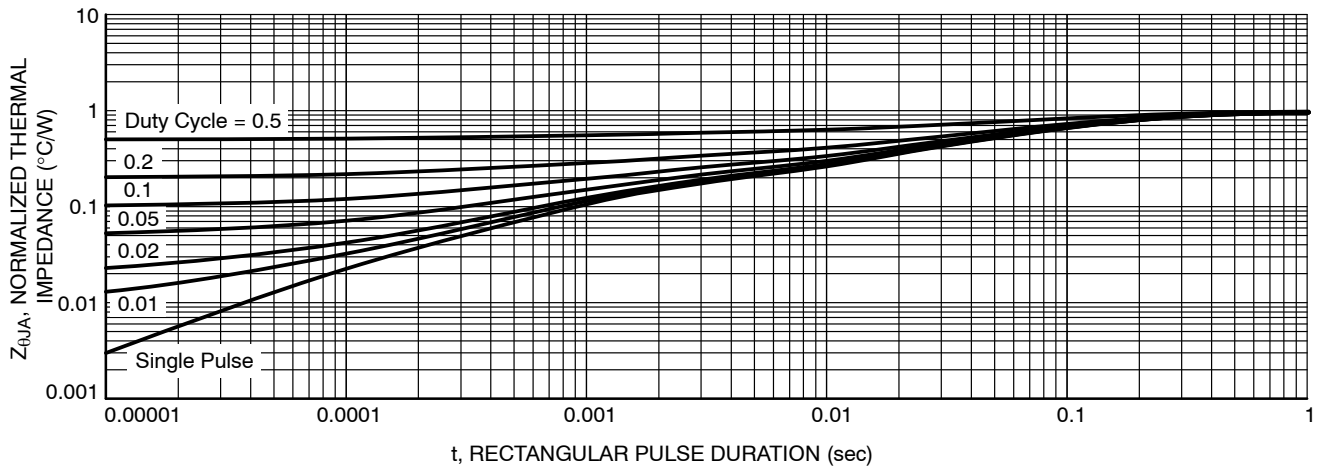
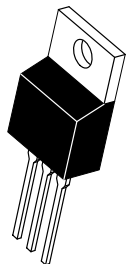
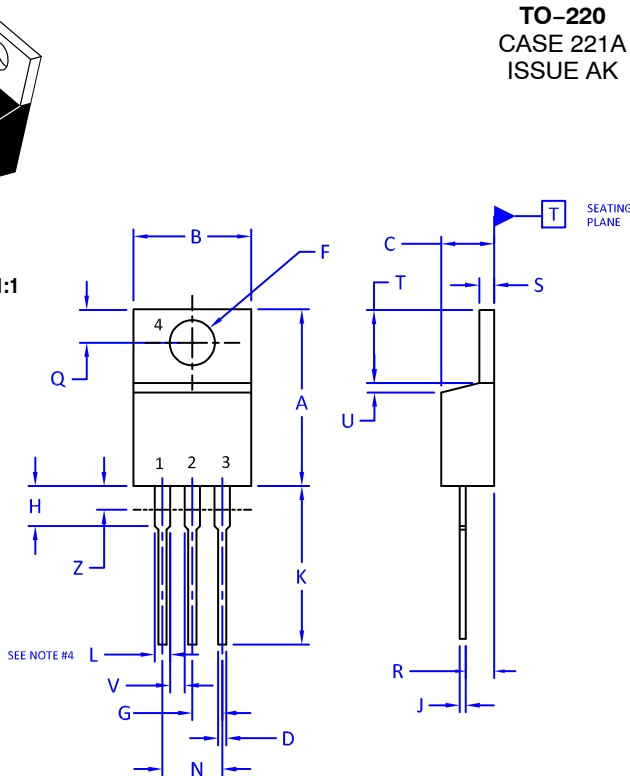


Figure 13. Transient Thermal Impedance



SCALE 1:1



TO-220
CASE 221A
ISSUE AK

DATE 13 JAN 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:

- PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:

- PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:

- PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:

- PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:

- PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:

- PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:

- PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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