

NTD78N03

Power MOSFET

25 V, 78 A, Single N-Channel, DPAK

Features

- Low $R_{DS(on)}$
- Optimized Gate Charge
- Pb-Free Packages are Available

Applications

- Desktop VCORE
- DC-DC Converters
- Low Side Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	25	V
Gate-to-Source Voltage			V _{GS}	± 20	V
Continuous Drain Current (Note 1)	Steady State	T _C = 25°C	I _D	14.8	A
		T _C = 85°C		11.5	
Power Dissipation (Note 1)		T _C = 25°C	P _D	2.3	W
Continuous Drain Current (Note 2)		T _C = 25°C	I _D	11.4	A
		T _C = 85°C		8.8	
Power Dissipation (Note 2)		T _C = 25°C	P _D	1.4	W
Continuous Drain Current (R _{θJC})		T _C = 25°C	I _D	78	A
		T _C = 85°C		56	
Power Dissipation (R _{θJC})		T _C = 25°C	P _D	64	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	210	A
Current Limited by Package		T _A = 25°C	I _{DmaxPkg}	45	A
Drain to Source dV/dt			dV/dt	8.0	V/ns
Operating Junction and Storage Temperature			T _J , T _{stg}	−55 to 175	°C
Source Current (Body Diode)			I _S	78	A
Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 24 V, V _{GS} = 10 V, L = 5.0 mH, I _{L(pk)} = 17 A, R _G = 25 Ω)			E _{AS}	722.5	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			T _L	260	°C

THERMAL RESISTANCE

Junction-to-Case (Drain)	$R_{\theta JC}$	1.95	$^\circ\text{C/W}$
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	65	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	110	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

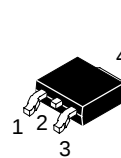
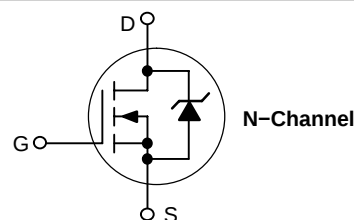
1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size.



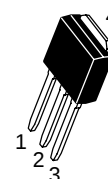
ON Semiconductor®

<http://onsemi.com>

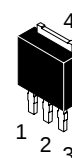
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
25 V	4.6 @ 10 V	78 A
	6.5 @ 4.5 V	



CASE 369AA
DPAK
(Bend Lead)
STYLE 2

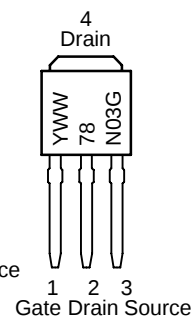
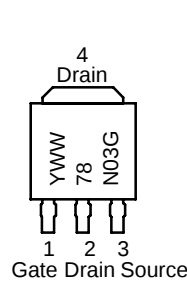
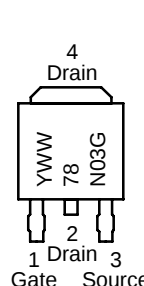


CASE 369D
DPAK
(Straight Lead)
STYLE 2



CASE 369AD
IPAK
(Straight Lead)

MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year
WW = Work Week
78N03 = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD78N03

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			24		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 20 V			1.5	μA
					10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.0	1.6	3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-5.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 78 A		4.6	6.0	mΩ
		V _{GS} = 4.5 V, I _D = 36 A		6.5	7.8	
Forward Transconductance	g _{FS}	V _{DS} = 10 V, I _D = 15 A		22		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 12 V		1920	2250	pF
Output Capacitance	C _{oss}			960		
Reverse Transfer Capacitance	C _{rss}			420		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 20 V, I _D = 20 A		25.5	35	nC
Threshold Gate Charge	Q _{G(TH)}			2.4		
Gate-to-Source Charge	Q _{GS}			5.3		
Gate-to-Drain Charge	Q _{GD}			18.2		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 4.5 V, V _{DS} = 20 V, I _D = 20 A, R _G = 3.0 Ω		11		ns
Rise Time	t _r			68		
Turn-Off Delay Time	t _{d(off)}			23		
Fall Time	t _f			42		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 20 A	T _J = 25°C		0.83	1.0	V
			T _J = 125°C		0.7		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /d _t = 100 A/μs, I _S = 20 A		39		ns	
Charge Time	t _a			17.8			
Discharge Time	t _b			21			
Reverse Recovery Time	Q _{RR}			33		nC	

PACKAGE PARASITIC VALUES

Source Inductance	L _S	Ta = 25C		2.49		nH
Drain Inductance	L _D			0.02		
Gate Inductance	L _G			3.46		
Gate Resistance	R _G			1.0		Ω

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

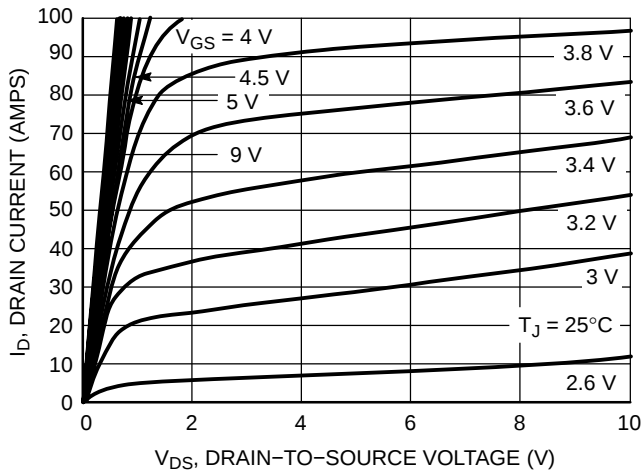


Figure 1. On-Region Characteristics

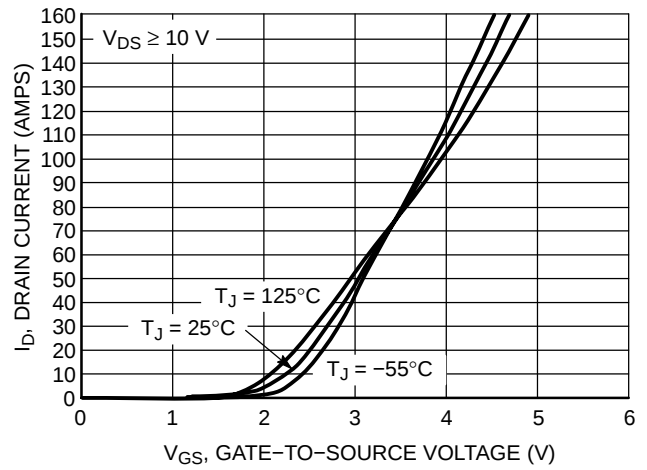


Figure 2. Transfer Characteristics

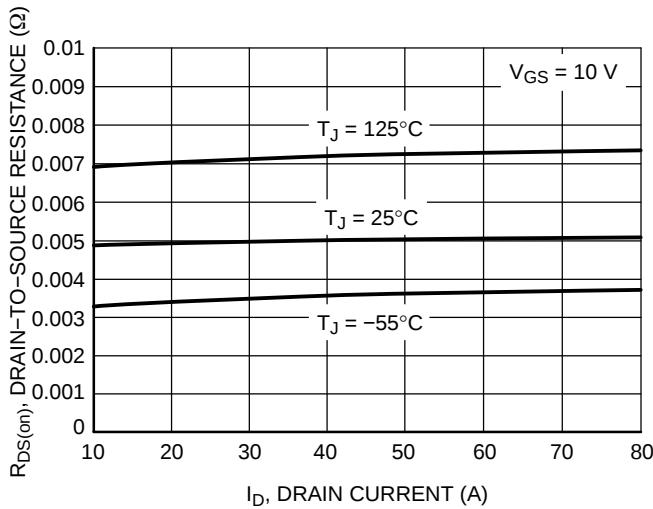


Figure 3. On-Resistance versus Drain Current and Temperature

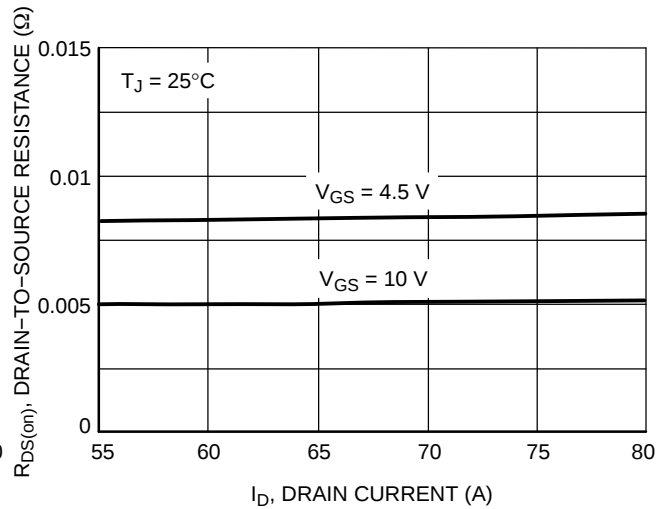


Figure 4. On-Resistance versus Drain Current and Gate Voltage

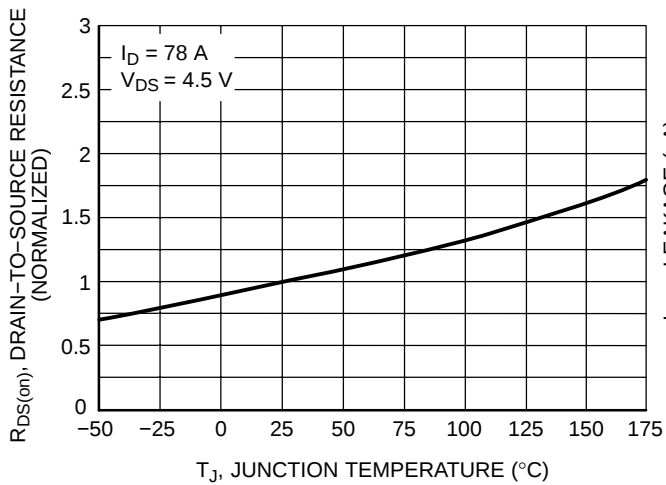


Figure 5. On-Resistance Variation with Temperature

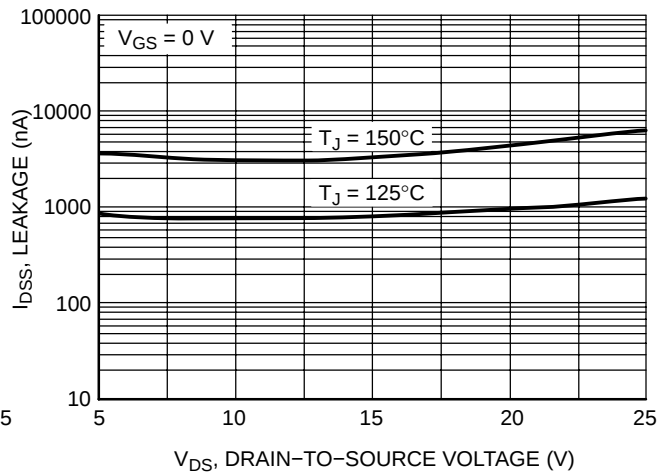
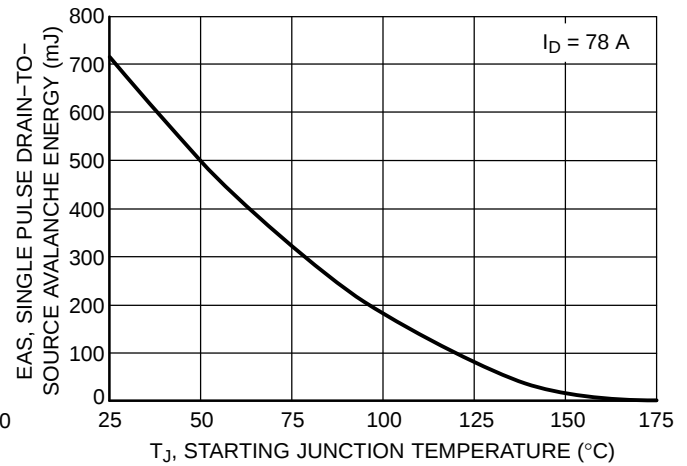
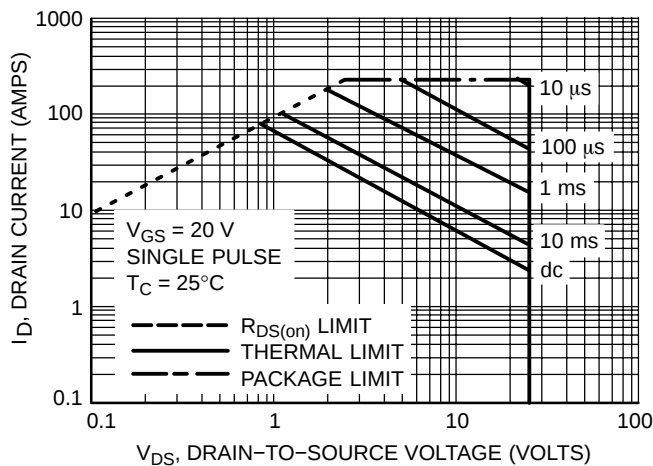
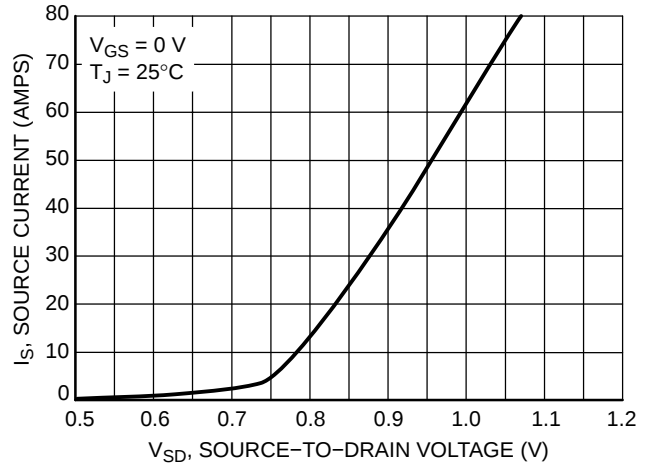
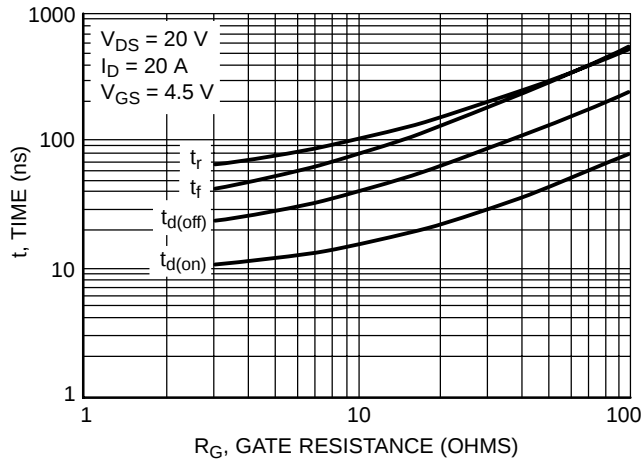
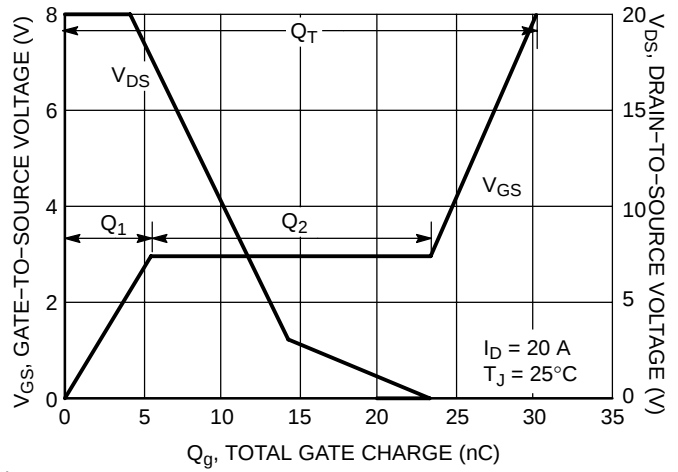
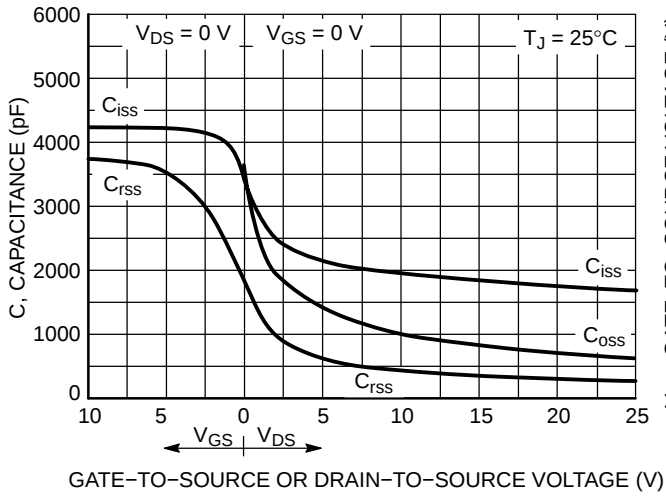


Figure 6. Drain-To-Source Leakage Current versus Voltage



NTD78N03

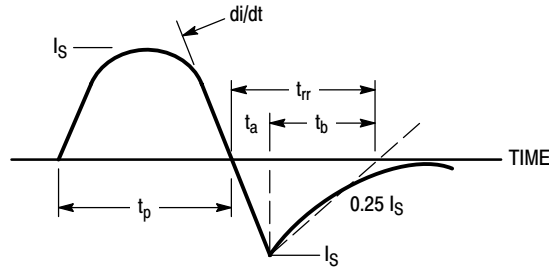


Figure 13. Diode Reverse Recovery Waveform

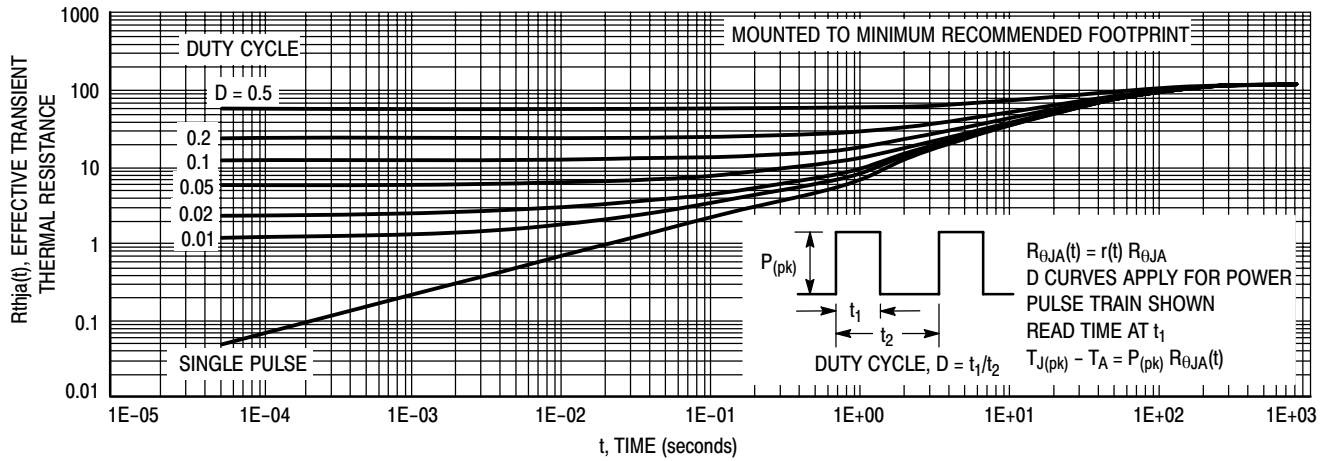
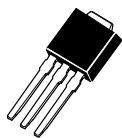


Figure 14. Thermal Response – Various Duty Cycles

ORDERING INFORMATION

Order Number	Package	Shipping [†]
NTD78N03	DPAK	75 Units/Rail
NTD78N03G	DPAK (Pb-Free)	75 Units/Rail
NTD78N03T4	DPAK	2500 Tape & Reel
NTD78N03T4G	DPAK (Pb-Free)	
NTD78N03-1	DPAK Straight Lead	75 Units/Rail
NTD78N03-1G	DPAK Straight Lead (Pb-Free)	
NTD78N03-35	DPAK-3 Straight Lead (3.5 ± 0.15 mm)	75 Units/Rail
NTD78N03-35G	DPAK-3 Straight Lead (3.5 ± 0.15 mm) (Pb-Free)	

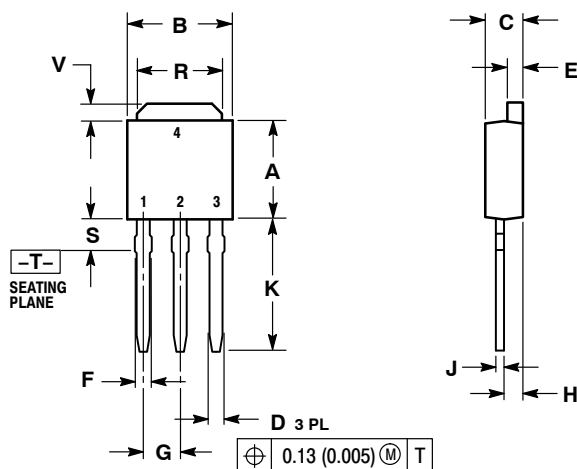
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



DPAK INSERTION MOUNT
CASE 369
ISSUE O

DATE 02 JAN 2000

SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

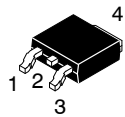
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

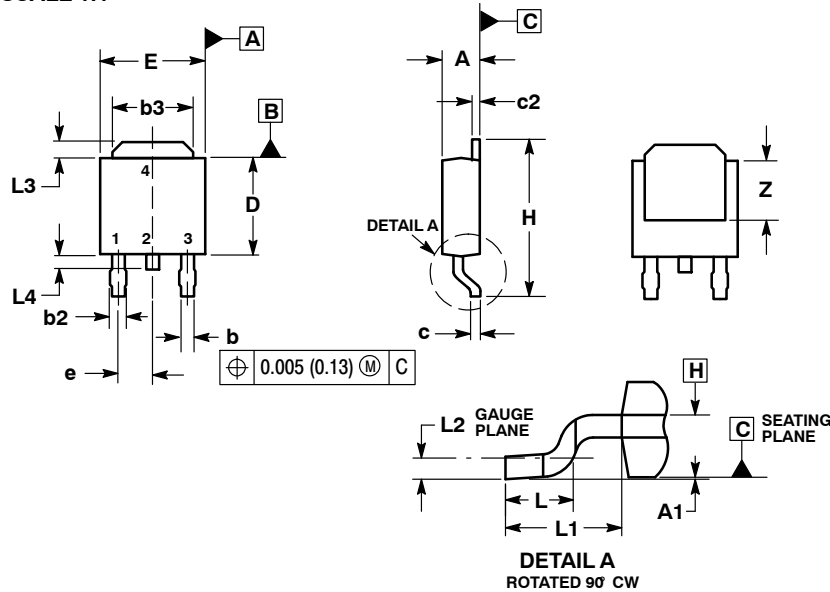
STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

DOCUMENT NUMBER:	98ASB42319B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK INSERTION MOUNT	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



SCALE 1:1



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

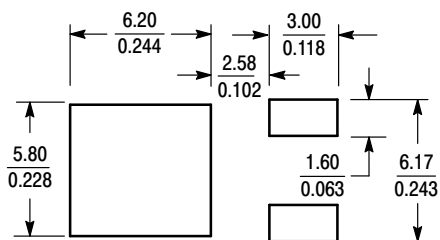
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

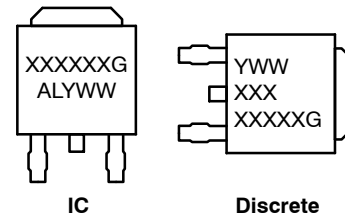
*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	0.040		1.01	
Z	0.155		3.93	

GENERIC
MARKING DIAGRAM*

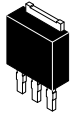


XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

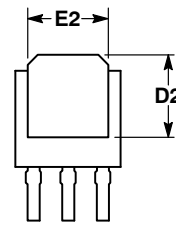
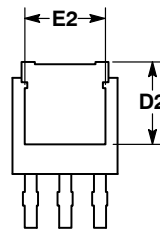
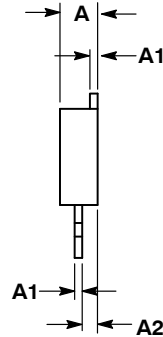
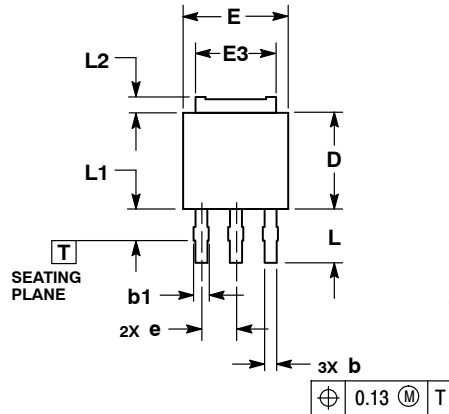
DOCUMENT NUMBER:	98AON13126D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.


3.5 MM IPAK, STRAIGHT LEAD
CASE 369AD
ISSUE B

DATE 18 APR 2013

SCALE 1:1


**OPTIONAL
CONSTRUCTION**
NOTES:

- 1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	---
E	6.35	6.73
E2	4.57	5.45
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	---	2.10
L2	0.89	1.27

**GENERIC MARKING
DIAGRAMS***
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

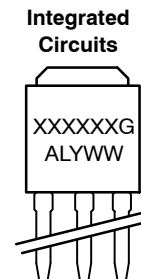
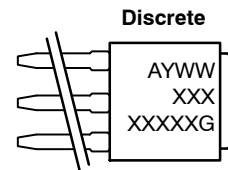
STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR


XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

DOCUMENT NUMBER:	98AON23319D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	3.5 MM IPAK, STRAIGHT LEAD	PAGE 1 OF 1

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales