



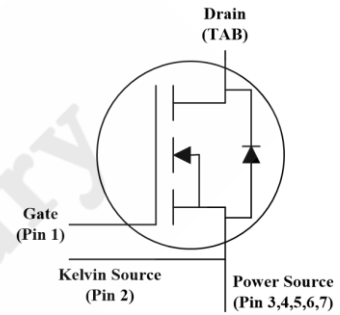
P3M06060G7 SiC MOS N-Channel Enhancement Mode

V_{RRM}	=	650	V
I_D	=	44	A
$I_D(100^\circ\text{C})$	=	31	A
$R_{DS(on)}$	=	60	m Ω

SiC MOS P3M06060G7 N-Channel Enhancement Mode

Features

- Qualified to AEC-Q101
- High Blocking Voltage with Low On-Resistance
- High-Frequency Operation
- Ultra-Small Q_{gd}
- 100% UIS tested



Benefits

- Improve System Efficiency
- Increase Power Density
- Reduce Heat Sink Requirements
- Reduction of System Cost

Applications

- Solar Inverters
- EV Battery Chargers
- High Voltage DC/DC Converters
- Switch Mode Power Supplies

TO-263-7

Drain	TAB
Gate	1
Kelvin Source	2
Power Source	3~7



Order Information

Part Number	Package	Marking
P3M06060G7	TO-263-7	P3M06060G7



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1. Maximum Ratings

At $T_J = 25^\circ\text{C}$, unless specified otherwise

Parameter	Symbol	Value	Unit	Test Conditions
Drain - Source Voltage	V_{DSmax}	650	V	$V_{GS} = -3\text{V}$ $I_D = 100\mu\text{A}$
Gate - Source Voltage (dynamic)	V_{GSmax}	-8 / +20	V	AC ($f > 1\text{ Hz}$)
Gate - Source Voltage (static)	V_{GSop}	-3 / +15	V	Static
Continuous Drain Current	I_D	44	A	$V_{GS} = 15\text{V}$ $T_C = 25^\circ\text{C}$
		31		$V_{GS} = 15\text{V}$ $T_C = 100^\circ\text{C}$
Power Dissipation	P_D	159	W	
Operating Junction Temperature	T_J	-55 To +175	$^\circ\text{C}$	
Storage Temperature	T_{stg}	-55 To +175	$^\circ\text{C}$	
Solder Temperature	T_L	245	$^\circ\text{C}$	



2. Electrical Characteristics

At $T_J = 25^\circ\text{C}$, unless specified otherwise

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650	/	/	V	$V_{GS} = -3\text{V}$ $I_D = 100\mu\text{A}$
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.2	/	V	(tested after 30ms pulse at $V_{GS} = 15\text{V}$) $V_{DS} = V_{GS}$ $I_D = 20\text{mA}$ $T_J = 25^\circ\text{C}$
		/	1.65	/	V	$V_{DS} = V_{GS}$ $I_D = 20\text{mA}$ $T_J = 175^\circ\text{C}$
Reverse Bias Drain Current	I_{DSS}	/	0.5	10	μA	$V_{GS} = -3\text{V}$ $V_{DS} = 650\text{V}$
Gate-Source Leakage Current	I_{GSS}	/	20	250	nA	$V_{GS} = 15\text{V}$ $V_{DS} = 0\text{V}$
Drain-Source On-State Resistance	$R_{DS(on)}$	/	60	79	m Ω	$V_{GS} = 15\text{V}$ $I_D = 20\text{A}$
		/	52	/		$V_{GS} = 18\text{V}$ $I_D = 20\text{A}$
Trans conductance	g_{fs}	/	12	/	S	$V_{DS} = 20\text{V}$ $I_{DS} = 20\text{A}$ $T_J = 25^\circ\text{C}$
		/	11	/		$V_{DS} = 20\text{V}$ $I_{DS} = 20\text{A}$ $T_J = 175^\circ\text{C}$



P3M06060G7 SiC MOS N-Channel Enhancement Mode

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Input Capacitance	C_{iss}	/	1911	/	pF	$V_{GS} = 0V$ $V_{DS} = 400V$ $f = 1MHz$ $V_{AC} = 25mV$
Output Capacitance	C_{oss}	/	162	/		
Reverse Transfer Capacitance	C_{rss}	/	15.3	/		
Coss Stored Energy	E_{oss}	/	15	/	μJ	
Turn-on Energy	E_{on}	/	58.3	/	μJ	$V_{DS} = 400V$ $V_{GS} = -3/15V$ $I_D = 20A$ $R_G = 1\Omega$
Turn-off Energy	E_{off}	/	22.4	/		
Turn-On Delay Time	$t_{d(on)}$	/	12	/	nS	$V_{DS} = 400V$ $V_{GS} = -3/15V$ $I_D = 20A$ $R_G = 1\Omega$
Rise Time	t_r	/	12.5	/		
Turn-Off Delay Time	$t_{d(off)}$	/	21.9	/		
Fall Time	t_f	/	15	/		
Internal Gate Resistance	$R_{G(int)}$	/	1.06	/	Ω	$f = 1MHz$ $V_{AC} = 25mV$
Gate to Source Charge	Q_{gs}	/	17.5	/	nC	$V_{DS} = 400V$ $I_{DS} = 20A$ $V_{GS} = -3 \text{ to } 15V$ $I_G = 50mA$
Gate to Drain Charge	Q_{gd}	/	15.3	/		
Total Gate Charge	Q_g	/	53.1	/		



3. Reverse Diode Characteristics

At $T_J = 25^\circ\text{C}$, unless specified otherwise

Parameter	Symbol	Value		Unit	Test Conditions
		Typ.	Max.		
Diode Forward Voltage	V_{SD}	4.8	/	V	$V_{GS} = -3\text{V}$ $I_{SD} = 10\text{A}$ $T_J = 25^\circ\text{C}$
		4.3	/	V	$V_{GS} = -3\text{V}$ $I_{SD} = 10\text{A}$ $T_J = 175^\circ\text{C}$
Continuous Diode Forward Current	I_S	25	/	A	$V_{GS} = -3\text{V}$
Reverse Recover Time	t_{rr}	15.2	/	nS	$V_{GS} = -3\text{V}$ $I_{SD} = 20\text{A}$ $V_R = 400\text{V}$ $d_{if}/d_t = 4200\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}	430.6	/	nC	
Peak Reverse Recovery Current	I_{rrm}	45.1	/	A	$T_J = 25^\circ\text{C}$

4. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.94	$^\circ\text{C}/\text{W}$

5. Typical Performance

At $T_J = 25^\circ\text{C}$, unless specified otherwise

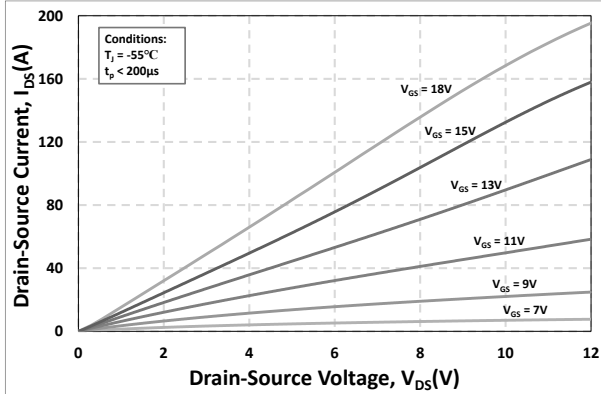


Figure 1. Output Characteristics $T_J = -55^\circ\text{C}$

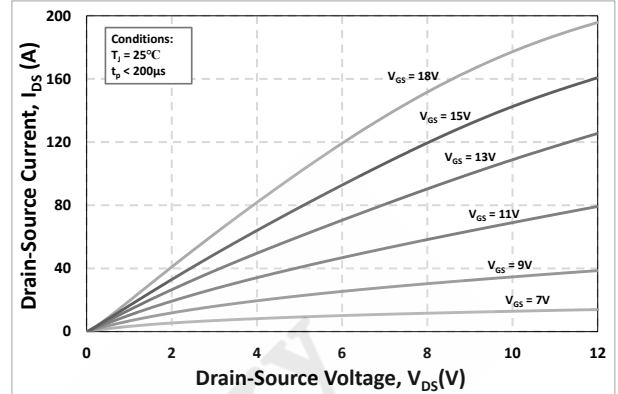


Figure 2. Output Characteristics $T_J = 25^\circ\text{C}$

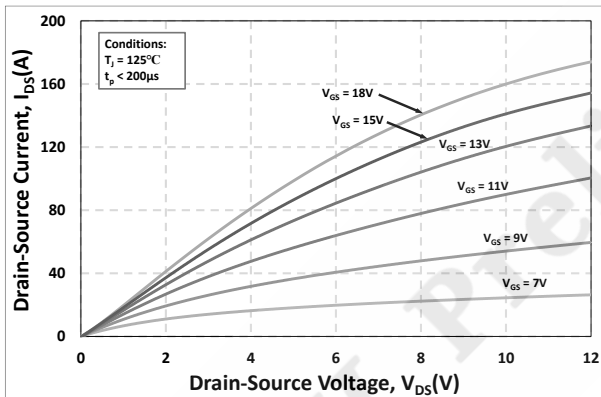


Figure 3. Output Characteristics $T_J = 125^\circ\text{C}$

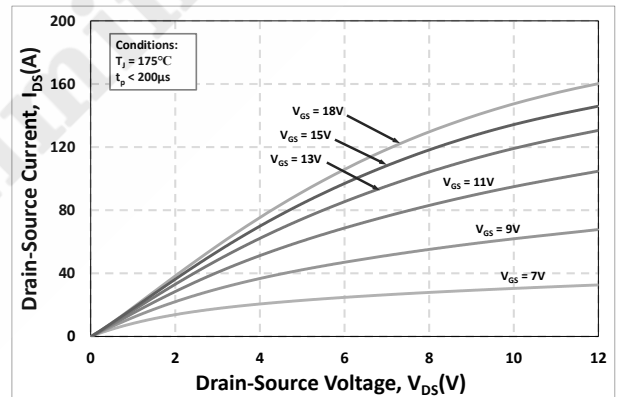


Figure 4. Output Characteristics $T_J = 175^\circ\text{C}$

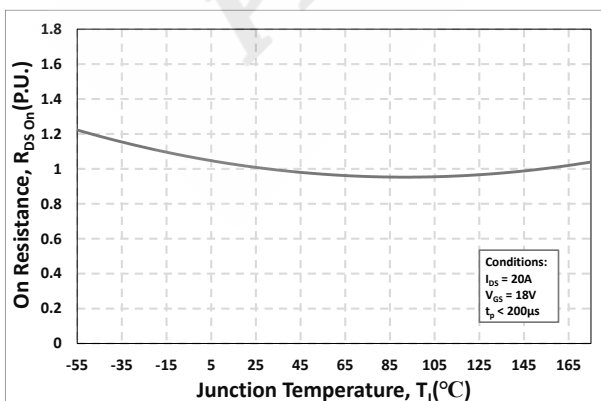


Figure 5. Normalized On-Resistance vs. Temperature

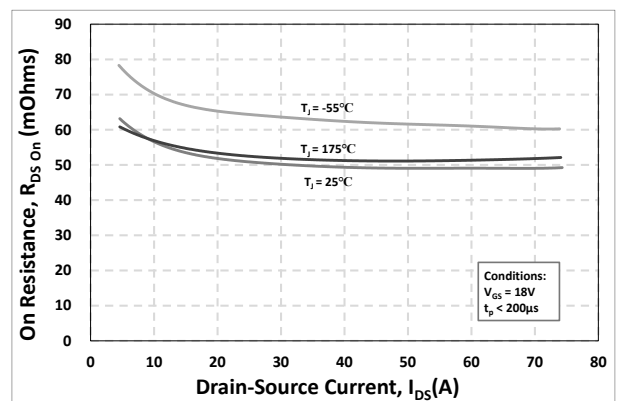


Figure 6. On-Resistance vs. Drain Current Various Temperatures



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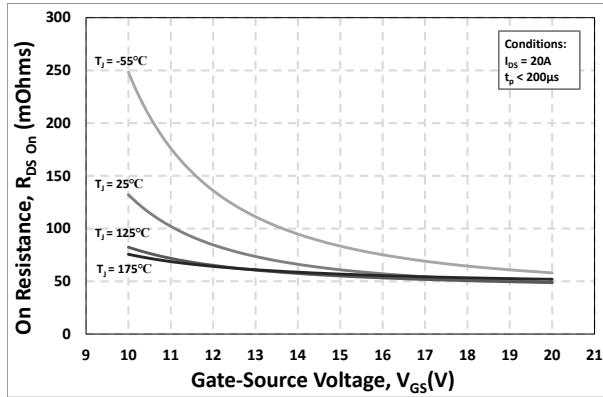


Figure 7. On-Resistance vs. Gate-Source Voltage

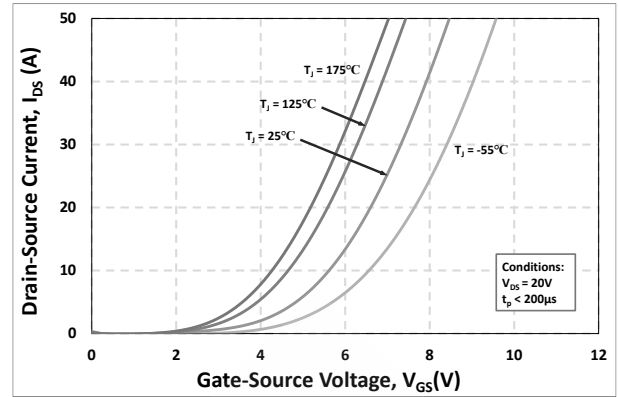


Figure 8. Transfer Characteristic for Various Junction Temperatures

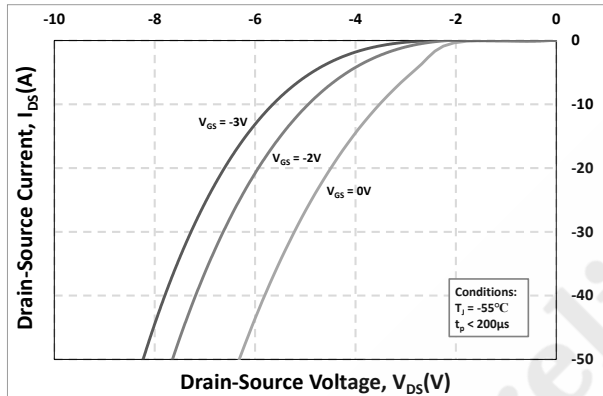


Figure 9. Body Diode Characteristic at -55°C

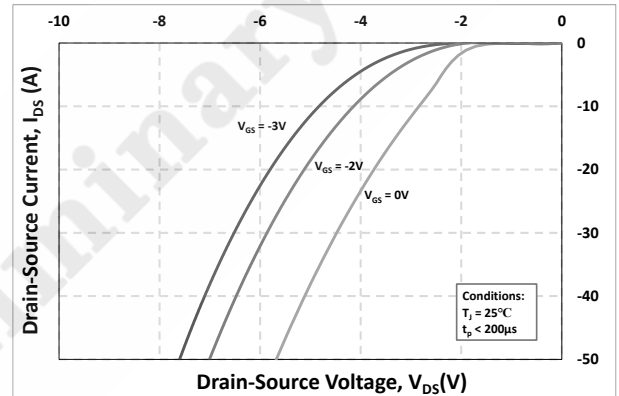


Figure 10. Body Diode Characteristic at 25°C

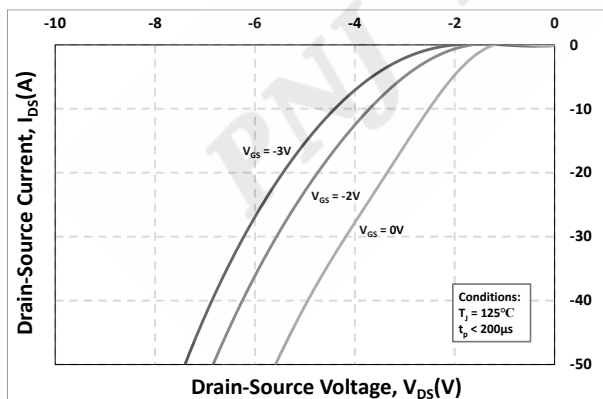


Figure 11. Body Diode Characteristic at 125°C

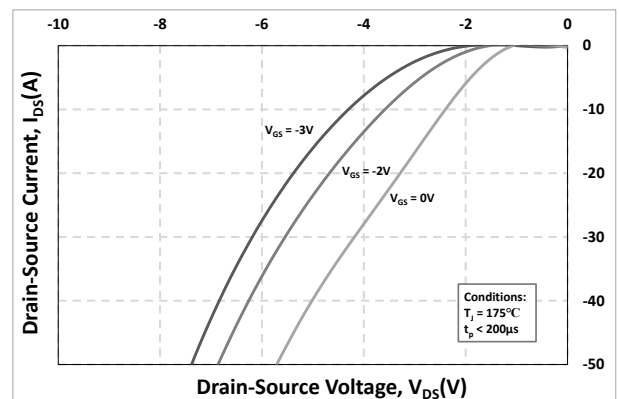


Figure 12. Body Diode Characteristic at 175°C

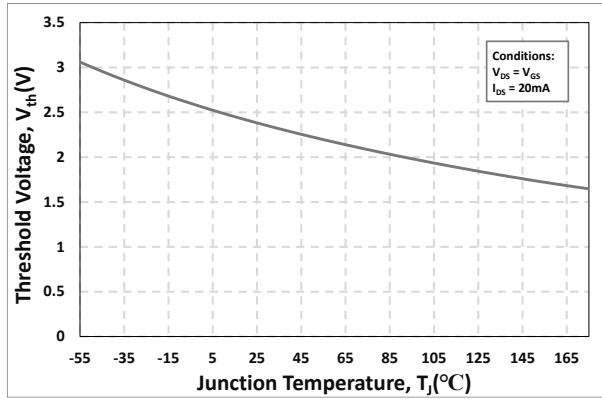


Figure 13. Threshold Voltage vs. Temperature

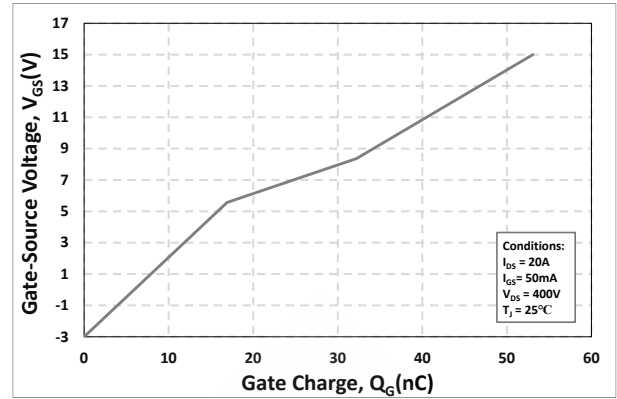


Figure 14. Gate Charge Characteristics

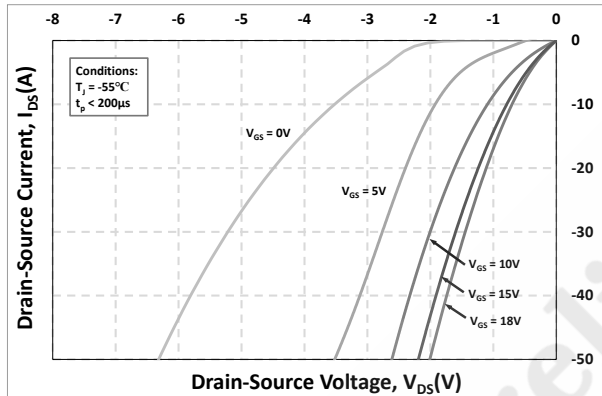


Figure 15. 3rd Quadrant Characteristic at -55°C

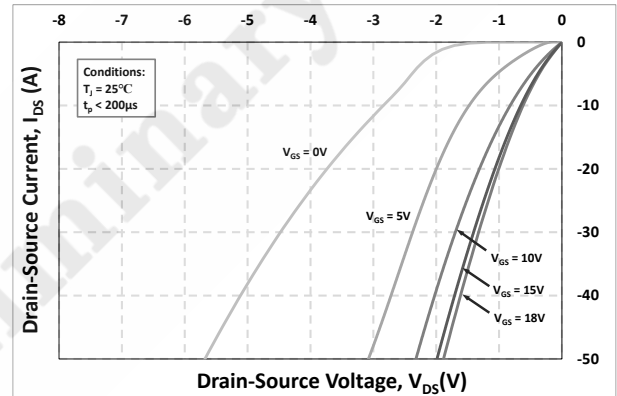


Figure 16. 3rd Quadrant Characteristic at 25°C

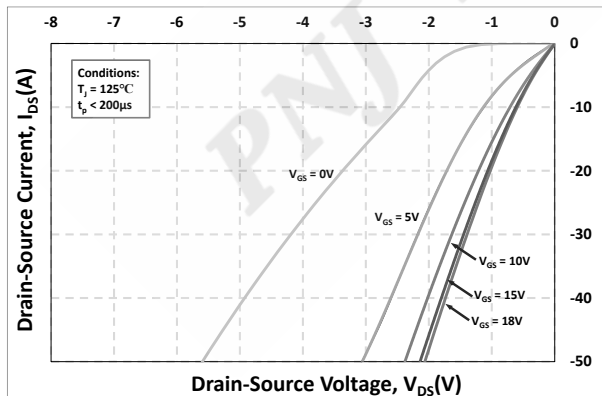


Figure 17. 3rd Quadrant Characteristic at 125°C

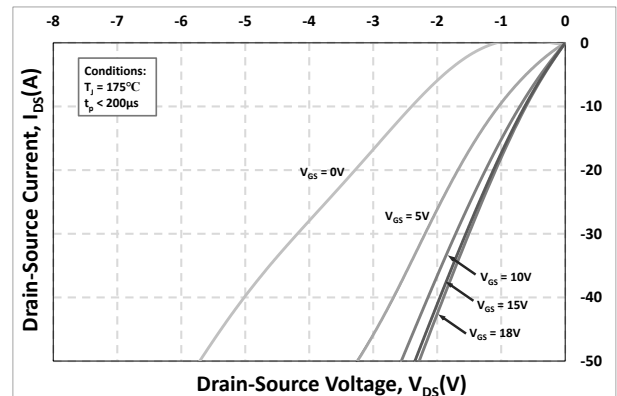


Figure 18. 3rd Quadrant Characteristic at 175°C

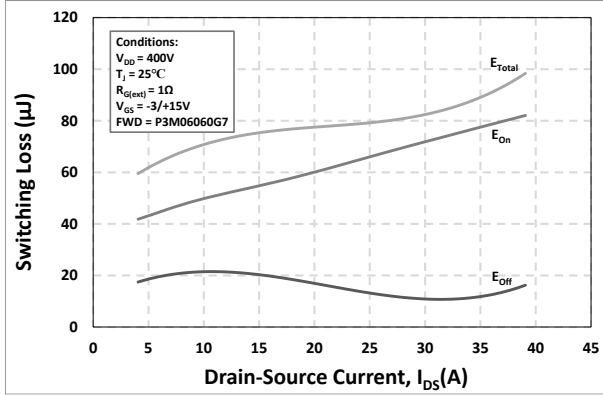


Figure 19. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400V$)

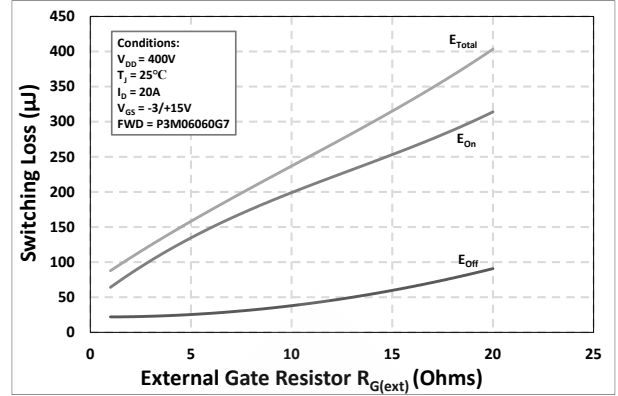


Figure 20. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

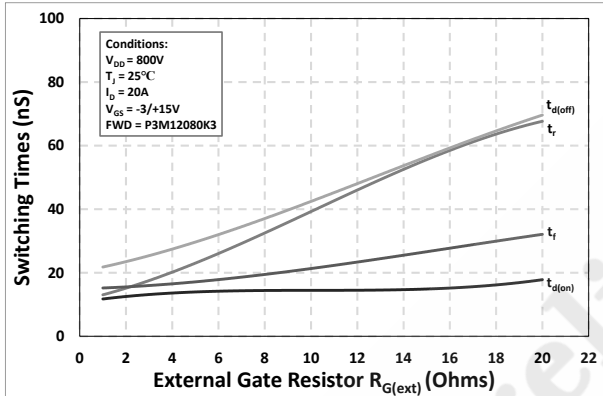


Figure 21. Switching Times vs. $R_{G(ext)}$

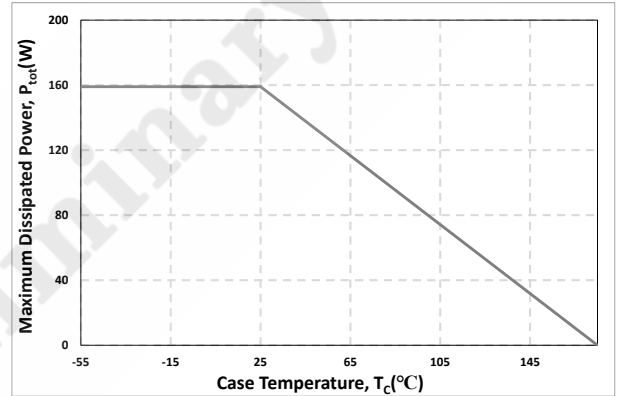


Figure 22. Maximum Power Dissipation Derating vs. Case Temperature

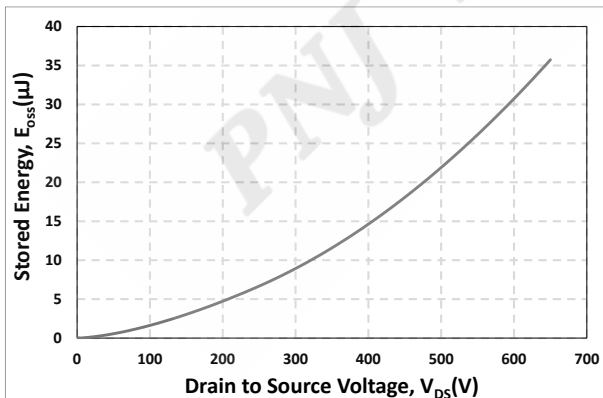


Figure 23. Output Capacitor Stored Energy

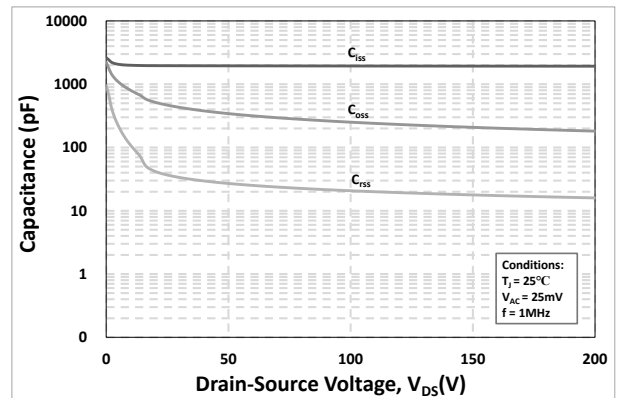


Figure 24. Capacitances vs. Drain-Source Voltage (0 - 200V)

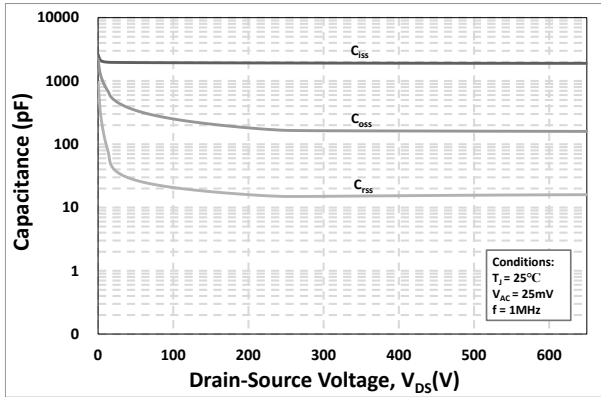


Figure 25. Capacitances vs. Drain-Source Voltage (0 - 650V)

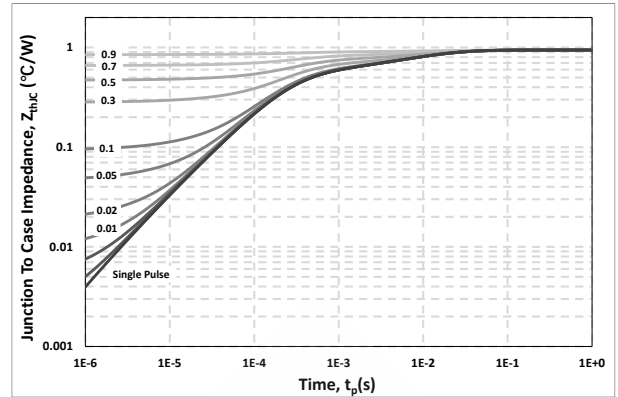


Figure 26. Transient Thermal Impedance (Junction - Case)

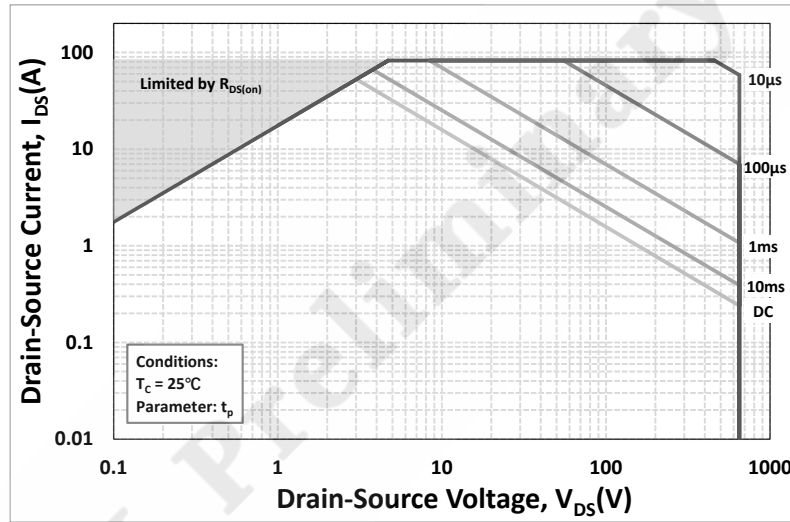


Figure 27. Safe Operating Area

6. Definitions

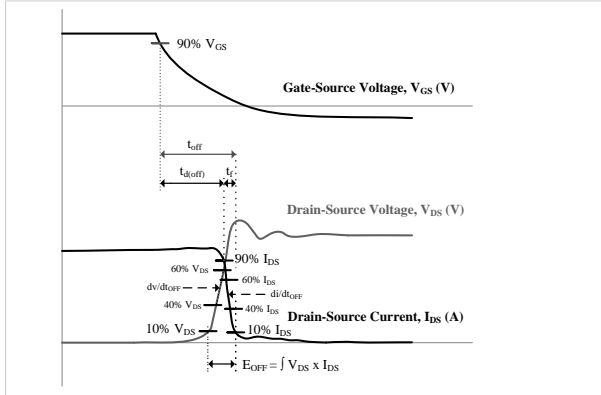


Figure 28. Turn-off Transient Definitions

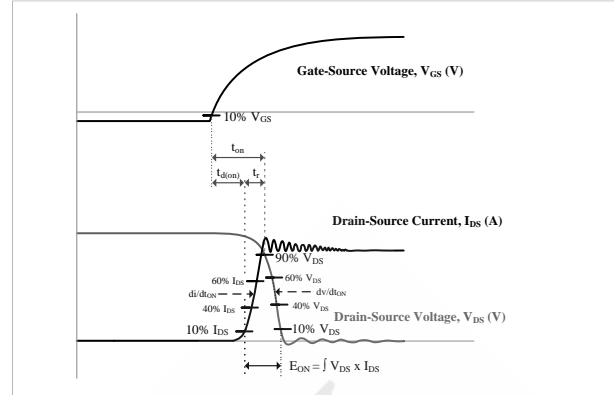


Figure 29. Turn-on Transient Definitions

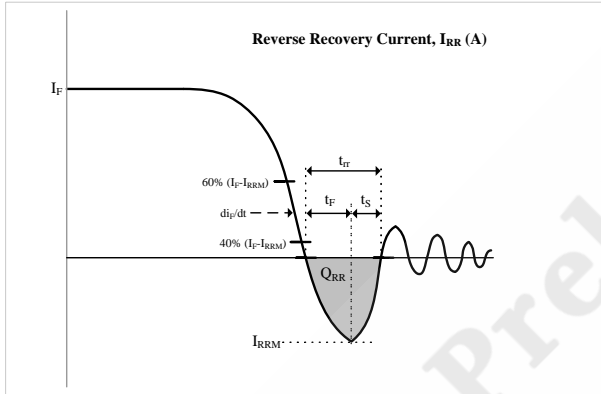


Figure 30. Reverse Recovery Definitions

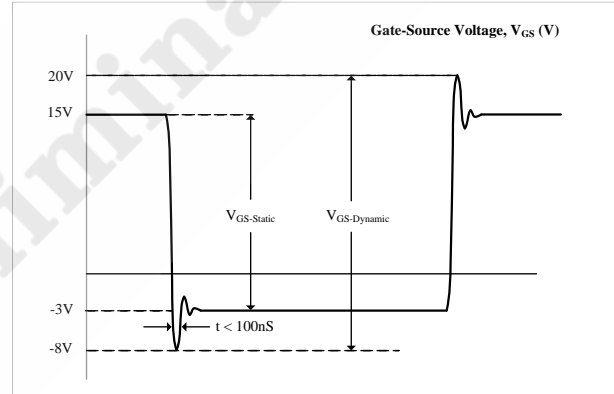
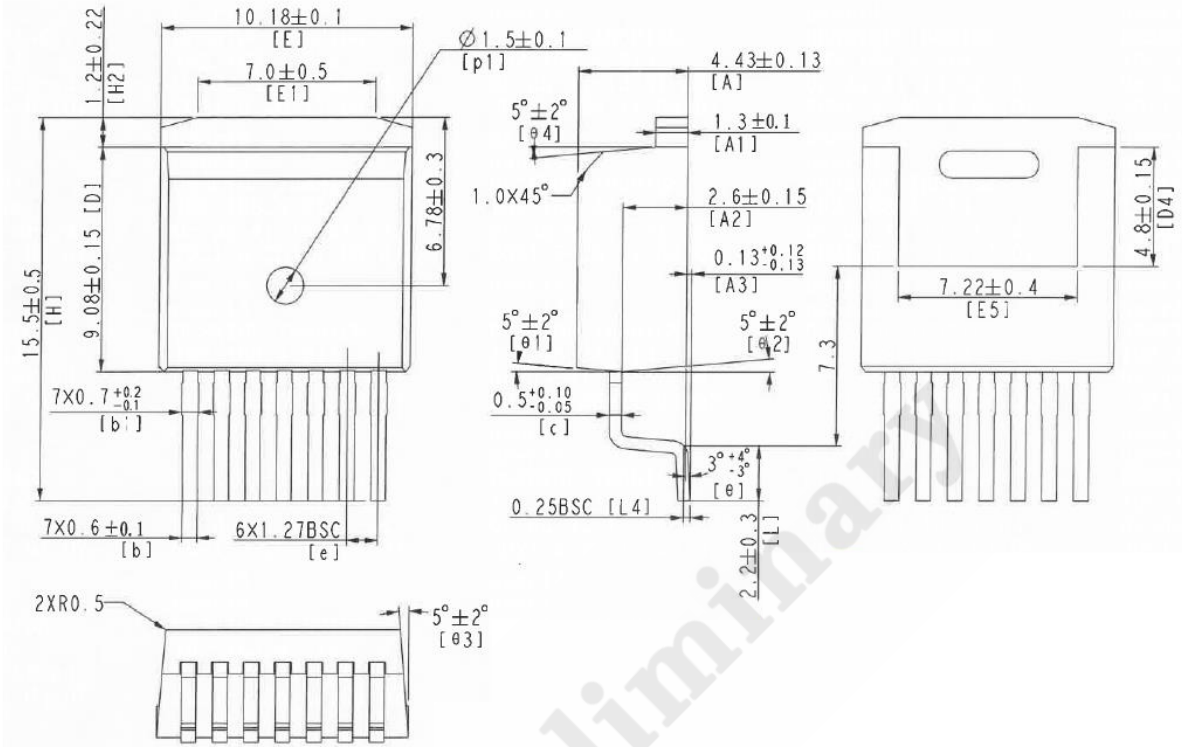


Figure 31. V_{GS} Transient Definitions

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7. Package Outlines



Drawing and Dimensions

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