

MOSFET – Power, Single P-Channel, μ 8FL

-30 V, -88.6 A, 7.5 m Ω

NVTFS015P03P8Z

Features

- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Advanced Package Technology in 3.3 x 3.3 mm for Space Saving and Excellent Thermal Conduction
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Load Switch
- Protection: Reverse Current, Over Voltage, and Reverse Negative Voltage
- Battery Management

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	± 25	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2)	Steady State $T_C = 25^\circ\text{C}$ -88.6 $T_C = 100^\circ\text{C}$ -62.6	A
P_D	Power Dissipation $R_{\theta JC}$ (Notes 1, 2)	$T_C = 25^\circ\text{C}$ 88.2 $T_C = 100^\circ\text{C}$ 44.1	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State $T_A = 25^\circ\text{C}$ -17 $T_A = 100^\circ\text{C}$ -12	A
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	$T_A = 25^\circ\text{C}$ 3.2 $T_A = 100^\circ\text{C}$ 1.6	W
I_{DM}	Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$ -353	A
T_J , T_{stg}	Operating Junction and Storage Temperature Range	-55 to 175	$^\circ\text{C}$
I_S	Source Current (Body Diode)	73.5	A
E_{AS}	Single Pulse Drain to Source Avalanche Energy ($I_L = 8.5 \text{ A}$)	88	mJ
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

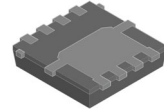
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Drain) (Note 2)	1.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	46.4	$^\circ\text{C/W}$

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 1 in², 2 oz. Cu pad. Assuming a 76 mm x 76 mm x 1.6 mm board.

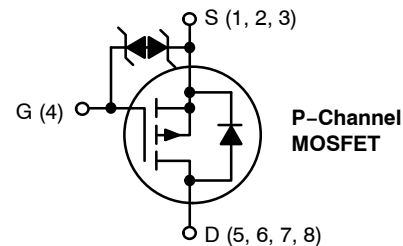
$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
-30 V	7.5 m Ω @ -10 V 12 m Ω @ -4.5 V	-88.6 A



WDFN8
(μ 8FL)
CASE 511AB



WDFNW8
(μ 8FL WF)
CASE 515AN



MARKING DIAGRAMS



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

NVTF5015P03P8Z

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-30			V
V _{(BR)DSS} /T _J	Drain-to-Source Breakdown Voltage Temperature Coefficient	I _D = -250 μA, ref to 25°C		-4.4		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = -30 V, T _J = 25°C			-10	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = ±25 V			±10	μA

ON CHARACTERISTICS (Note 3)

V _{GS(TH)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-1.0		-3.0	V
V _{GS(TH)} /T _J	Threshold Temperature Coefficient	I _D = -250 μA, ref to 25°C		5.6		mV/°C
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = -10 V, I _D = -12 A		5.0	7.5	mΩ
		V _{GS} = -4.5 V, I _D = -10 A		8.0	12	
g _{FS}	Forward Transconductance	V _{DS} = -5 V, I _D = -10 A		77		S

CHARGES AND CAPACITANCES

C _{iss}	Input Capacitance	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -15 V		2706		pF
C _{oss}	Output Capacitance			907		
C _{rss}	Reverse Transfer Capacitance			875		
Q _{G(TOT)}	Total Gate Charge	V _{GS} = -4.5 V, V _{DS} = -15 V, I _D = -10 A		37		nC
Q _{G(TH)}	Threshold Gate Charge			5.1		
Q _{GS}	Gate-to-Source Charge			8.2		
Q _{GD}	Gate-to-Drain Charge			21.7		
Q _{G(TOT)}	Total Gate Charge	V _{GS} = -10 V, V _{DS} = -15 V, I _D = -10 A		62.3	105	

SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 3)

t _{d(on)}	Turn-On Delay Time	V _{GS} = -4.5 V, V _{DS} = -15 V, I _D = -10 A, R _G = 6 Ω		25		ns
t _r	Rise Time			138		
t _{d(off)}	Turn-Off Delay Time			55		
t _f	Fall Time			98		

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)

t _{d(on)}	Turn-On Delay Time	V _{GS} = -10 V, V _{DS} = -15 V, I _D = -10 A, R _G = 6 Ω		6		ns
t _r	Rise Time			17		
t _{d(off)}	Turn-Off Delay Time			52		
t _f	Fall Time			63		

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = -10 A	T _J = 25°C		-0.8	-1.3	V
			T _J = 125°C		-0.65		
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = -10 A		40.7			ns
t _a	Charge Time			18.4			
t _b	Discharge Time			22.3			
Q _{RR}	Reverse Recovery Charge			29			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

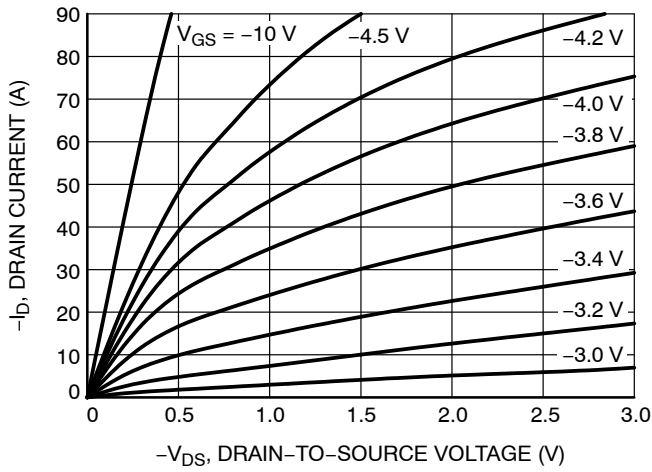


Figure 1. On-Region Characteristics

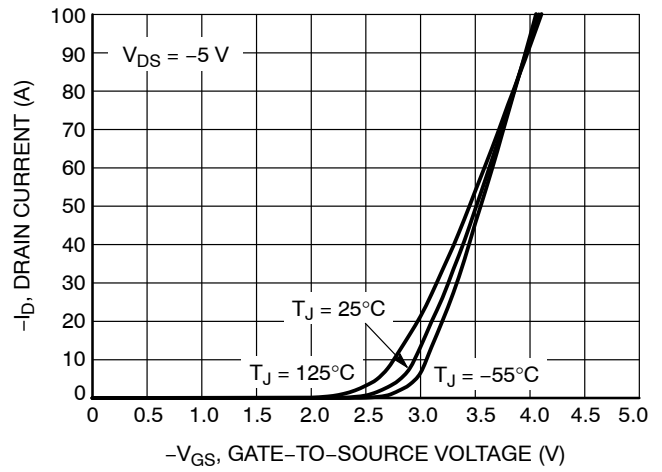


Figure 2. Transfer Characteristics

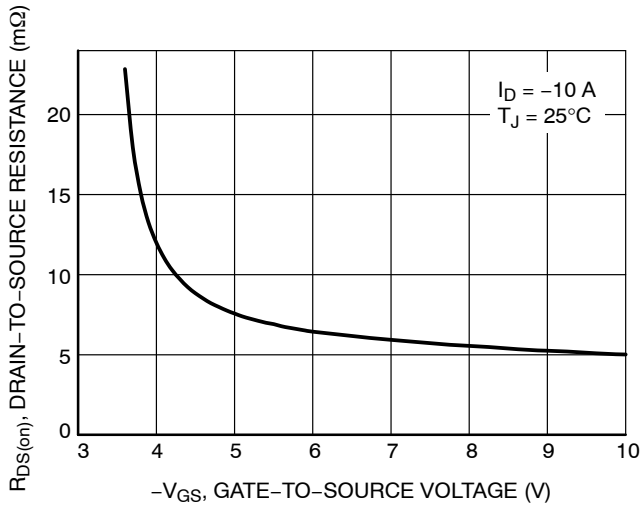


Figure 3. On-Resistance vs. Gate-to-Source Voltage

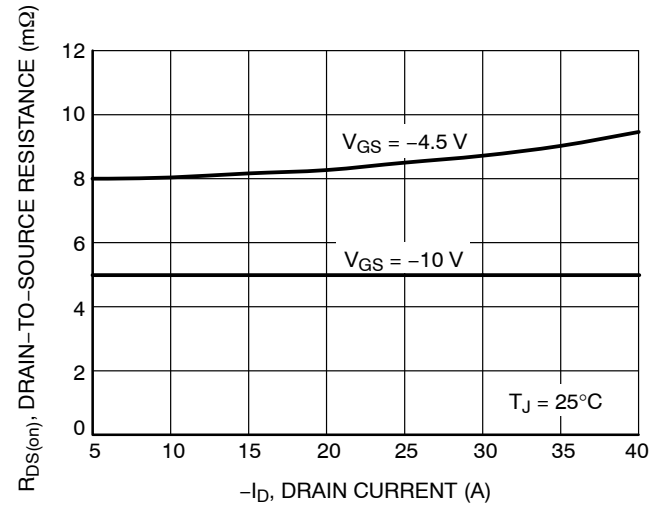


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

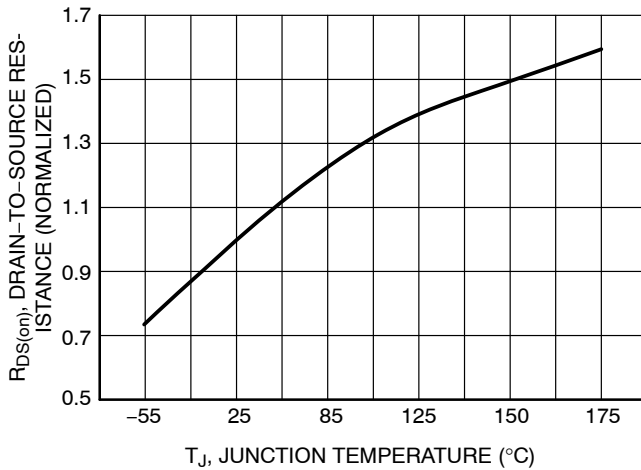


Figure 5. On-Resistance Variation with Temperature

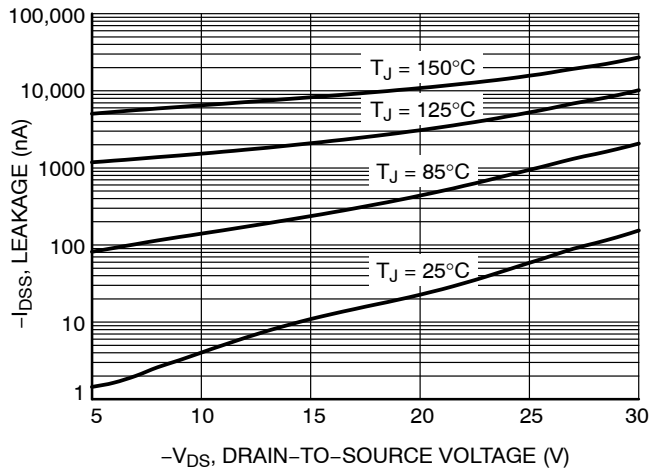


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

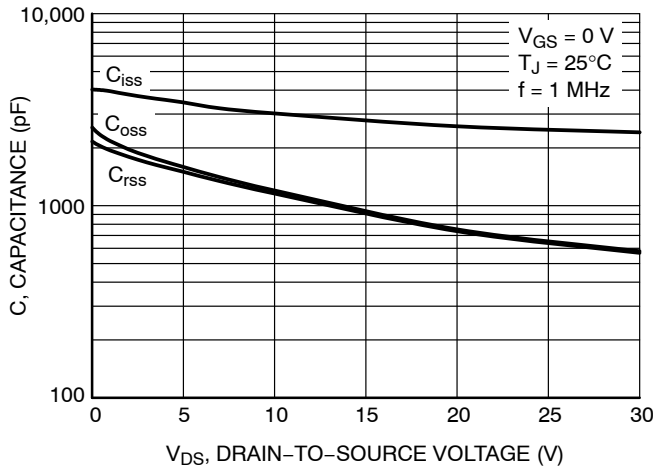


Figure 7. Capacitance Variation

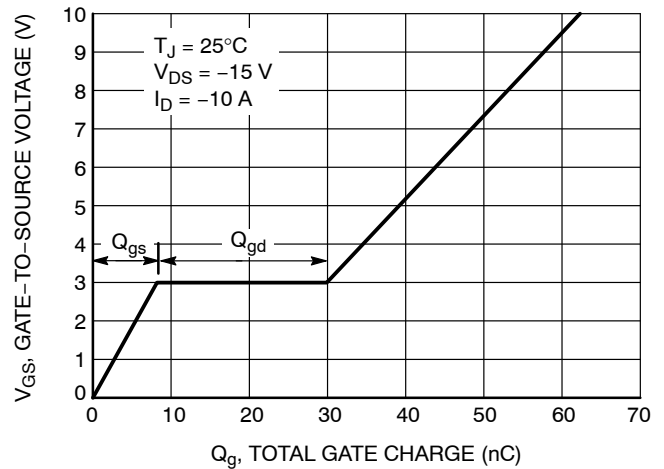


Figure 8. Gate-to-Source vs. Total Charge

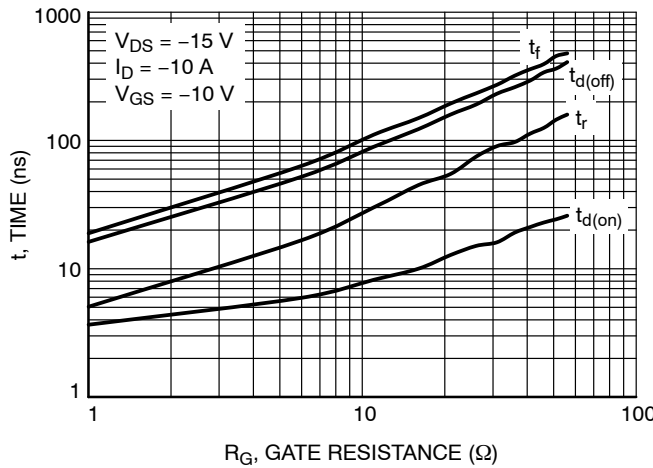


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

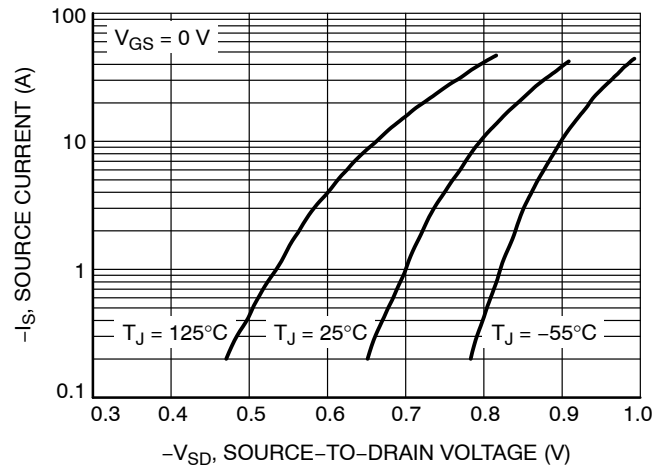


Figure 10. Diode Forward Voltage vs. Current

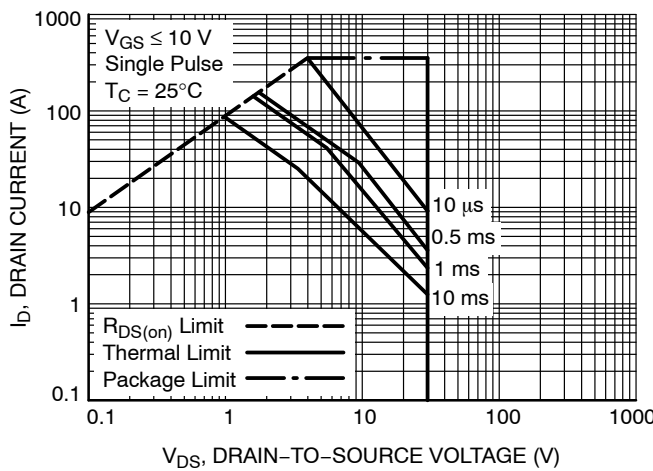


Figure 11. Maximum Rated Forward Biased Safe Operating Area

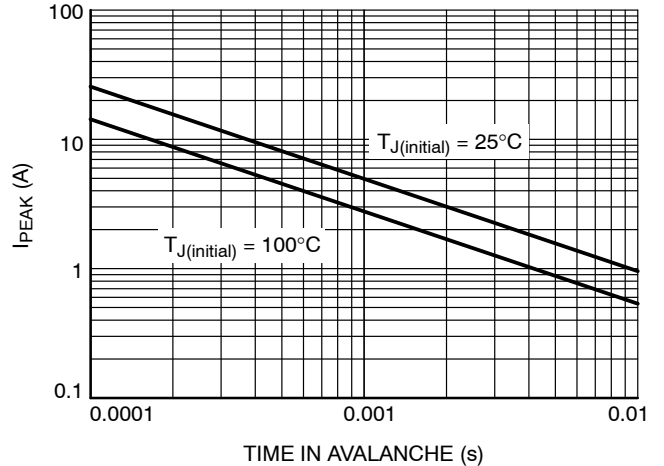


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVTFS015P03P8Z

TYPICAL CHARACTERISTICS (continued)

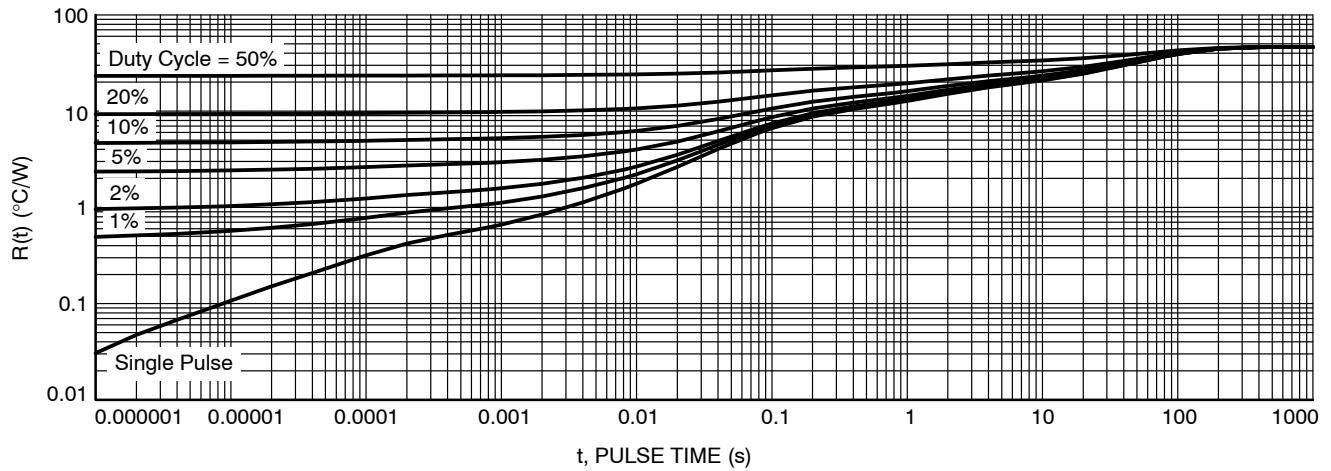


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVTFS015P03P8ZTAG	15PW	WDFN8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

DISCONTINUED (Note 4)

NVTFS015P03P8ZTAG	15P3	WDFN8 (Pb-Free)	1500 / Tape & Reel
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[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

4. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



SCALE 2:1

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

DATE 23 APR 2012


GENERIC
MARKING DIAGRAM*


XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

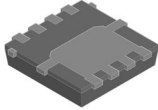
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °

SOLDERING FOOTPRINT*


*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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WDFNW8 3.3x3.3, 0.65P (Full-Cut μ8FL WF)
CASE 515AN
ISSUE O

DATE 25 AUG 2020



TOP VIEW



SIDE VIEW



DETAIL A



DETAIL B

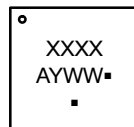


BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60


RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

**GENERIC
MARKING DIAGRAM***


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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