

MOSFET – Power, Single N-Channel

80 V, 48 A, 14.5 mΩ

NTTFS6H854N

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Value	Unit	
V_{DSS}	Drain-to-Source Voltage		80	V	
V_{GS}	Gate-to-Source Voltage		± 20	V	
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4)	Steady State	$T_C = 25^\circ\text{C}$	44	A
			$T_C = 100^\circ\text{C}$	31	
P_D	Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	68	W
			$T_C = 100^\circ\text{C}$	34	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4)	Steady State	$T_A = 25^\circ\text{C}$	9.5	A
			$T_A = 100^\circ\text{C}$	6.7	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	3.2	W
			$T_A = 100^\circ\text{C}$	1.6	
I_{DM}	Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	175	A	
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55 to +175	$^\circ\text{C}$	
I_S	Source Current (Body Diode)		57	A	
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 2.2 \text{ A}$)		205	mJ	
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 3)	2.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 3)	47	

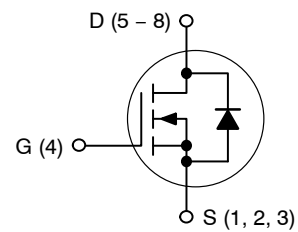
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
80 V	14.5 mΩ @ 10 V	48 A

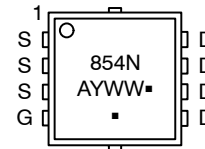


WDFN8
(μ8FL)
CASE 511AB

N-Channel



MARKING DIAGRAM



854N = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTTFS6H854N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	80			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 80 V	T _J = 25°C		10	μA
			T _J = 125°C		250	
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 5)

V _{GS(TH)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 45 μA	2.0		4.0	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 10 A		11.9	14.5	mΩ
		V _{GS} = 6 V, I _D = 10 A		17.1	23.1	
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 15 A		39.5		S

CHARGES AND CAPACITANCES

C _{iss}	Input Capacitance	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 40 V		770		pF
C _{oss}	Output Capacitance			113		
C _{rss}	Reverse Transfer Capacitance			5.4		
Q _{G(TH)}	Threshold Gate Charge	V _{GS} = 10 V, V _{DS} = 40 V, I _D = 15 A		2.7		nC
Q _{GS}	Gate-to-Source Charge			4.3		
Q _{GD}	Gate-to-Drain Charge			2.3		
Q _{G(TOT)}	Total Gate Charge	V _{GS} = 10 V, V _{DS} = 40 V, I _D = 15 A		13		nC

SWITCHING CHARACTERISTICS (Note 6)

t _{d(on)}	Turn-On Delay Time	V _{GS} = 6.0 V, V _{DS} = 64 V, I _D = 15 A		11		ns
t _r	Rise Time			22		
t _{d(off)}	Turn-Off Delay Time			24		
t _f	Fall Time			6.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 10 A	T _J = 25°C		0.8	1.2	V
			T _J = 125°C		0.7		
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 15 A		33		ns	
t _a	Charge Time			22			
t _b	Discharge Time			11			
Q _{RR}	Reverse Recovery Charge			29			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

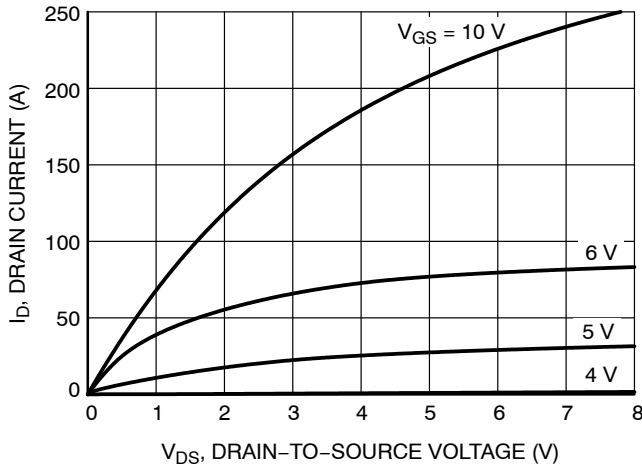


Figure 1. On-Region Characteristics

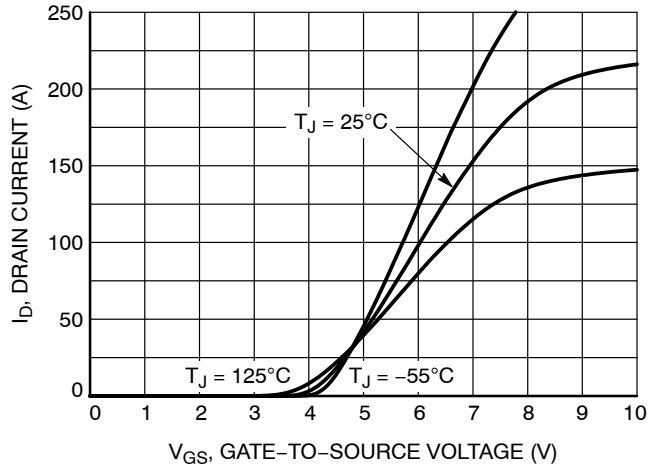


Figure 2. Transfer Characteristics

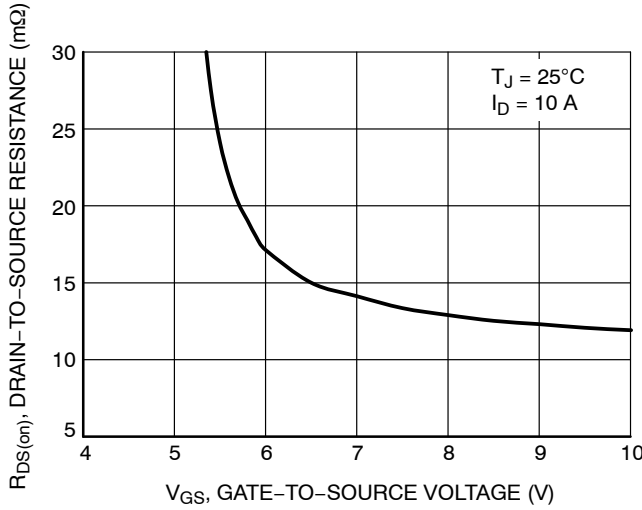


Figure 3. On-Resistance vs. Gate-to-Source Voltage

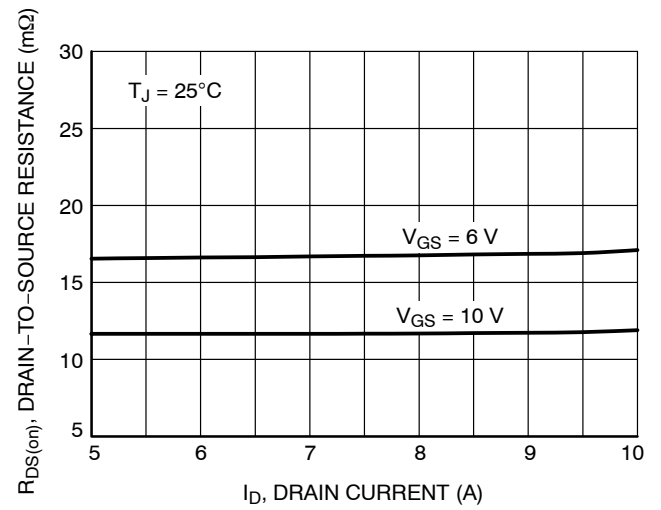


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

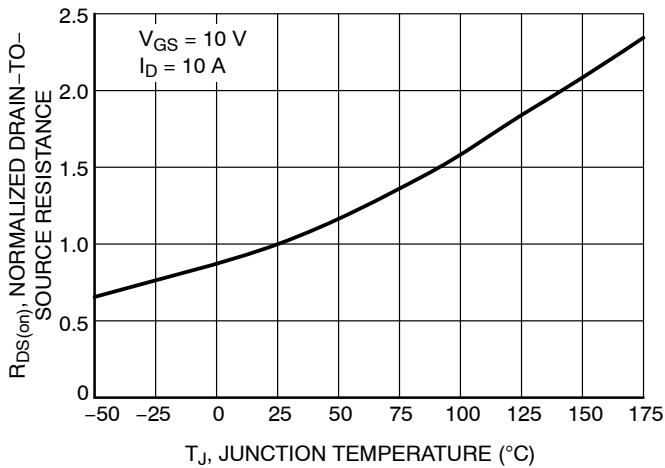


Figure 5. On-Resistance Variation with Temperature

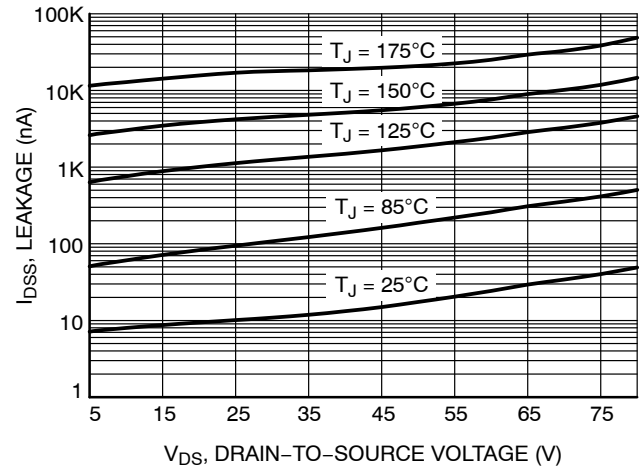


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (continued)

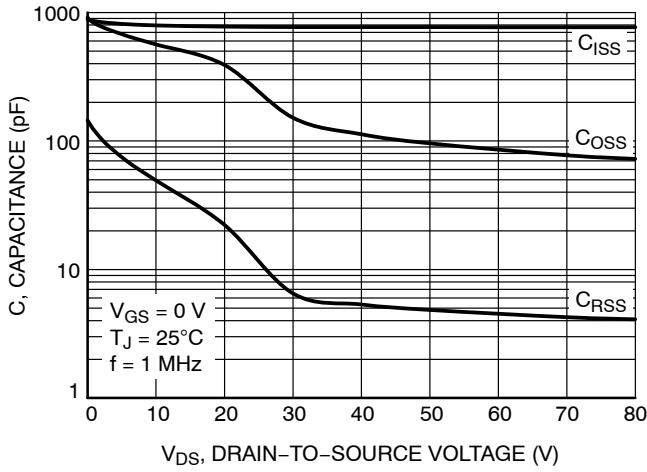


Figure 7. Capacitance Variation

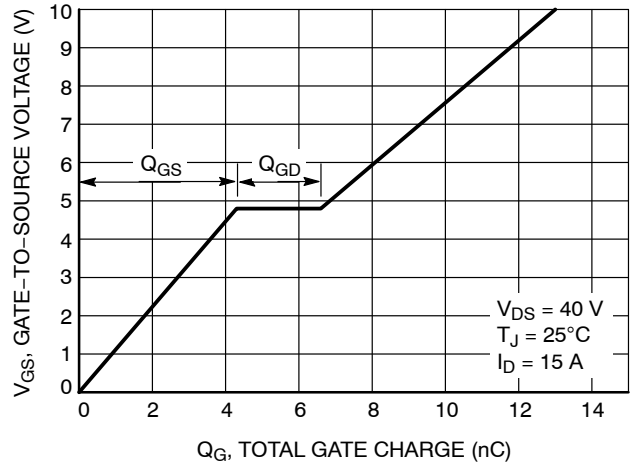


Figure 8. Gate-to-Source Voltage vs. Total Charge

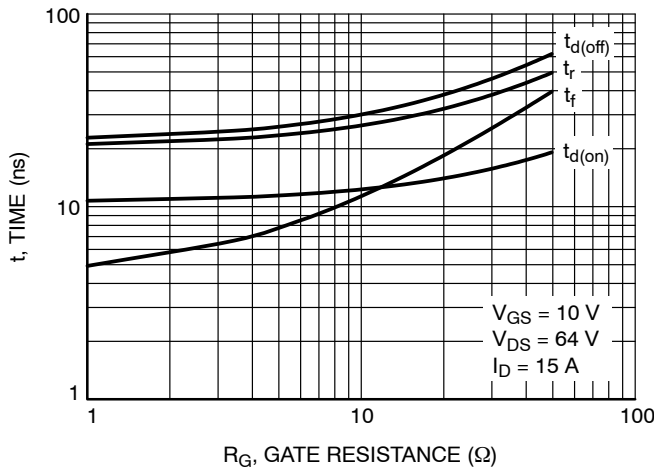


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

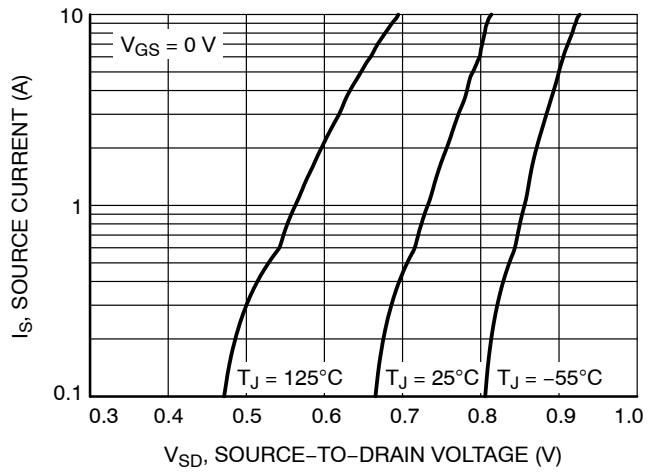


Figure 10. Diode Forward Voltage vs. Current

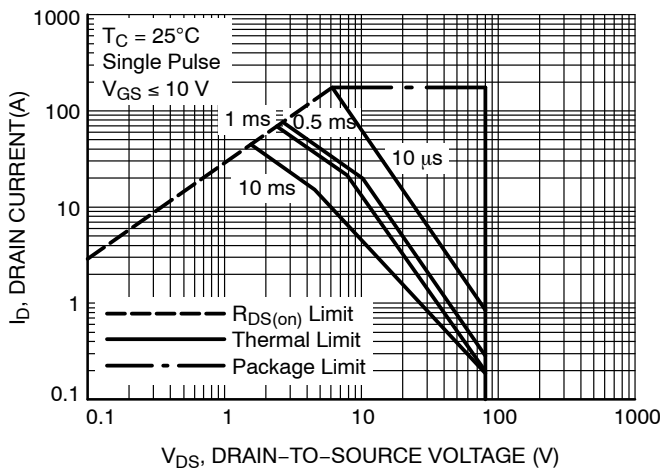


Figure 11. Maximum Rated Forward Biased Safe Operating Area

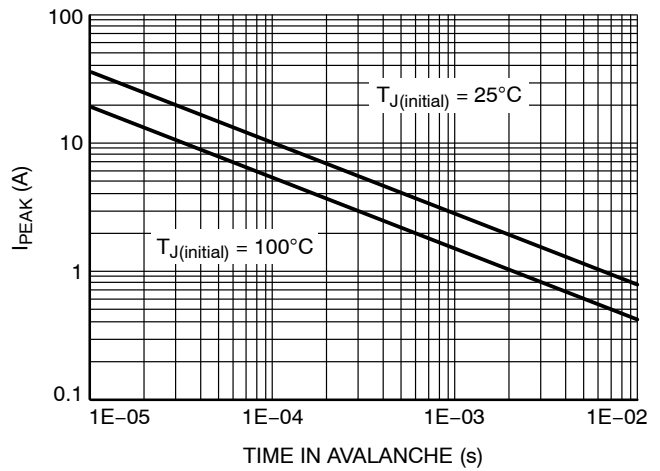


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS (continued)

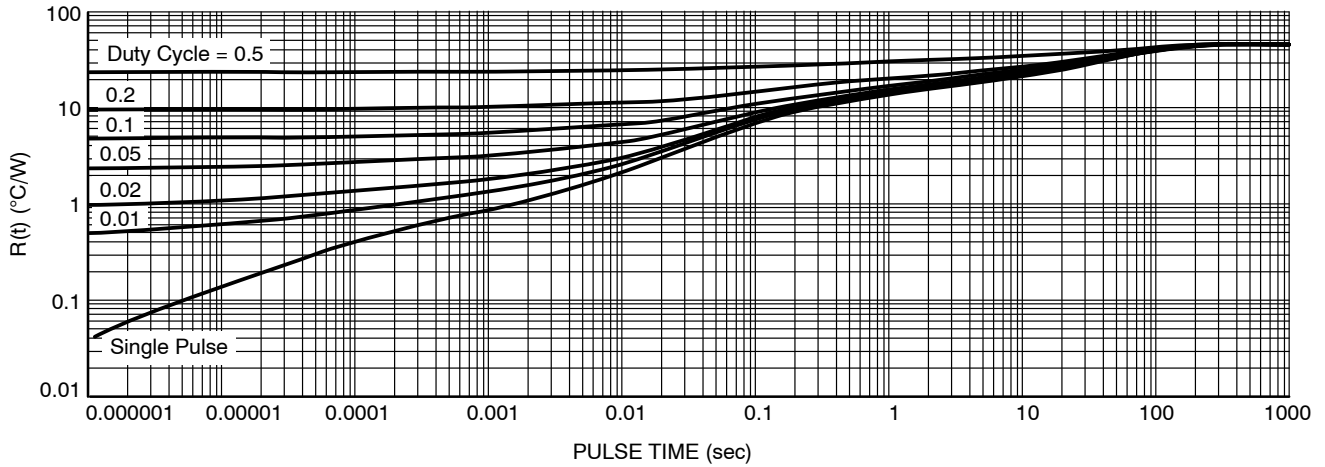


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTTFS6H854NTAG	854N	WDFN8 (Pb-Free)	1,500 / Tape & Reel

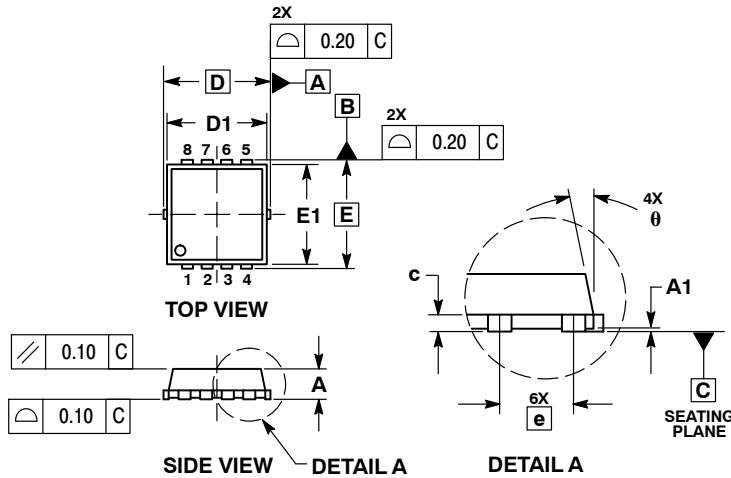
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



SCALE 2:1

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

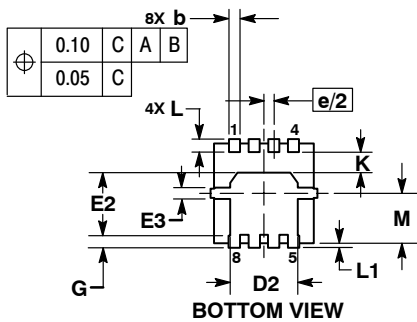
DATE 23 APR 2012



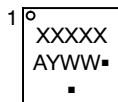
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °



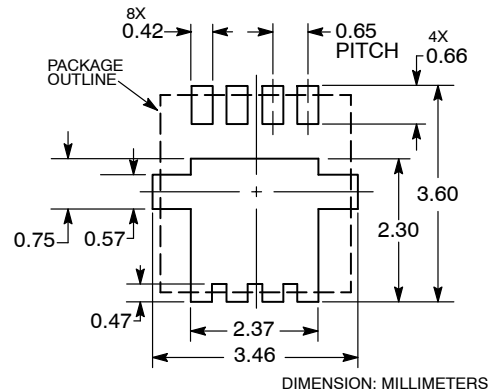
GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	WDFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

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