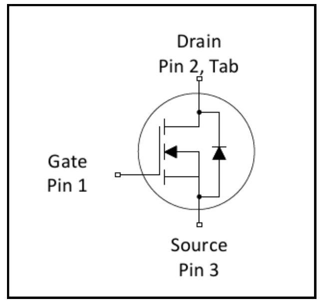
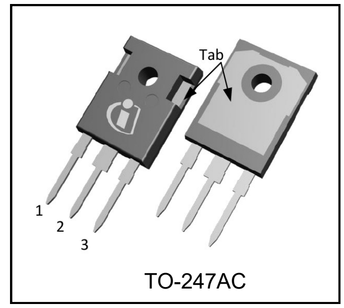
Strong*IR*FET™
IRFP7430PbF

V_{DSS}	40V
$R_{DS(on)}$ typ.	1.0mΩ
max.	1.3mΩ
$I_{D\ (Silicon\ Limited)}$	404A①
$I_{D\ (Package\ Limited)}$	195A





G	D	S
Gate	Drain	Source

Application
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- RoHS Compliant, Halogen-Free *

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP7430PbF	TO-247AC	Tube	25	IRFP7430PbF

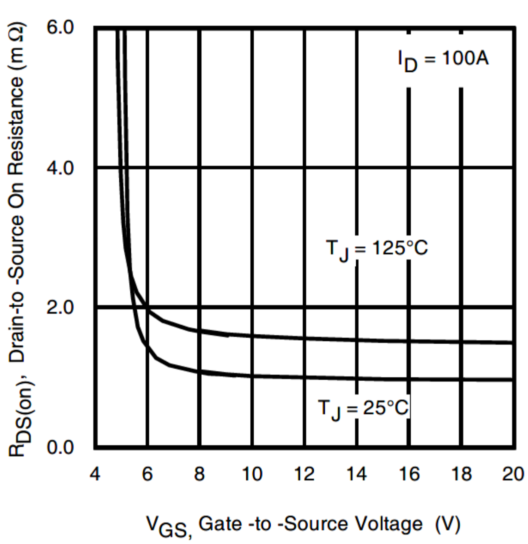


Fig 1. Typical On-Resistance vs. Gate Voltage

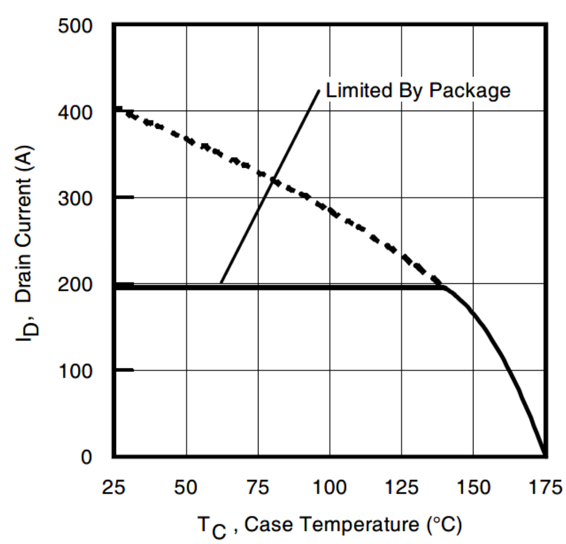


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	404①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	286①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	195	
I_{DM}	Pulsed Drain Current ②	1524	
P_D @T_C = 25°C	Maximum Power Dissipation	366	W
	Linear Derating Factor	2.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	722	mJ
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ⑩	1405	
I_{AR}	Avalanche Current ②	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨	——	0.41	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient ⑧	——	40	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.014	——	V/°C	Reference to 25°C, I_D = 1mA ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	1.0	1.3	mΩ	V_{GS} = 10V, I_D = 100A
		——	1.2	——		V_{GS} = 6.0V, I_D = 50A
$V_{GS(th)}$	Gate Threshold Voltage	2.2	——	3.9	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} =40 V, V_{GS} = 0V
		——	——	150		V_{DS} =40V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
R_G	Gate Resistance	——	2.1	——	Ω	

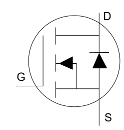
Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A.Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
② Repetitive rating; pulse width limited by max. Junction temperature.
③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.14mH, R_G = 50Ω, I_{AS} = 100A,V_{GS} =10V.
④ I_{SD} ≤ 100A, di/dt ≤ 990A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.
⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
⑥ Coss eff. (TR) is a fixed capacitance that gives the same charging time as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.
⑦ Coss eff. (ER) is a fixed capacitance that gives the same energy as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.
⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
⑨ R_θ is measured at T_J approximately 90°C.
⑩ Limited by T_{Jmax}, starting T_J = 25°C, L = 1.0mH, R_G = 50Ω, I_{AS} = 53A,V_{GS} =10V.
* Halogen -Free since April 30, 2014

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	150	——	——	S	V_{DS} = 10V, I_D = 100A
Q_g	Total Gate Charge	——	300	460	nC	I_D = 100A
Q_{gs}	Gate-to-Source Charge	——	77	——		V_{DS} =20V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	98	——		V_{GS} = 10V ⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	——	202	——		
$t_{d(on)}$	Turn-On Delay Time	——	32	——	ns	V_{DD} = 20V
t_r	Rise Time	——	105	——		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	——	160	——		R_G = 2.7Ω
t_f	Fall Time	——	100	——		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	——	14240	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	2130	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	1460	——		*ƒ* = 1.0 MHz, See Fig. 5
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	——	2605	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑦ See Fig. 11
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	——	2920	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	376①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	1576		
V_{SD}	Diode Forward Voltage	——	0.86	1.2	V	T_J = 25°C, I_S = 100A, V_{GS} = 0V ⑤
dv/dt	Peak Diode Recovery ④	——	2.7	——	V/ns	T_J = 175°C, I_S = 100A, V_{DS} = 40V
t_{rr}	Reverse Recovery Time	——	52	——	ns	T_J = 25°C; V_R = 34V, I_F = 100A, di/dt = 100A/μs ⑤
		——	52	——		T_J = 125°C
Q_{rr}	Reverse Recovery Charge	——	97	——	nC	T_J = 25°C
		——	97	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	2.3	——	A	T_J = 25°C

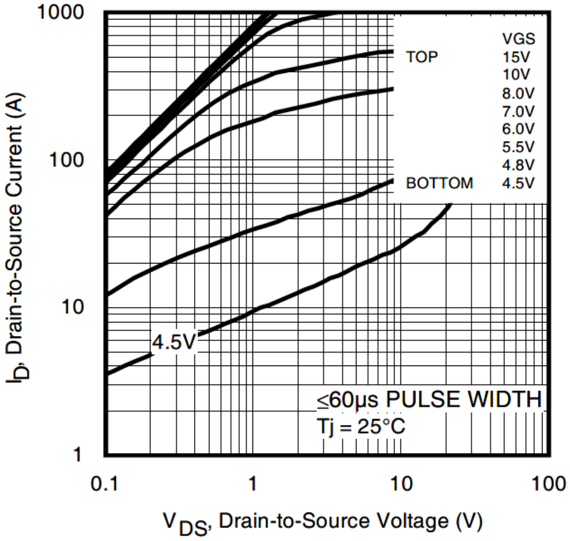


Fig 3. Typical Output Characteristics

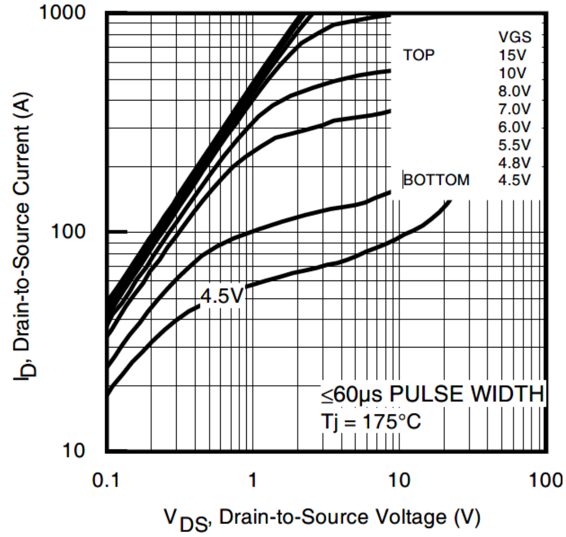


Fig 4. Typical Output Characteristics

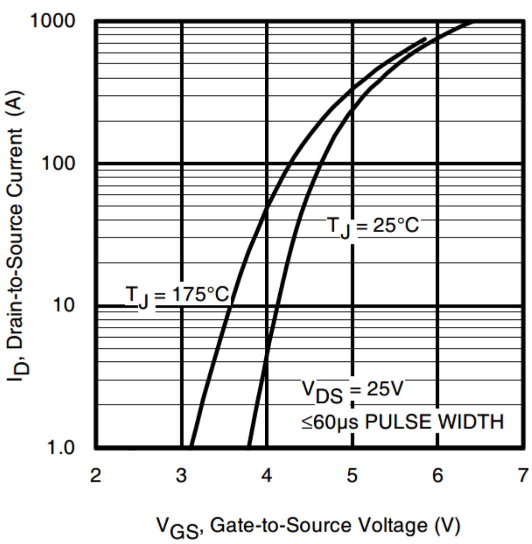


Fig 5. Typical Transfer Characteristics

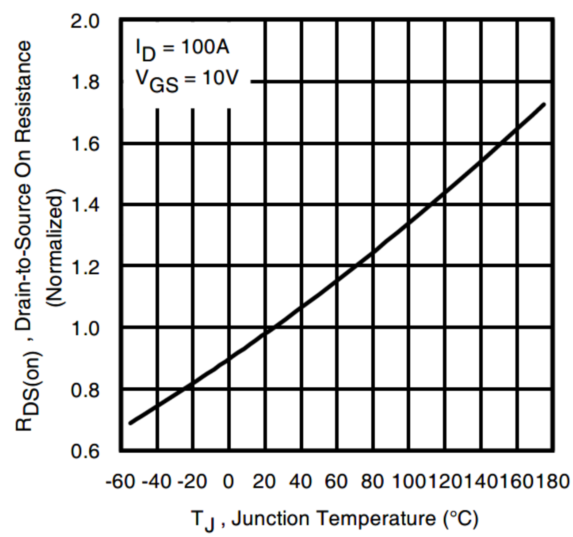


Fig 6. Normalized On-Resistance vs. Temperature

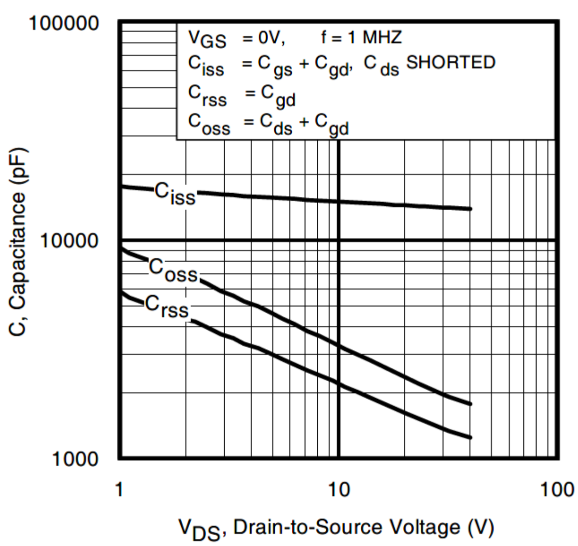


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

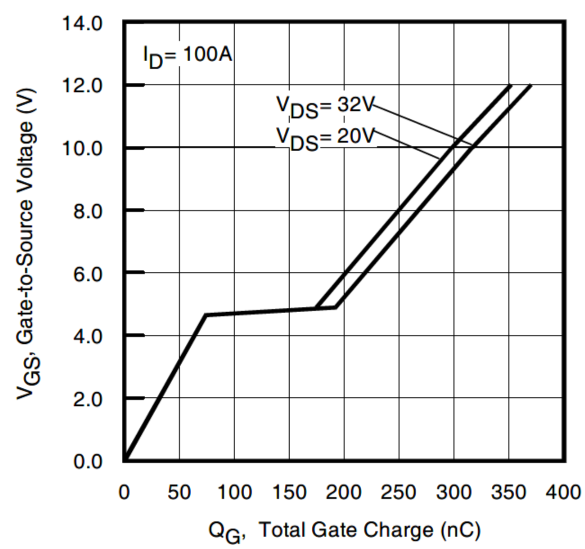


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

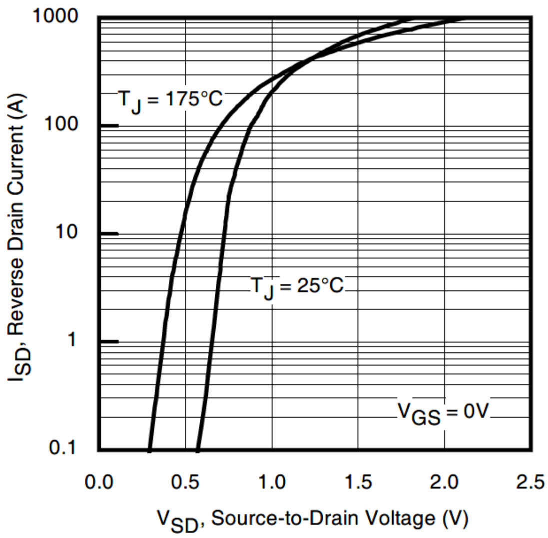


Fig 9. Typical Source-to-Drain Diode Forward Voltage

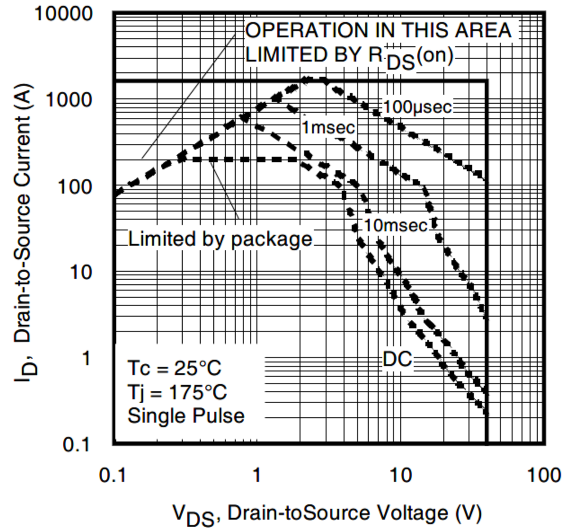


Fig 10. Maximum Safe Operating Area

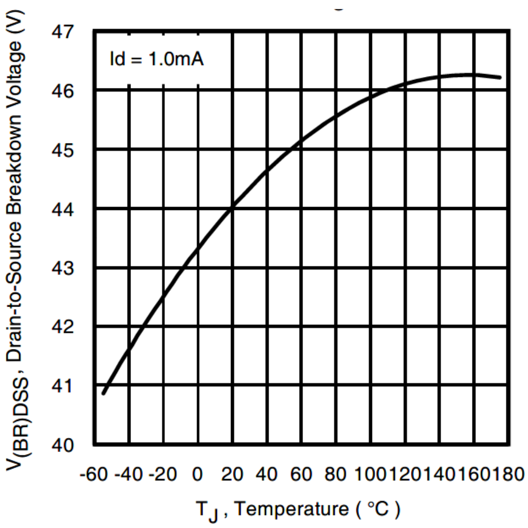


Fig 11. Drain-to-Source Breakdown Voltage

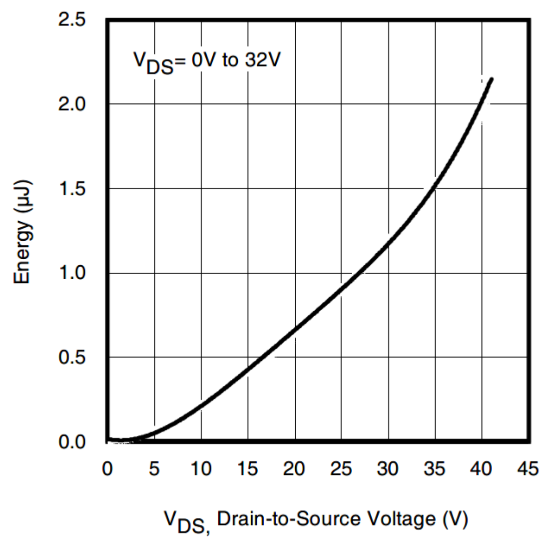


Fig 12. Typical C_{OSS} Stored Energy

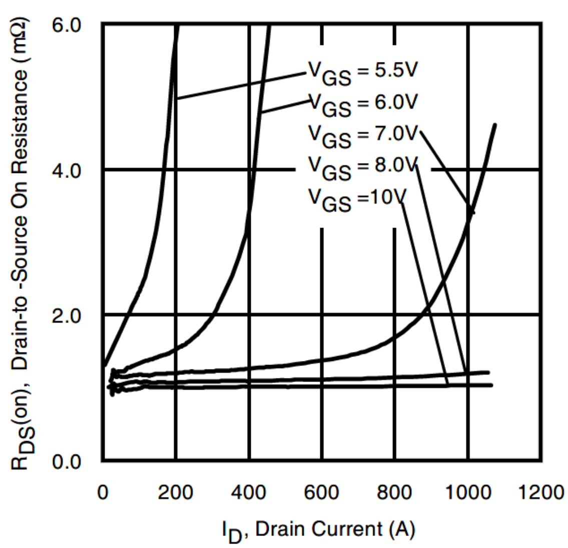


Fig 13. Typical On-Resistance vs. Drain Current

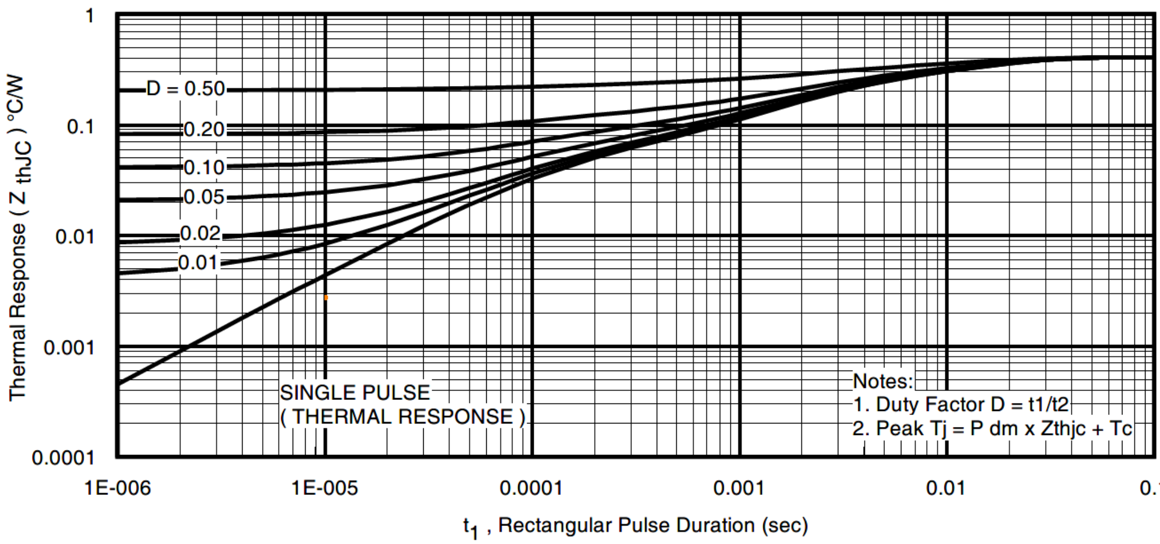


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

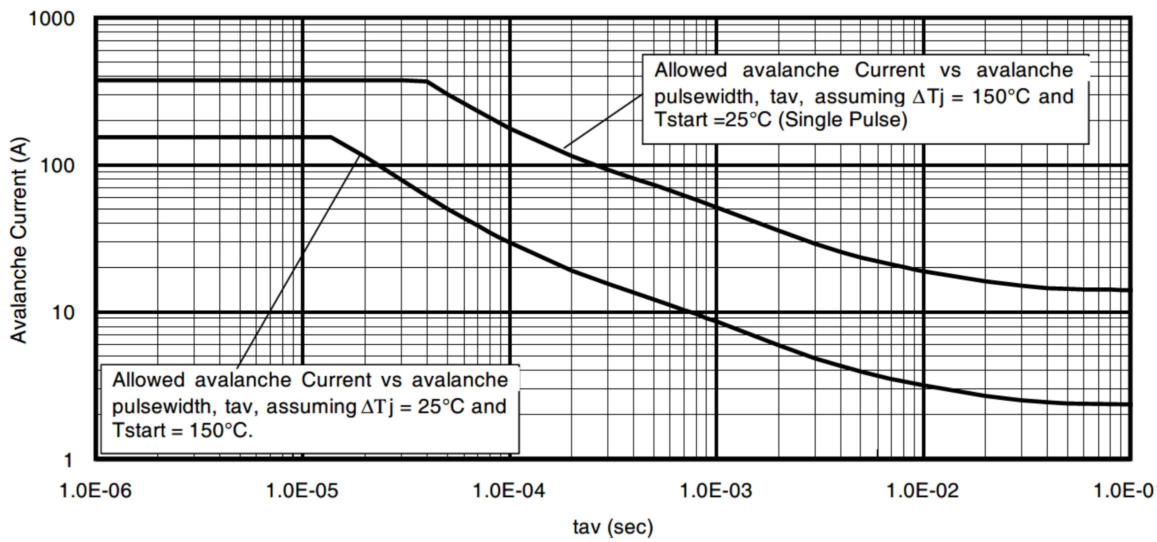


Fig 15. Typical Avalanche Current vs. Pulsewidth

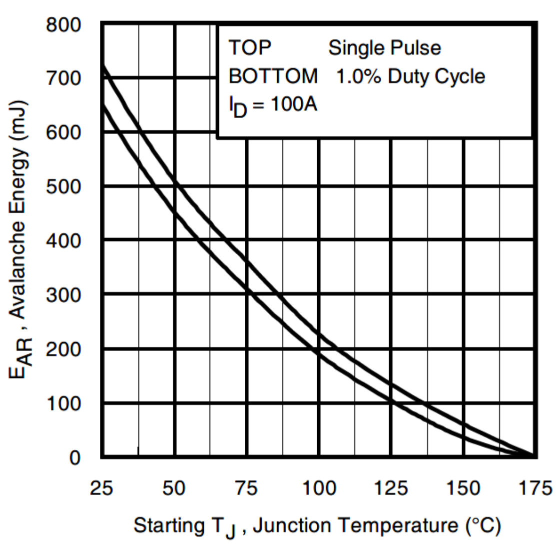


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of Tjmax. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as Tjmax is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D\,(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed Tjmax (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

$$P_{D\,(ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$$

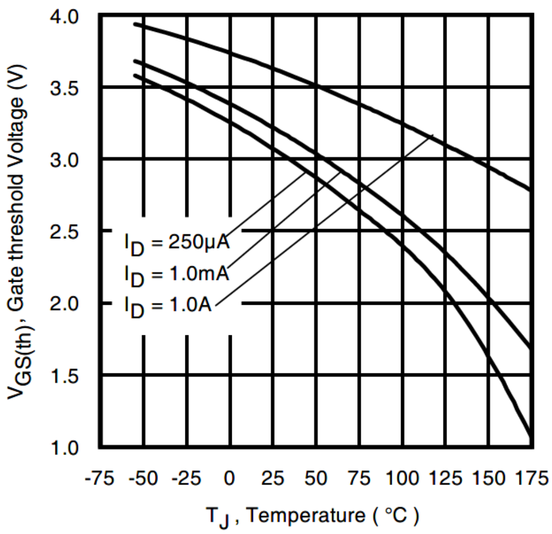


Fig. 17 Threshold Voltage vs. Temperature

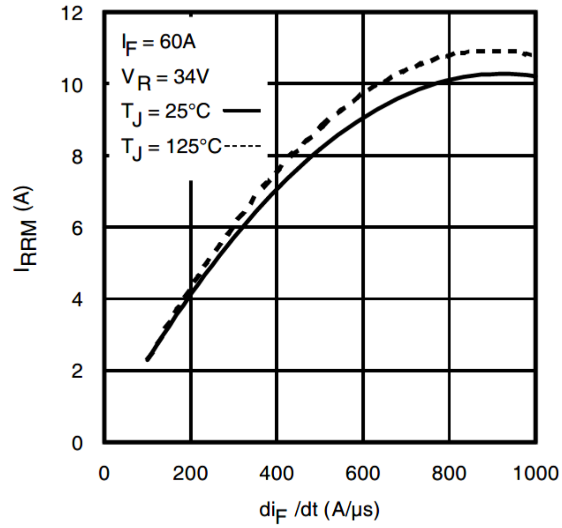


Fig. 18 Typical Recovery Current vs. di_f/dt

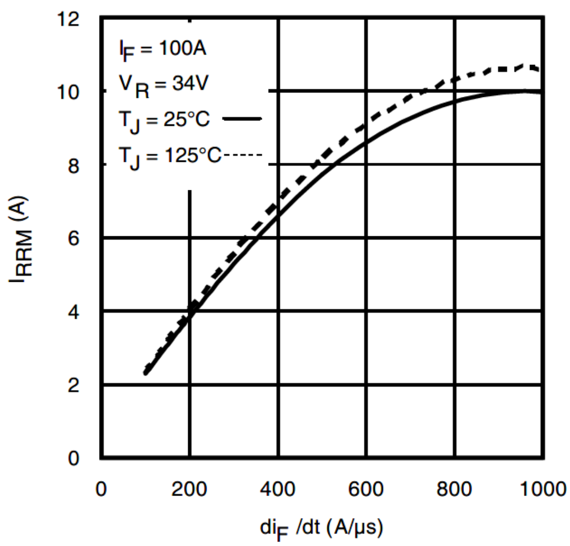


Fig 19. Typical Recovery Current vs. di_f/dt

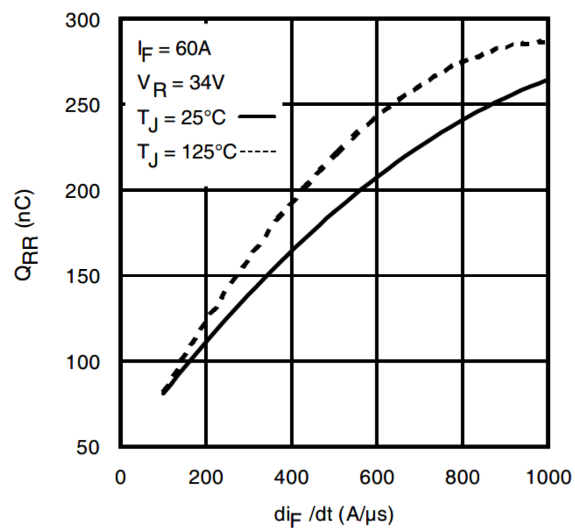


Fig 20. Typical Stored Charge vs. di_f/dt

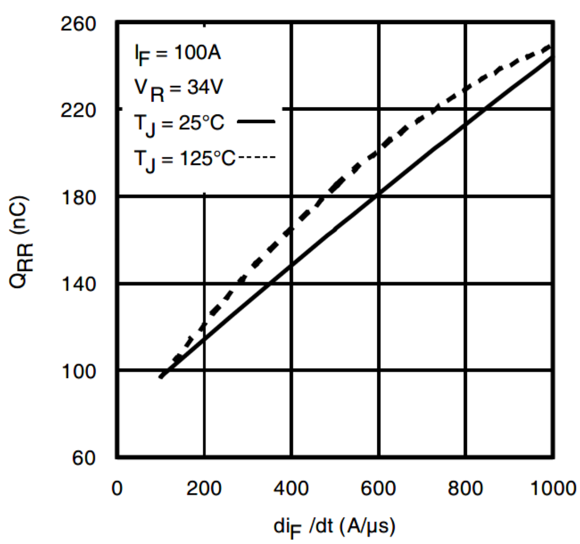
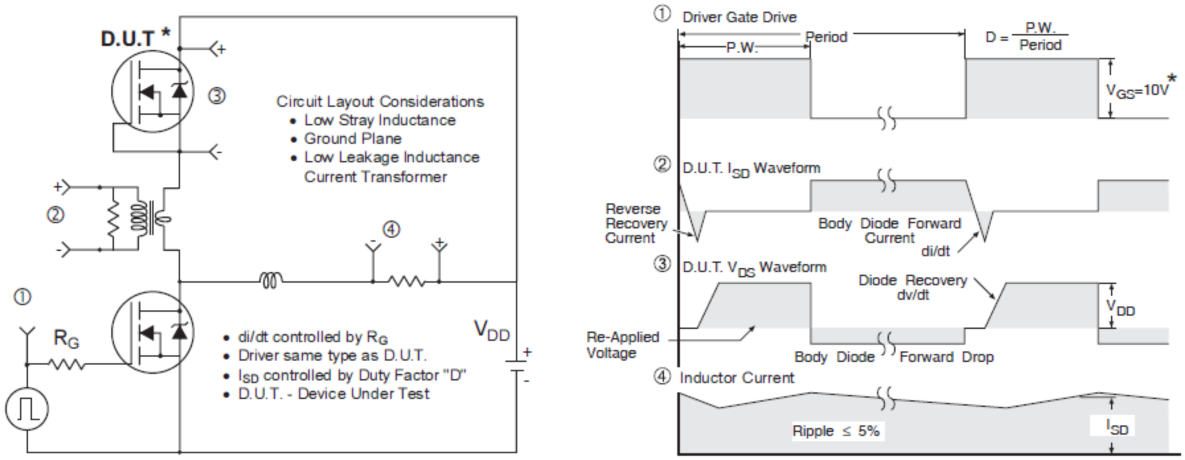


Fig 21. Typical Stored Charge vs. di_f/dt



* Reverse Polarity of D.U.T for P-Channel

* V_{GS} = 5V for Logic Level Devices

Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

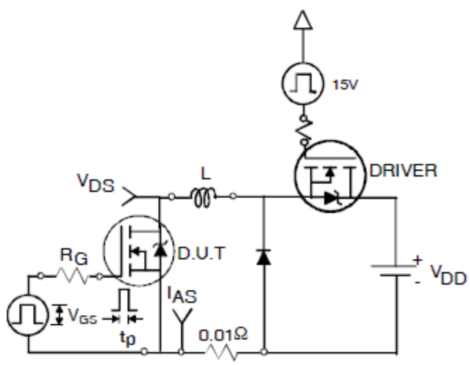


Fig 23a. Unclamped Inductive Test Circuit

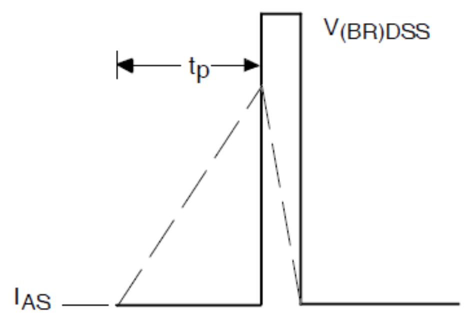


Fig 23b. Unclamped Inductive Waveforms

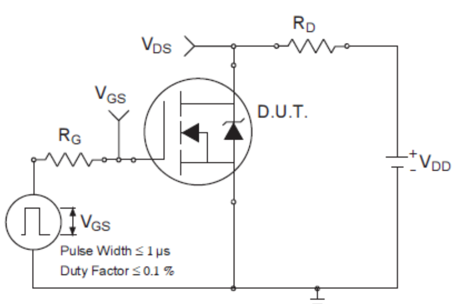


Fig 24a. Switching Time Test Circuit

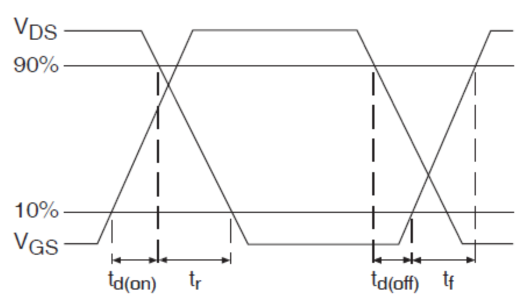


Fig 24b. Switching Time Waveforms

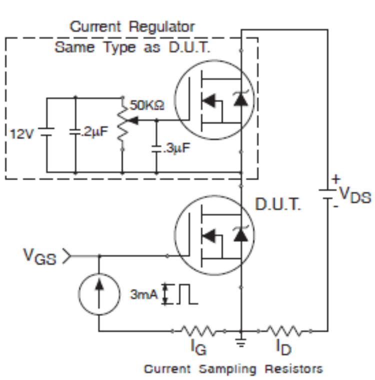


Fig 25a. Gate Charge Test Circuit

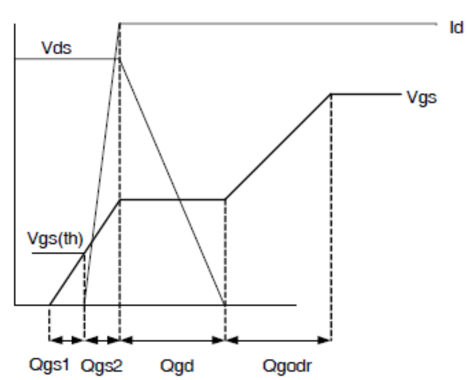
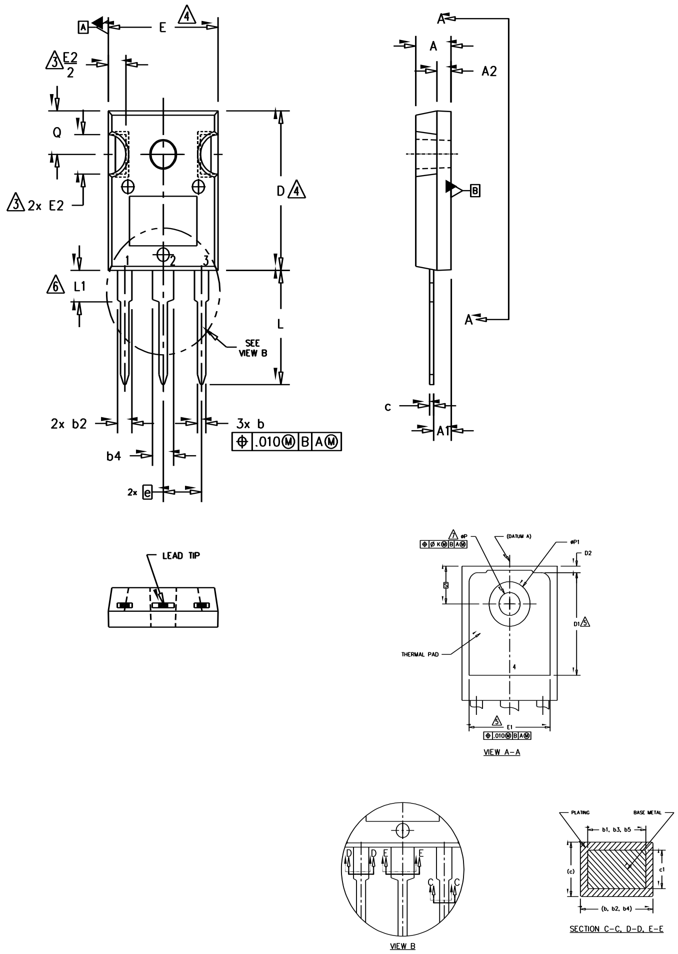


Fig 25b. Gate Charge Waveform

TO-247AC Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

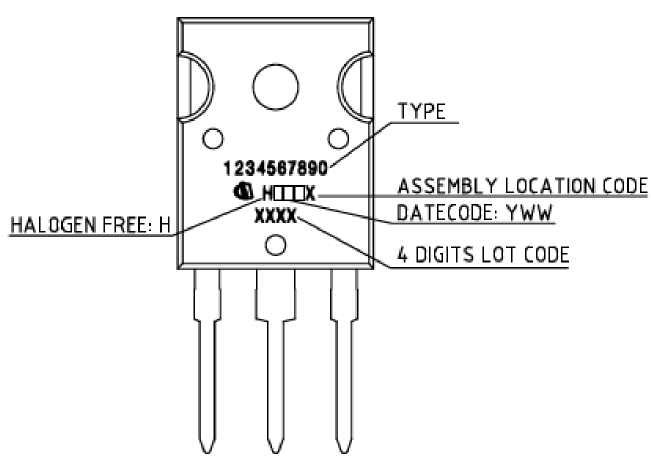
IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

DIODES

1.- ANODE/OPEN
2.- CATHODE
3.- ANODE

TO-247AC Part Marking Information



TO-247AC package is not recommended for Surface Mount Application.

Qualification information†

Qualification level	Industrial (per JEDEC JESD47F)††	
Moisture Sensitivity Level	TO-247AC	N/A
RoHS compliant	Yes	

† Qualification standards can be found at Infineon web site: https://www.infineon.com/
†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Rev.	Comments
2014-04-22	2.1	• Updated data sheet with new IR corporate template • Updated package outline and part marking on page 9 • Added bullet point in the Benefits "RoHS Compliant, Halogen - Free" on page 1
2015-02-19	2.2	• Updated E_{AS} (L=1mH) = 1405mJ on page 2 • Updated note 10 " "Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 53A, V_{GS} =10V" on page 2
2024-10-03	2.3	• Update datasheet to Infineon format • Updated Part marking –page 9 • Added disclaimer on last page.

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For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

The Infineon Technologies component described in this Data Sheet may be used in life support devices or systems and or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.