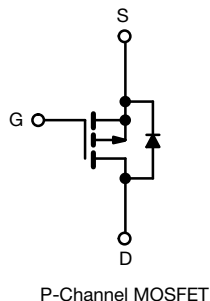


Power MOSFET



P-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- For automatic insertion
- End stackable
- P-channel
- Fast switching
- 175 °C operating temperature
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



PRODUCT SUMMARY

V _{DS} (V)	-100	
R _{DS(on)} (Ω)	V _{GS} = -10 V	1.2
Q _g (Max.) (nC)	8.7	
Q _{gs} (nC)	2.2	
Q _{gd} (nC)	4.1	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD9110PbF

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	-100	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current	V _{GS} at -10 V	T _A = 25 °C	A
		T _A = 100 °C	
Pulsed drain current ^a	I _{DM}	-5.6	
Linear derating factor		0.0083	W/°C
Single pulse avalanche energy ^b	E _{AS}	140	mJ
Repetitive avalanche current ^a	I _{AR}	-0.7	A
Repetitive avalanche energy ^a	E _{AR}	0.13	mJ
Maximum power dissipation	P _D	1.3	W
Peak diode recovery dv/dt ^c	dV/dt	-5.5	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to + 175	°C
Soldering rRecommendations (peak temperature) ^d	For 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DD} = -25 V, starting T_J = 25 °C, L = 52 mH, R_g = 25 Ω, I_{AS} = -2.0 A (see fig. 12)
- I_{SD} ≤ -4.0 A, dI/dt ≤ 75 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C
- 1.6 mm from case

THERMAL RESISTANCE RATINGS

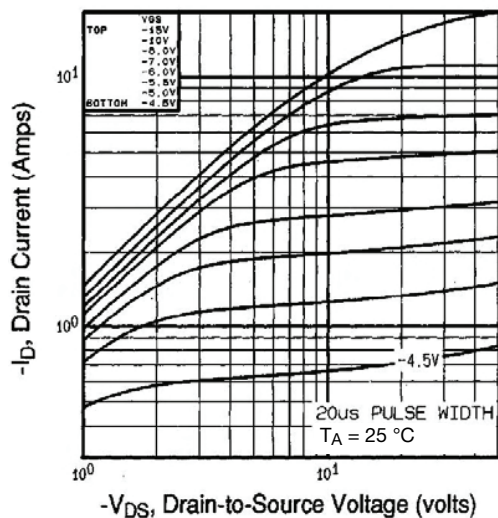
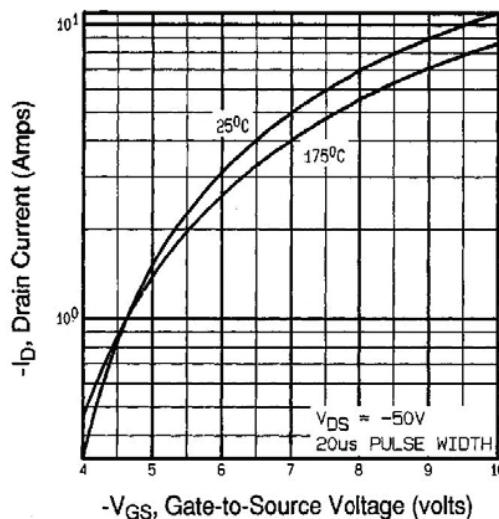
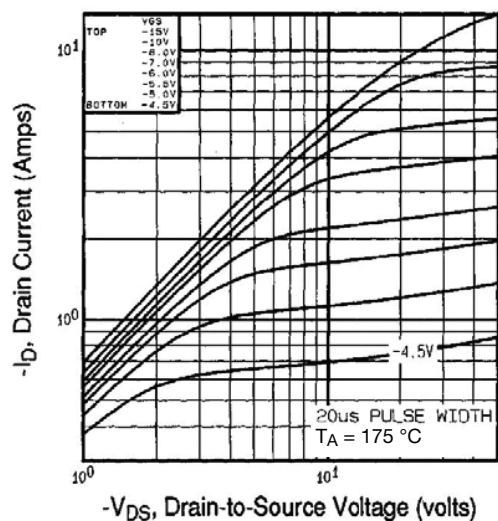
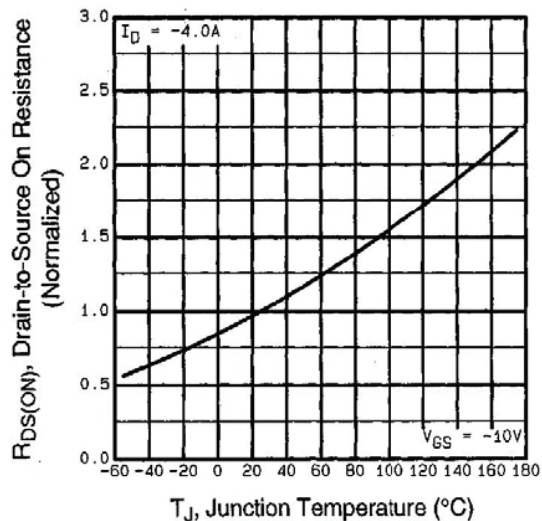
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA		-100	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = -1 mA		-	-0.091	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-2.0	-	-4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -100 V, V _{GS} = 0 V		-	-	-100	μA
		V _{DS} = -80 V, V _{GS} = 0 V, T _J = 150 °C		-	-	-500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -0.42 A ^b	-	-	1.2	Ω
Forward Transconductance	g _{fs}	V _{DS} = -50 V, I _D = -0.42 A		0.60	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -25 V, f = 1.0 MHz, see fig. 5		-	200	-	pF
Output Capacitance	C _{oss}			-	94	-	
Reverse Transfer Capacitance	C _{rss}			-	18	-	
Total Gate Charge	Q _g	V _{GS} = -10 V	I _D = -4.0 A, V _{DS} = -80 V see fig. 6 and 13 ^b	-	-	8.7	nC
Gate-Source Charge	Q _{gs}			-	-	2.2	
Gate-Drain Charge	Q _{gd}			-	-	4.1	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -50 V, I _D = -4.0 A R _g = 24 Ω, R _D = 11 Ω, see fig. 10 ^b		-	10	-	ns
Rise Time	t _r			-	27	-	
Turn-Off Delay Time	t _{d(off)}			-	15	-	
Fall Time	t _f			-	17	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal Source Inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-0.70	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	-5.6	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = -0.7 A, V _{GS} = 0 V ^b		-	-	-5.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = -4.0 A, dI/dt = 100 A/μs ^b		-	82	160	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.15	0.30	μC

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_A = 25\text{ }^{\circ}\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_A = 175\text{ }^{\circ}\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

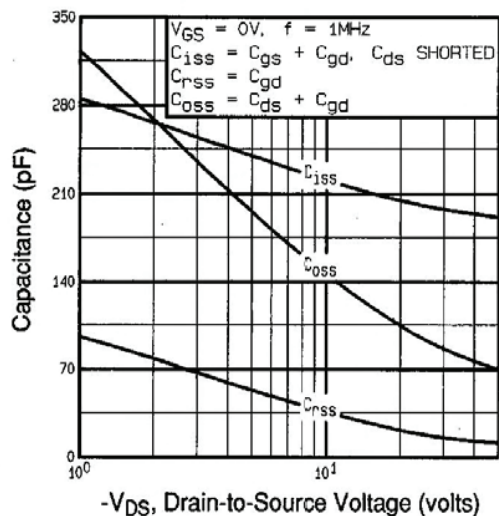


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

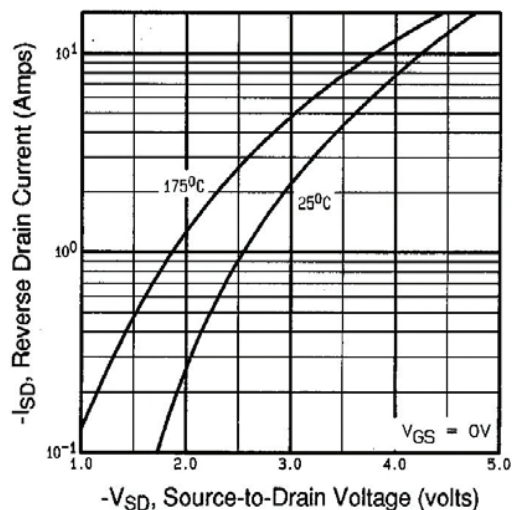


Fig. 7 - Typical Source-Drain Diode Forward Voltage

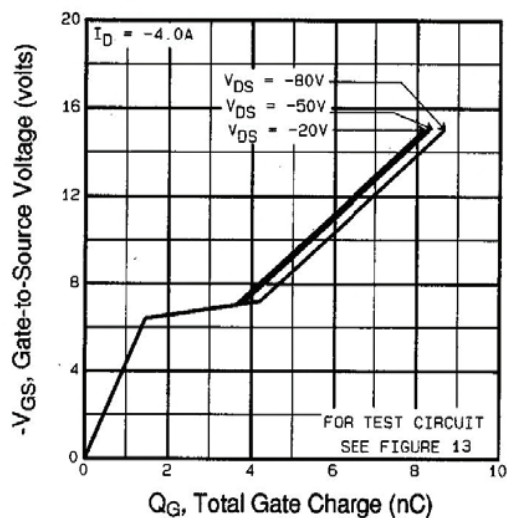


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

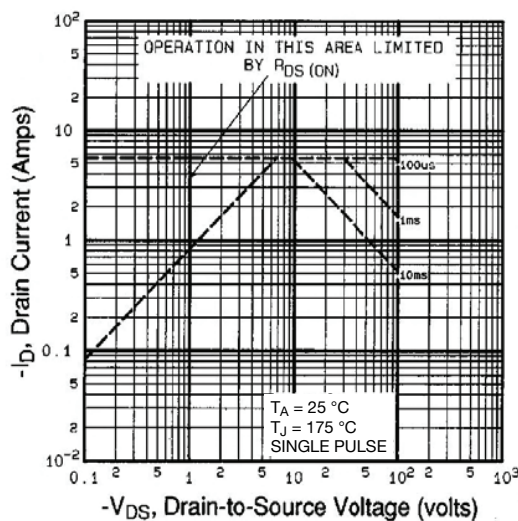
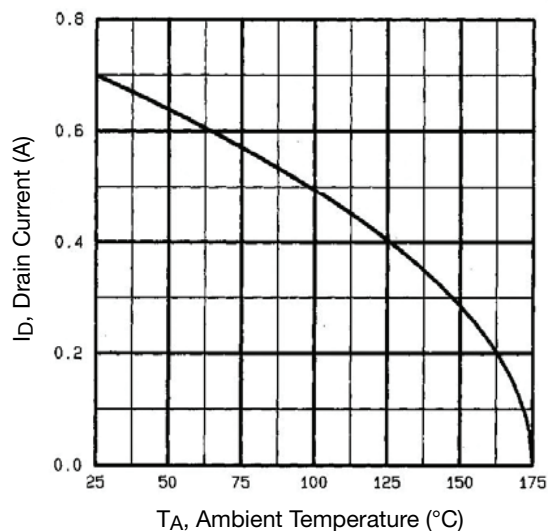
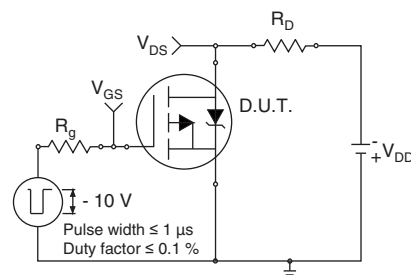
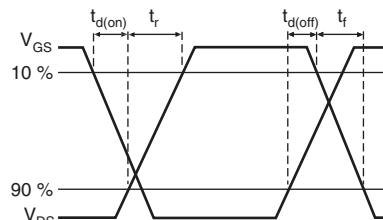
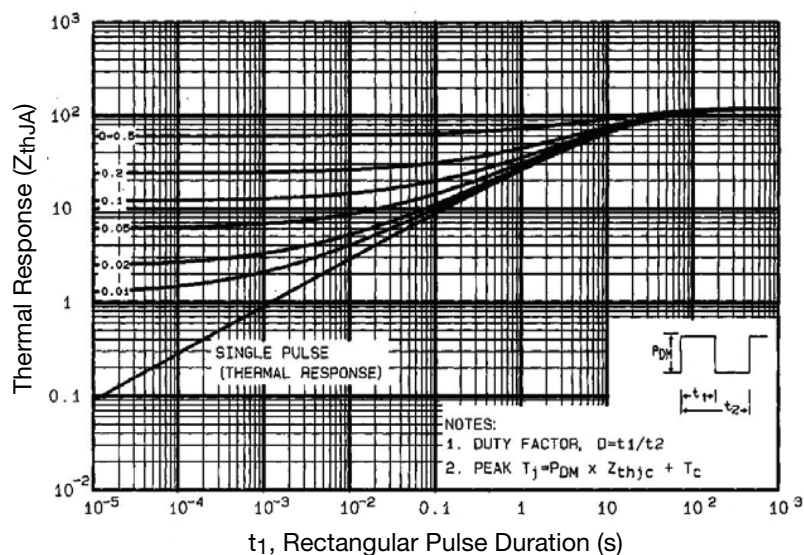


Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

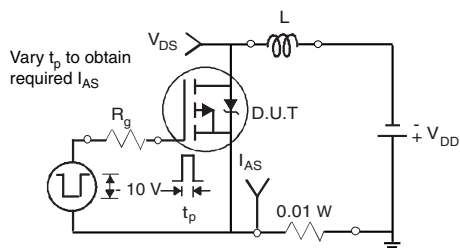
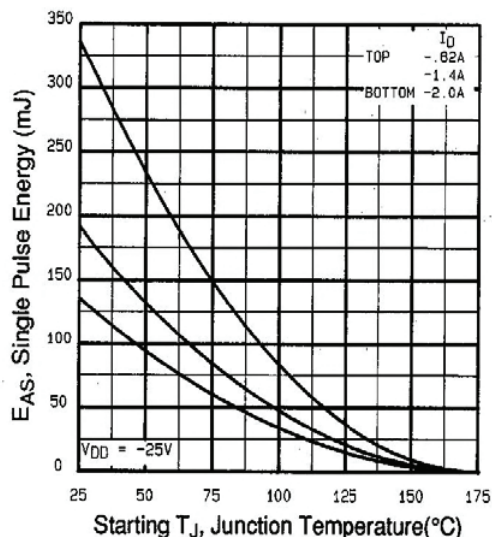
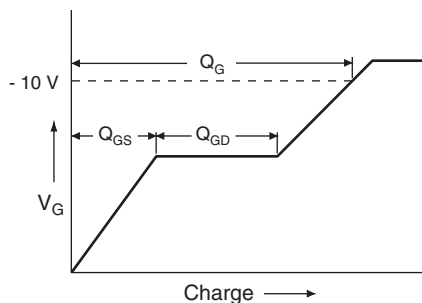
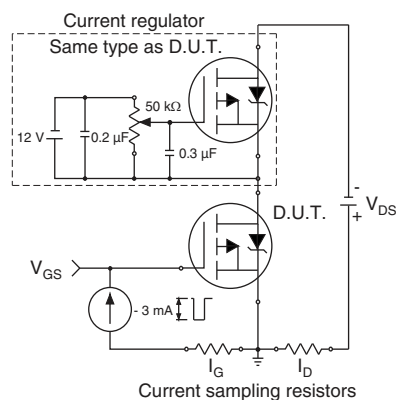

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

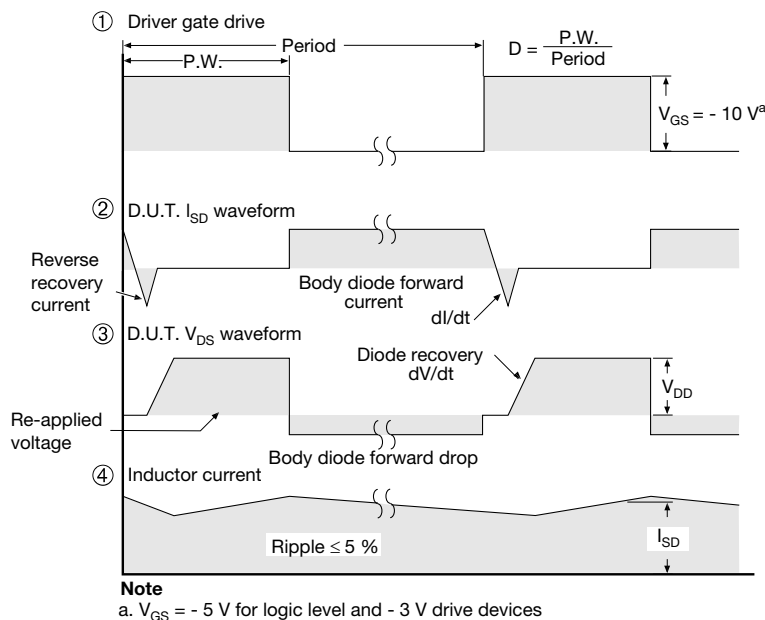
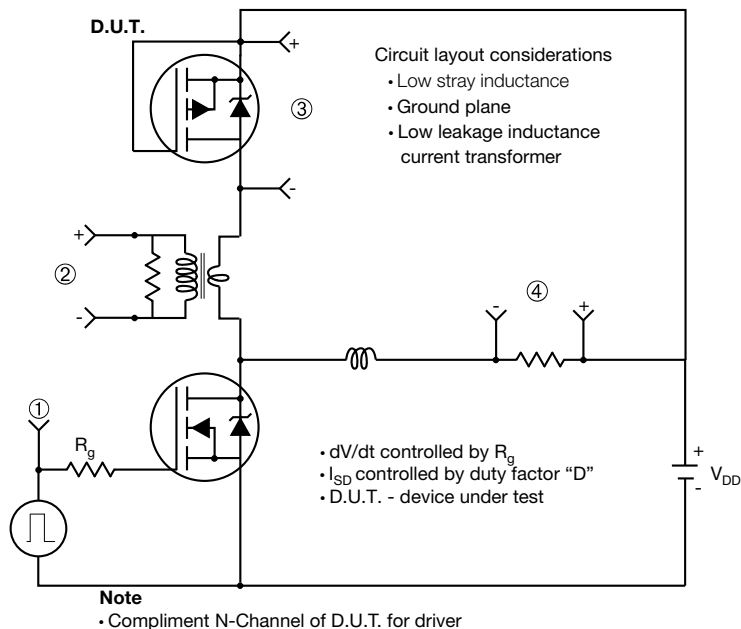
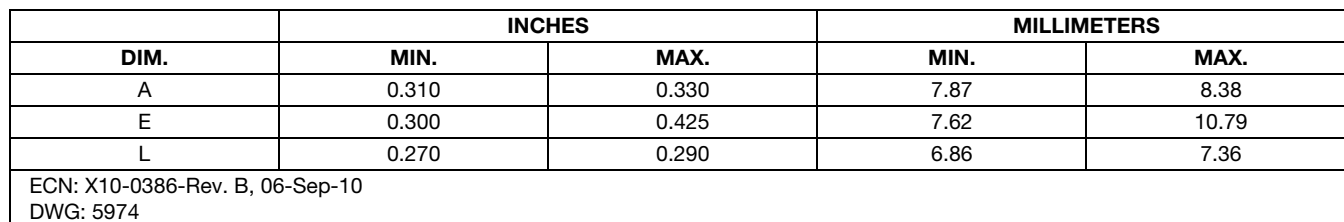


Fig. 14 - For P-Channel

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1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.



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