NCP51820GAN2GEVB

NCP51820 HB GaN Driver Evaluation Board User's Manual

NCP51820 High−Speed, Half−Bridge, GaN Driver Evaluation Board for Existing or New PCB Designs

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EVAL BOARD USER'S MANUAL

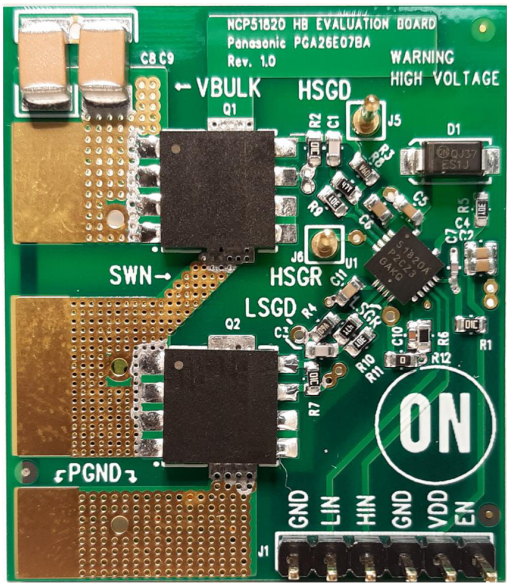


Figure 1. Evaluation Board Photo

INTRODUCTION

Purpose

The NCP51820 HB GaN Driver Evaluation Board (EVB) is intended to replace the driver and power MOSFETs used in existing half−bridge or full−bridge power supplies. This EVB highlights the performance, simplicity and minimal number of components required to efficiently and reliably drive two gallium nitride power switches used in a high−voltage, totem pole configuration. Intended applications include off−line power converter topologies such as: LLC, phase−shifted full−bridge, totem pole PFC, active clamp flyback and forward, dual active−bridge, Phi−2 and high voltage synchronous buck. This document describes the NCP51820 HB GaN Driver EVB mated to a 400 V to 12.5 V LLC converter, as one commonly used example from the topologies listed.

NCP51820 GaN Driver Description

The NCP51820 high−speed, gate driver is designed to meet the stringent requirements of driving enhancement mode (E−mode), high electron mobility transistor (HEMT) and gate injection transistor (GIT) HEMT, gallium nitride (GaN) power switches in off−line, half−bridge power topologies. The NCP51820 offers short and matched propagation delays with advanced level shift technology providing −3.5 V to +650 V (typical) common mode voltage range for the high−side drive and −3.5 V to +3.5 V common mode voltage range for the low−side drive. In addition, the device provides stable and reliable operation when used in high dV/dt environments up to 200 V/ns. In order to fully protect the gates of the GaN power switches against excessive voltage, both NCP51820 drive stages employ separate, dedicated voltage regulators to accurately maintain the gate−source drive signal amplitude. The circuit offers active clamping of the driver's bias rails thus protecting against potential gate−source over−voltage under various operating conditions.

The NCP51820 offers important protection functions such as independent under−voltage lockout (UVLO), monitoring VDD bias voltage, VDDH and VDDL driver bias and thermal shutdown based on die junction temperature of the device. As shown in Figure 2, the Schmitt trigger, EN, HIN and LIN inputs are internally pulled LOW to assure the driver is always in a default 'OFF' state during initial application of V_{DD} bias. Programmable dead−time control is available by the DT pin and can be configured to prevent or allow cross−conduction.

The NCP51820 can be considered as having two independent high−side and low−side "floating" drive stages. The high−side can float up to 650 V referenced to SW and the low−side can float up to 3.5 V referenced to PGND, making it well suited for applications where the driver has to float above a low−side current sense resistor as described in "Connection Method #2" section. Each drive stage includes dedicated input level shifting to ensure accurately matched propagation delays to within 5 ns. Each output includes separate source and sink allowing rise and fall times to be set independently with a single resistor, eliminating additional, discrete circuitry often required for high−speed turn−off.

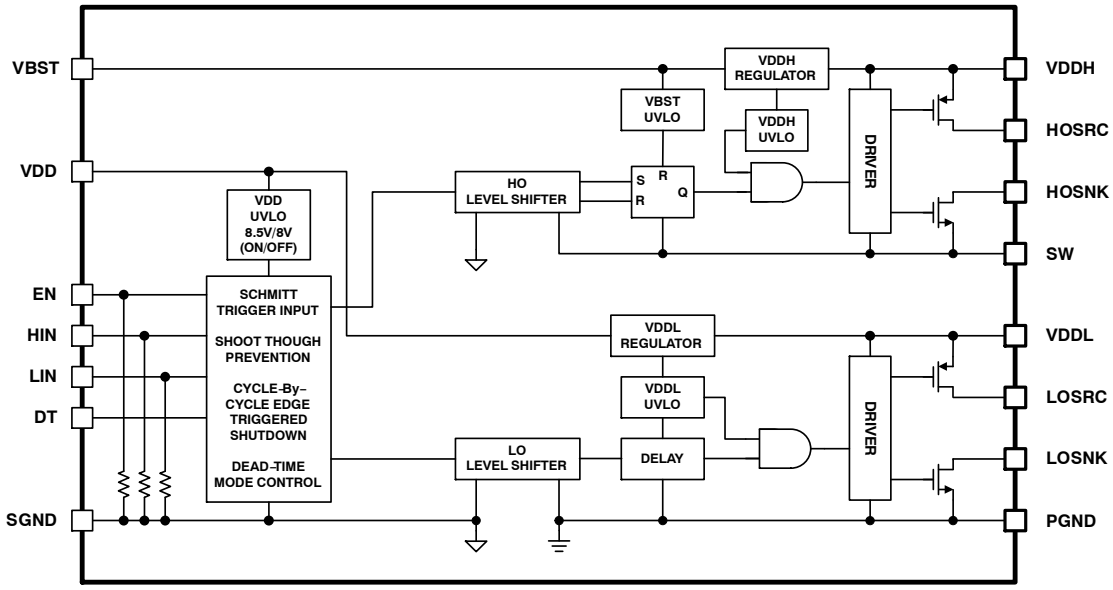


Figure 2. NCP51820, Functional Block Diagram

NCP51820 HB GaN Driver EVB Description

The NCP51820 HB GaN Driver EVB is designed using an 1180 mil x 1310 mil, four−layer printed circuit board (PCB) and includes the NCP51820 GaN driver, two E−mode GaN power switches connected in a high−side, low−side configuration and all necessary drive circuitry. The EVB does not include a PWM controller, and is generic from the point of view that it is not dedicated to any one topology, and can be used in any topology that requires the use of a high−side/low−side FET combination. The EVB can be connected into an existing power supply, and will replace the HS/LS driver and MOSFETs. The EVB has preset, but configurable dead−time control and driver enable/disable. The GaN power switches are rated up to 650 V, 30 A, making them well suited for half−bridge topologies operating from a PFC output in the range of 400 V. However, due to $R_{DS(ON)}$ temperature dependence, the maximum, practical case temperature should not exceed ~90°C (90°C = 1.6 x $R_{DS(ON)}$, normalized at 25°C). The EVB has only 23 components and its small size allows it to be installed in tight areas. Even with the small size, several pins are available to probe the circuit. HS and LS gate drives, as well as SWN are accessible. Note: In half−bridge operation, the HS gate drive can only be probed with a high−voltage differential probe on the Hi−Side Gate Drive (HSGD) pin and the Hi−Side Gate Return (HSGR) pin. The LS gate drive has two plated holes for a tip−and−barrel probe measurement (LSGD). The plated hole closest to the NCP51820 is probe GND, as shown in Figure 3. A tip−and−barrel measurement is performed by removing the "hat" from a passive probe and using the probe "pin" for the measurement and a spring pin fit on the GND barrel of the probe for ground. Figure 4 shows the typical tip−and−barrel measurement method for LSGD using a LeCroy passive probe and GND spring.

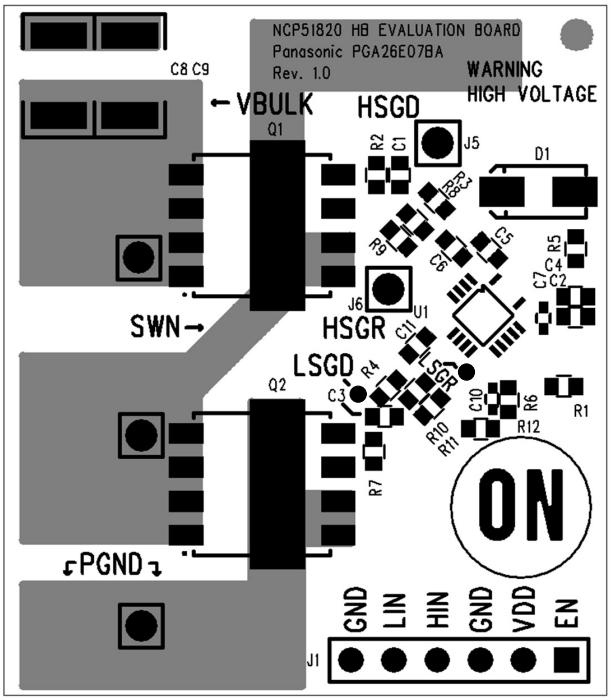


Figure 3. NCP51820 HB GaN Driver EVB

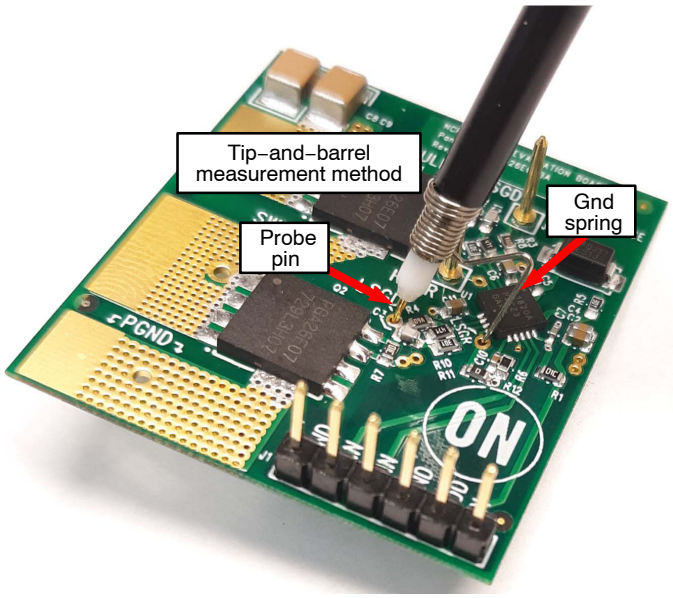


Figure 4. Tip−and−Barrel Measurement Method

NCP51820 EVB Schematic

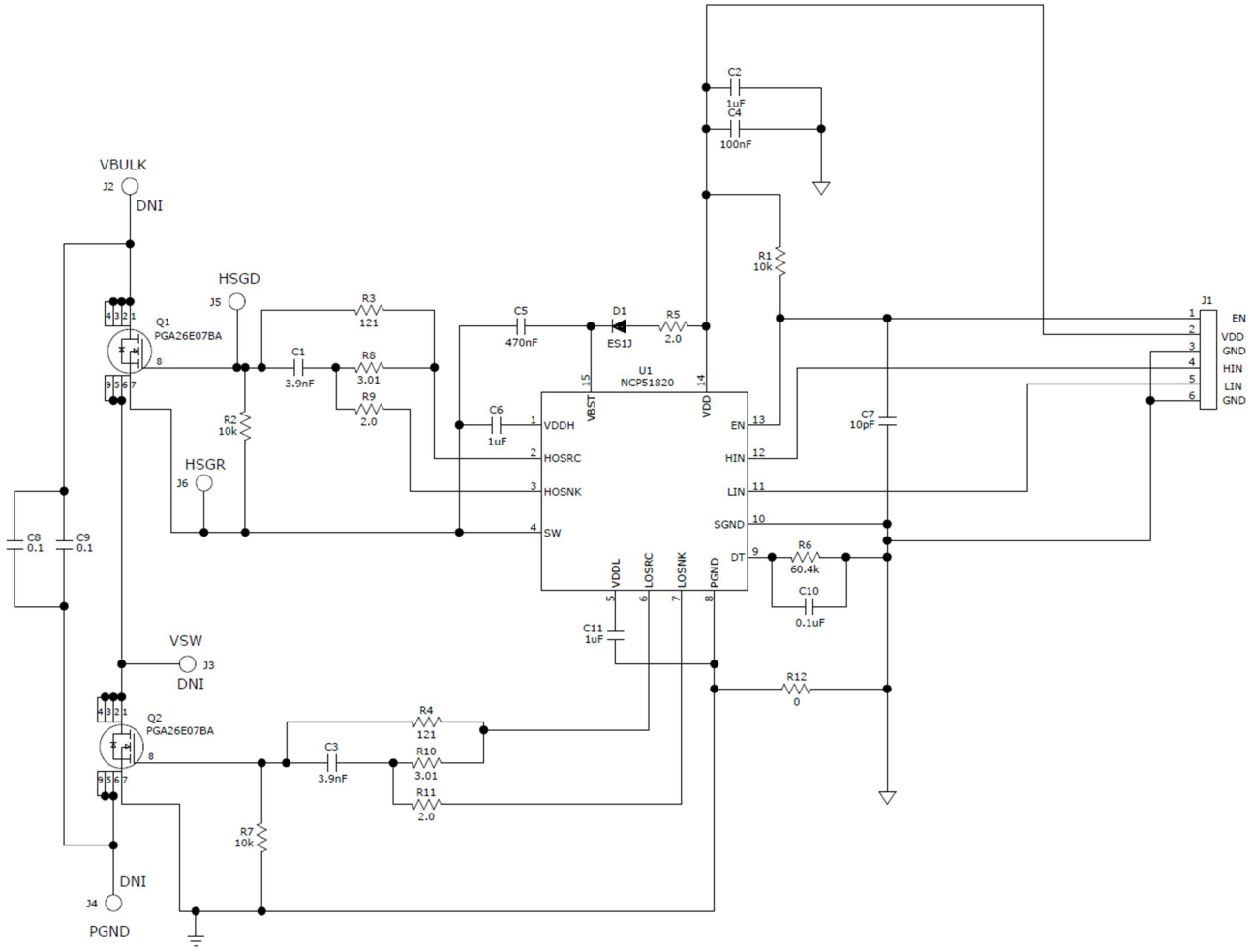


Figure 5. NCP51820 EVB Schematic

NCP51820 EVB Bill of Materials (BOM)

Table 1. NCP51820 EVB BILL OF MATERIALS

Item	Qty	Reference	Value	Part Number	Description	Manufacturer	Pkg Type
1	1	C4	100 nF	CL10B104KA8NNNC	CAP, SMD, CERAMIC, 25 V, X7R	Samsung	603
2	1	C5	470 nF	CL10B474KA8NFNC	CAP, SMD, CERAMIC, 25 V, X7R	Samsung	603
3	1	C7	10 pF	CC0402JRNPO9BN100	CAP, SMD, CERAMIC, 50 V, NPO	Yageo	402
4	1	C10	0.1 μF	GRM155R71E104KE14D	CAP, SMD, CERAMIC, 25V , X7R	Murata	402
5	2	C1,C3	3.9 nF	GCM1885C1H392JA16D	CAP, SMD, CERAMIC, 50 V, NPO	Murata	603
6	3	C2, C6, C11	1 μF	CL10B105KA8NNNC	CAP, SMD, CERAMIC, 25 V, X7R	Samsung	603
7	2	C8−9	0,1	C4532X7R2J104K230KA	CAP, SMD, CERAMIC, 630 V, X7R	TDK	1812
8	1	D1		ES1J	DIODE FAST REC 1 A 600 V	ON Semiconductor	SMA

Table 1. NCP51820 EVB BILL OF MATERIALS (continued)

Item	Qty	Reference	Value	Part Number	Description	Manufacturer	Pkg Type
9	1	J1		61300611121	Connector, Header, 100 Mil spacing	Wurth	Thru−Hole
10	5	J5, J6		1352−1	Testpin, Gold, 40 mil.	Keystone	Thru−Hole
11	3	J2−4	DNI				
12	2	Q1−2		PGA26E07BA	GaNFET, 650 V, 26 A, 56 mΩ	Panasonic	QFN−8x8
13	1	R6 (Note 1)	60.4 kΩ	RC0603FR−0760K4L	RES, SMD, 1/10 W	Yageo	603
14	1	R12 (Note 2)	0 Ω	RC0603JR−070RL	RES, SMD, 1/10 W	Yageo	603
15	3	R1, R2, R7	10 kΩ	RC0603FR−0710KL	RES, SMD, 1/10 W	Yageo	603
16	2	R3−4	121 Ω	RC0603FR−07121RL	RES, SMD, 1/10 W	Yageo	603
17	2	R8, R10	3,01 Ω	RC0603FR−073R01L	RES, SMD, 1/10 W	Yageo	603
18	3	R5, R9, R11	2 Ω	RC0603FR−072RL	RES, SMD, 1/10 W	Yageo	603
19	1	U1		NCP51820	High Speed Half Bridge GaN Driver	ON Semiconductor	MLP 4 × 4−15
20	1			ATS−54375W−C1−R0	Heatsink (optional)	Advanced Thermal	37.5 × 37.5 x 24.5 mm
21	1			LI98−28−28−0.25	Adhesive thermal isolator (optional)	T−Global Tech.	37.5 × 37.5 mm

1. R6 used to set dead−time (DT).
2. R12 used to connect SGND to LS gate return.

PGA26E07BA Gate Drive Circuit

The PGA26E07BA GaN switch used in this EVB is a GIT (Gate Injection Transistor). GITs have internal gate voltage clamps, and require a specific gate−drive circuit to ensure full turn−on, as shown in Figure 6. In this gate drive circuit, R_{CLAMP} is used to provide a constant current during turn−on to the GIT gate clamp, which is necessary for proper gate clamp operation. R_{SRC} and R_{SNK} are used to provide the turn−on and turn−off signals to the GIT gate. C_{GD} allows the turn on and turn off signals to pass to the GIT gate, but blocks the clamp current from the SRC and SNK pins. R_{PD} is the pull−down resistor for the GIT gate.

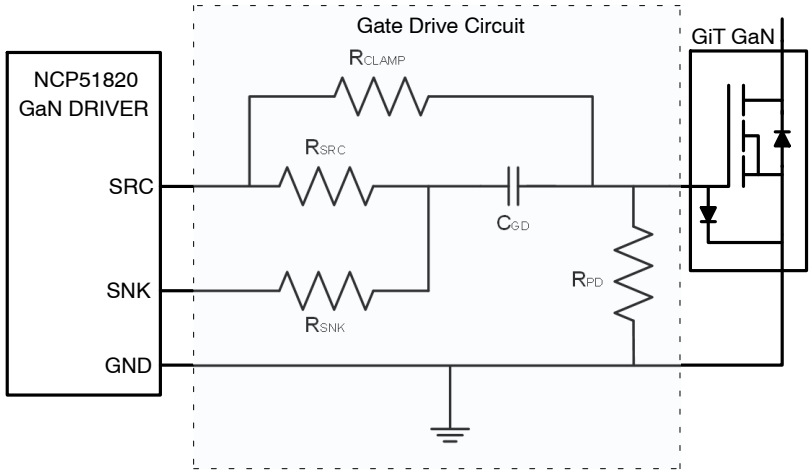
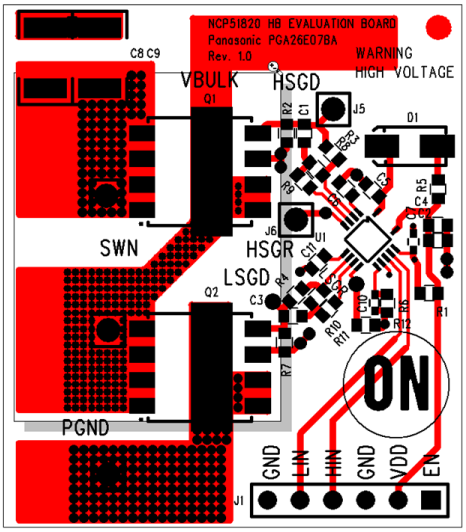


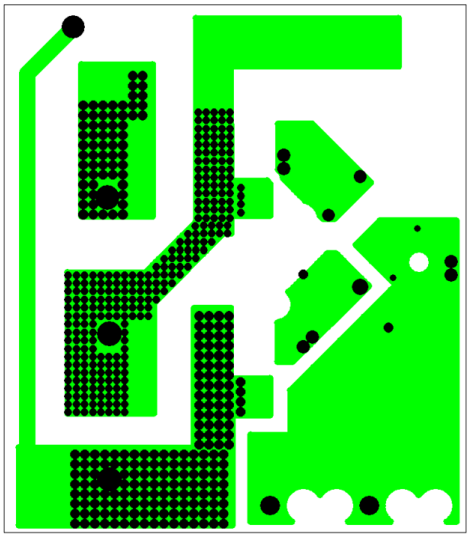
Figure 6. PGA26E07BA Gate Drive Circuit

NCP51820 Layers

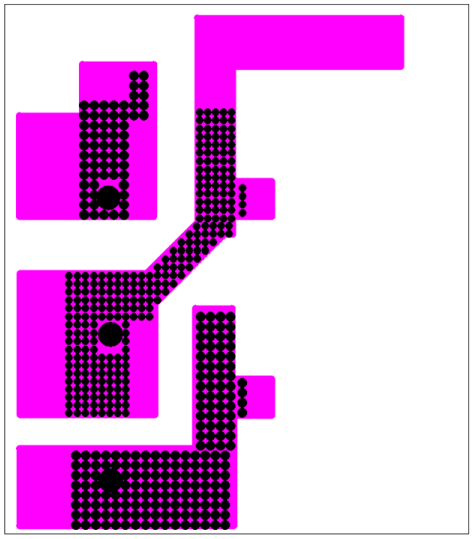
- **Top Layer:** All EVB components are on the top layer. The large copper high current carrying etches used to connect the HS/LS GaN power switches also act as heat spreaders.
- **Layer 2 (Internal):** This layer has a shielding plane for the driver and driver components as well as additional high current carrying etches for the HS/LS GaN power switches.
- **Layer 3 (Internal):** Layer 3 has additional high current carrying etches for the HS/LS GaN power switches.
- **Bottom Layer:** The high current carrying etches for the HS/LS GaN power switches on the bottom layer also act as heat spreaders. A heatsink (if utilized) will be attached to this layer.



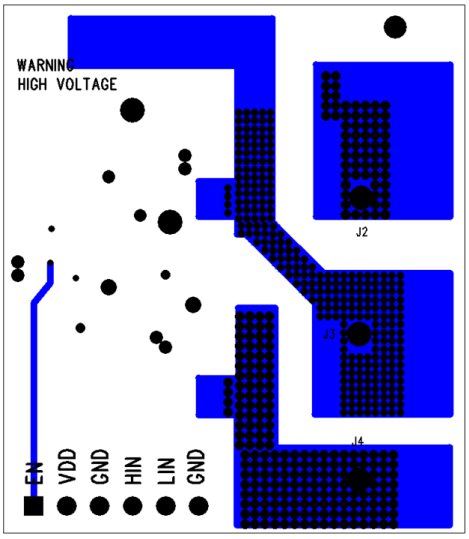
Top Assembly Layer



Layer 2, Internal



Layer 3, Internal



Bottom Layer

Figure 7. PCB Assembly and Layers

NCP51820 EVB I/C Connections

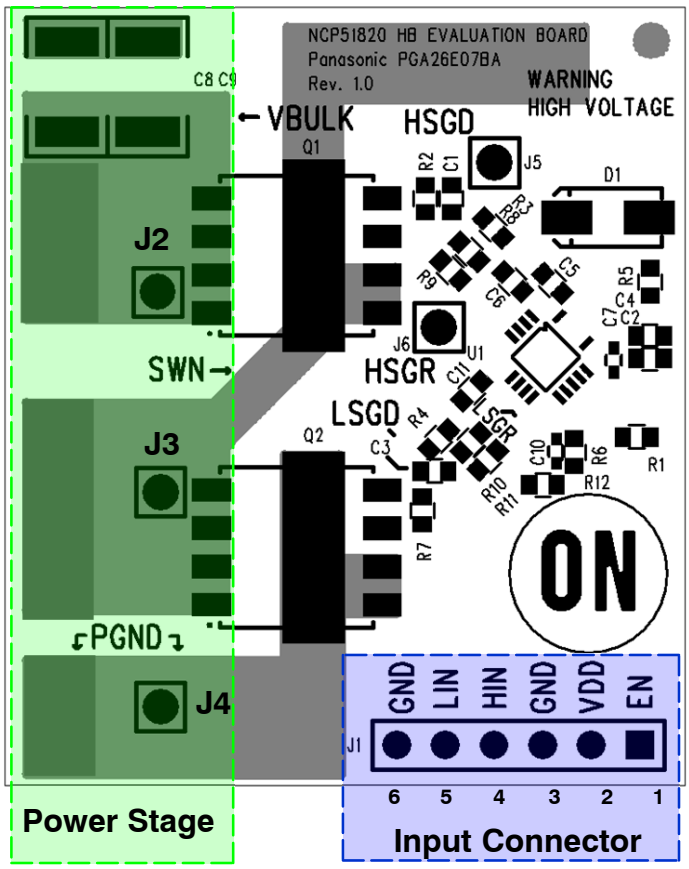


Figure 8. EVB I/O Connections

Table 2. I/O CONNECTOR DESCRIPTION

Pin Name	Pin Type	Description	Value
EN (Note 3)	J1−1	Logic input for enabling/disabling the driver	2.5 V < EN < V_{DD} + 0.3 V
VDD	J1−2	Bias voltage for high current driver	8 V < V_{DD} < 20 V
GND	J1−3,6	Signal ground on the driver	0 V
HIN	J1−4	Logic input for high−side gate driver	0 V< HIN < V_{DD} + 0.3 V
LIN	J1−5	Logic input for low−side gate driver	0 V< LIN < V_{DD} + 0.3 V
VBULK	J2 and PAD	VIN connection	650 V max
SWN	J3 and PAD	Switch Node connection	650 V max
PGND	J4 and PAD	Power Ground connection	0 V

3. EN pin tied to driver V_{DD} through 10 kΩ resistor (R1) on EVB.

NCP51820 EVB CONNECTION METHODS

There are two different methods for connecting the EVB to an existing power board.

Power topologies not using a current sense resistor connected in series with the LS GaN power switch source (a current sense transformer or other method of sensing current used) will use Connection Method #1, shown in "Connection Method #1" section.

Power topologies using a current sense resistor (R_{CS}) connected in series with the LS GaN source, will use Connection Method #2, shown in "Connection Method #2" section.

Preparing Power Board for EVB Connection

1. Remove HS and LS MOSFETs and HS and LS gate drive resistors from the power board as illustrated in Figure 9.
2. Remove any gate turn off circuitry. This is any circuit used to help drive the gate to 0 V during turn off.
3. Before connecting the EVB, ensure that VDD, HIN, LIN, and VBULK are within the parameters listed in Table 2.

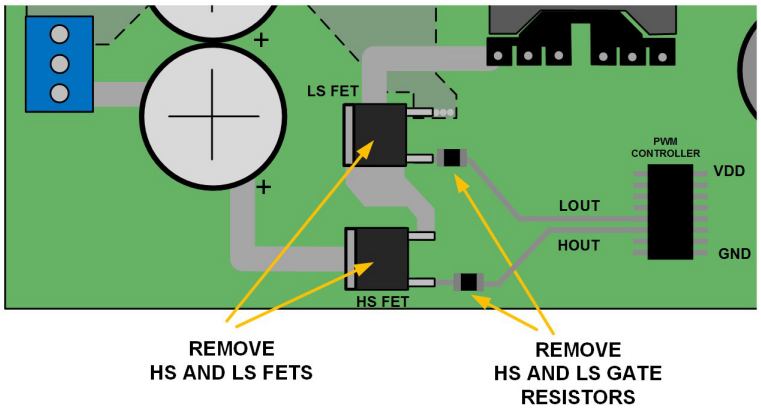


Figure 9. Power Board Preparation

Connection Method #1 – No GaN LS Current Sense Resistor on Power Board

Connect the EVB as shown in Figure 10. AWG #22 wire is suggested for LIN, HIN and VDD. AWG #18 or larger wire is suggested for VBULK, SWN and PGND. Keeping both the Input connections and the VBLK, SWN and PGND connections as short as possible is preferred.

Connection Method #2 – LS GaN Current Sense Resistor (R_{CS}) Present on Power Board

Low−power applications, such as an active−clamp flyback or forward converter often use a current sensing resistor, R_{CS}, located in the low−side GaN power switch-source leg. In such applications, the EVB PGND and SGND pins must be isolated on the EVB (normally connected by R12) because R_{CS} would essentially be shorted through this resistor if not removed. The NCP51820 low−side drive circuit is able to withstand −3.5 V to +3.5 V of common mode voltage. Since most current sense voltage signals are less than 1 V, the low−side drive stage can easily "float" above the voltage, V_{RCS}, generated by the current sense resistor.

Connection Method #2: Remove R12 on the EVB to isolate LS gate drive return from GND as shown in Figure 11 and Figure 14. Failure to remove R12 will short out R_{CS}. Connect the EVB as shown in Figure 11. AWG #22 wire is suggested for LIN, HIN and VDD. AWG #18 or larger wire is suggested for VBULK, SWN and PGND. Keeping both the input and power connections as short as possible is preferred.

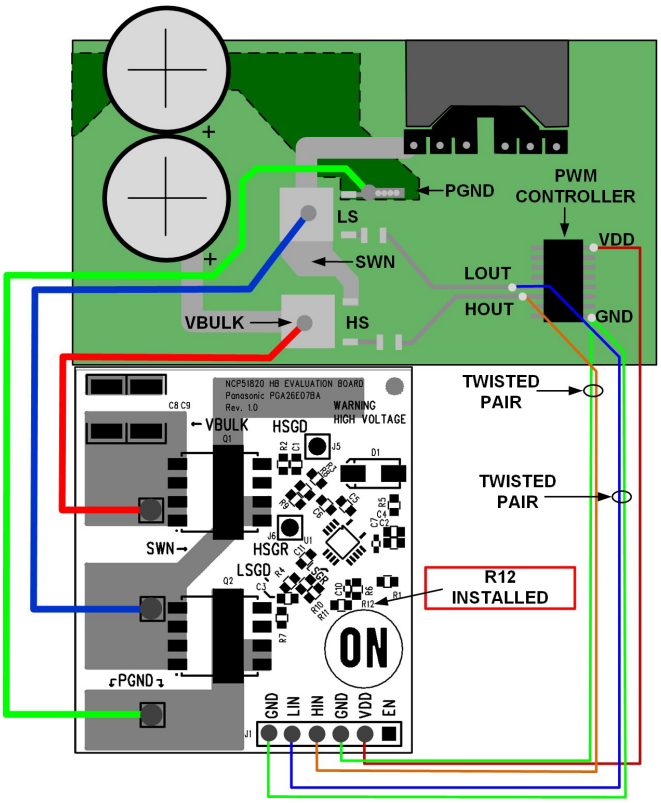


Figure 10. Connection Method #1 – No LS Current Sense Resistor

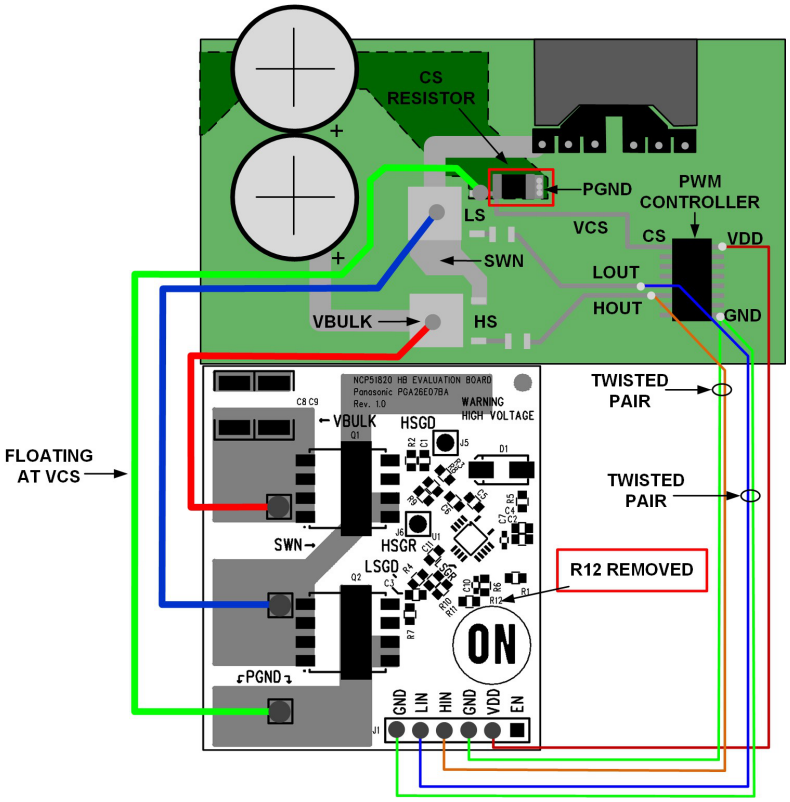


Figure 11. Connection Method #2 – LS Current Sense Resistor on Power Board

External VDD

An external VDD can be used, as long as the HIN and LIN signals still fall within the parameters listed in Table 2. If an external VDD is used, the external VDD GND connection must be connected to the power board VDD GND, as shown in Figure 12. An external VDD can be used for boards either with or without an LS Current Sense Resistor. When using an external VDD, put a 1N4148 blocking diode (or similar 60 V, 1A minimum diode) in series with VDD + to protect the VDD supply. It's also suggested to put a small electrolytic decoupling capacitor (example: 22 μF, 35 V) across the External VDD supply output, as shown in Figure 12. VDD voltage should be measured and set after the blocking diode to take into account the voltage drop across the diode.

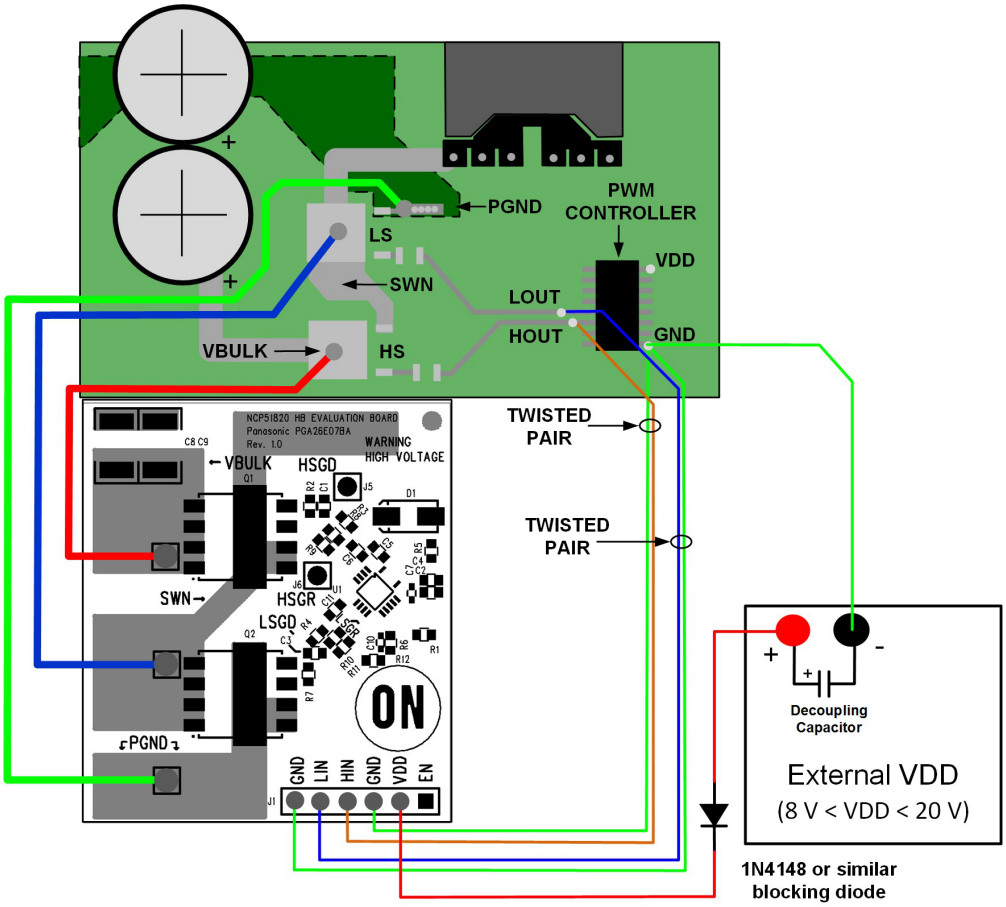


Figure 12. External VDD Connection

Thermal Considerations

Applications where higher currents could cause GaN power switch temperatures to exceed 90°C (such as a high voltage, synchronous buck), a voltage−isolated adhesive heatsink can be attached to the bottom of the EVB. The GaN power switches on this EVB are bottom−cooled. Copper heat spreaders are part of the bottom layer of this EVB. A voltage−isolated adhesive heatsink attached to the EVB bottom will aid in reducing the GaN power switch temperatures. Figure 13 shows the positioning of a heatsink.

NOTE: The heatsink is positioned so the input pins are exposed on the PCB bottom. A sample heatsink and adhesive thermal pad are listed as optional components on the BOM (Table 1).

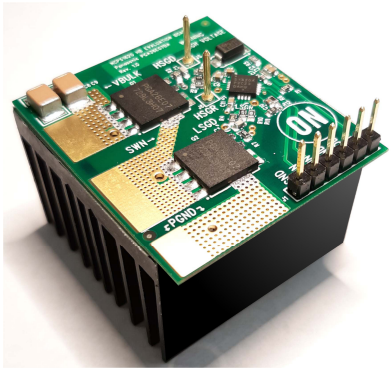


Figure 13. NCP51820 HB GaN Driver EVB and Heatsink

CONFIGURING ENABLE (EN) AND DEAD−TIME (DT)

EN Function and External Control

The NCP51820 GaN Driver EN is internally pulled low to SGND, so the driver is always defaulted to a disabled output status. Similar to HIN and LIN, EN is a Schmitt trigger TTL compatible input. Pulling the EN pin above 2.5 V typical, enables the outputs, placing the NCP51820 into an active ready state. Due to the nature of high−speed switching associated with GaN power stages, and for improved noise immunity, the EN pin is tied to V_{DD} through a 10−kΩ (R1) pull−up resistor and is bypassed by a 10 pF capacitor (C7). If an external enable signal is preferred, the external enable signal must conform to the value limits listed in Table 2. More information on EN control can be found in the NCP51820 datasheet.

When using an external active enable signal, remove R1 and connect a signal to the EN pin on the EVB. The external enable signal GND must connect to the EVB GND. The 10 pF EN bypass capacitor (C7) on the EVB must remain installed. Refer to Figure 14 for R1 and C7 locations.

DT Function and Mode Configuration

Accurately ensuring some minimal amount of dead−time between the high−side and low−side gate drive output signals is critical for safe, reliable optimized operation of any high−speed, half−bridge power stage. The NCP51820 uses a voltage−configured, dead−time control pin (DT). The NCP51820 offers four unique mode settings to utilize dead−time in such a way to be fully compatible with any control algorithm.

The EVB dead−time is preset to Mode B by a single, 60.4 kΩ resistor (R6) connected between the DT and SGND pins. This sets the dead−time voltage to 1.3 V, proportional to approximately 65 ns of dead−time. When adjusting the dead−time is required, the resistor value can be changed, which will change the voltage level on the DT pin. Follow the instructions outlined In DT Mode Descriptions to change DT modes. For noise immunity, the DT pin is bypassed with a 0.1 μF capacitor (C10). This capacitor must not be removed. More information on dead−time control can be found in the NCP51820 datasheet. Refer to Figure 14 for R6 and C10 locations.

DT Mode Descriptions

1. MODE A: Connect DT to SGND; When the DT pin voltage, V_{DT}, is less than 0.5 V typical (R_{DT} = 0 Ω), the DT programmability is disabled and fixed dead−time, anti−cross−conduction protection is enabled. If HIN and LIN are overlapping by X ns, then X ns of dead−time is automatically inserted. Conversely, if HIN and LIN have greater than 0 ns of dead−time then the dead−time is not modified by the NCP51820 and is passed through to the output stage as defined by the controller. This type of dead−time control is preferred when the controller will be making the necessary dead−time adjustments but needs to rely on the NCP51820 dead−time control function for anti−cross−conduction protection.
2. MODE B: Connect a 25 kΩ < R_{DT} < 200 kΩ Resistor from DT to SGND; Dead−time is programmable by a single resistor connected between the DT and SGND pins. The amount of desired dead time can be programmed via the dead time resistor, R_{DT}, between the range of 25 kΩ < R_{DT} < 200 kΩ to obtain an equivalent dead−time, proportional to R_{DT}, in the range of 25 ns < t_{DT} < 200 ns. If either edge between HIN and LIN result in a dead−time less than the amount set by R_{DT}, the set DT value shall be dominant. If either edge between HIN and LIN result in a dead−time greater than the amount set by R_{DT}, the controller dead−time shall be dominant.
3. MODE C: Connect a 249 kΩ Resistor from DT to SGND; Connect a 249 kΩ resistor between DT and SGND to program the maximum dead−time value of 200 ns. The control voltage range, V_{DT}, for assuring t_{DT} = 200 ns is 4 V < V_{DT} < 5 V.
4. MODE D: Connect DT to VDD; When the DT pin voltage, V_{DT}, is greater than 6 V (pulled up to VDD through 10 kΩ resistor), anti−cross−conduction protection is disabled, allowing the output signals to overlap. If choosing this operating mode while driving a half−bridge power stage, extreme caution should be taken, as cross conduction can potentially damage power components if not accounted for. This type of dead−time control is preferred when the controller will be making extremely accurate dead−time adjustments and can respond to the potential of over−current faults on a cycle−by−cycle basis.

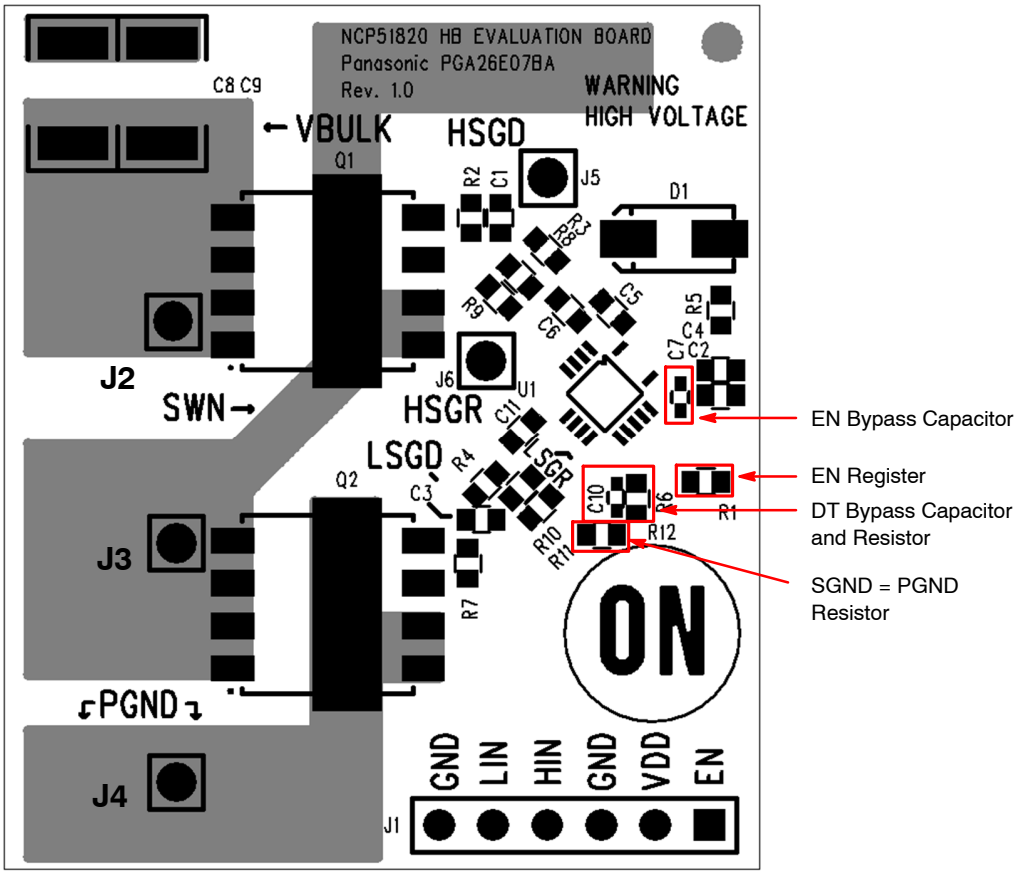


Figure 14. EN and DT Resistor and Capacitor Locations

NCP51820 HB GaN DRIVER EVB TEST EXAMPLE

NCP51820 HB GaN Driver EVB Mated to a FAN7688 LCC Resonant 250 W Converter

The NCP51820 HB GaN Driver EVB was mated to an LLC Resonant 250 W, 400 V to 12.5 V converter featuring ON Semiconductor's FAN7688, a secondary−side LLC resonant, pulse frequency modulated (PFM) controller with dedicated Synchronous Rectification (SR) drive, which offers best in class efficiency for isolated DC/DC converters.

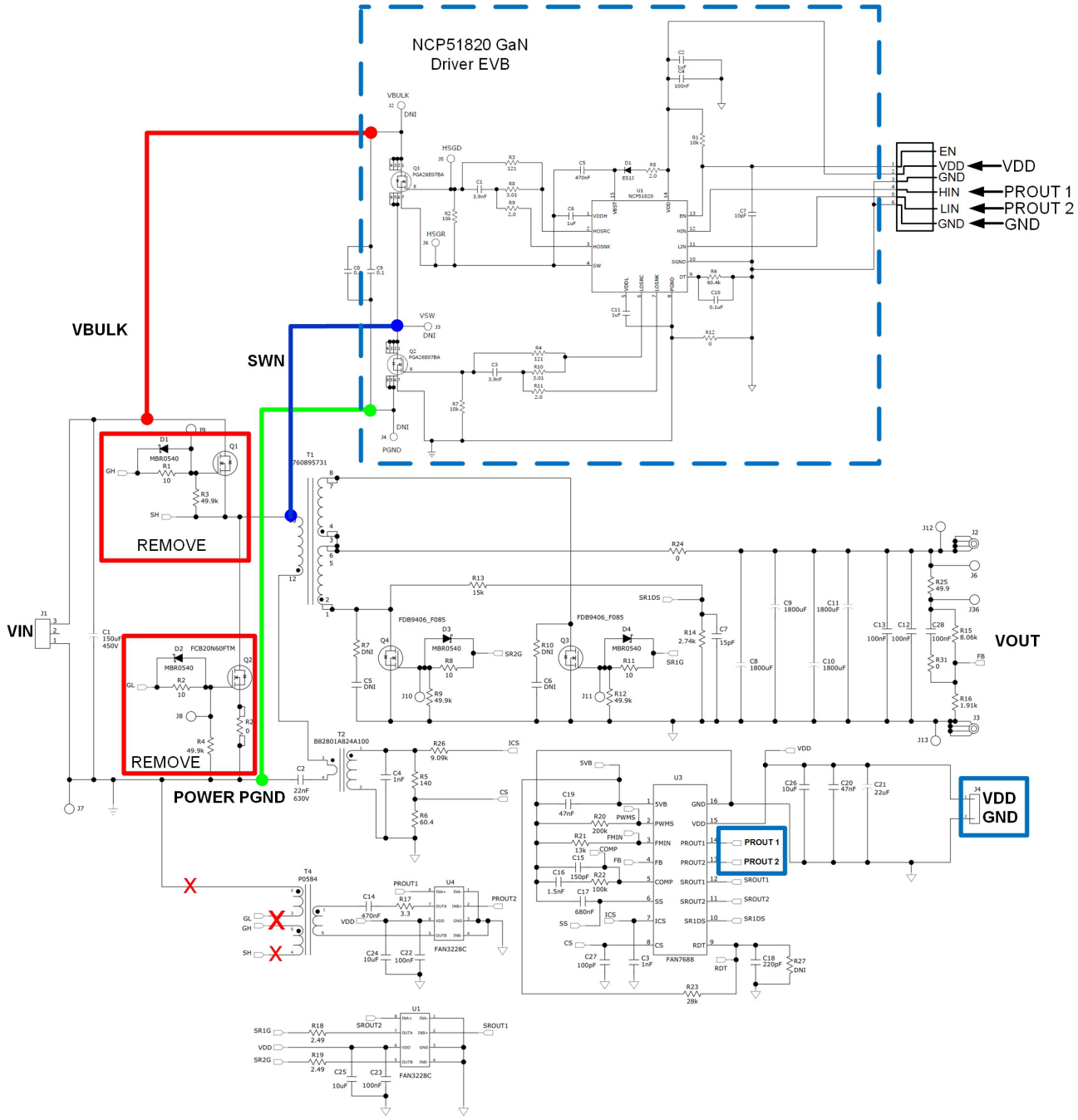


Figure 15. FAN7688 LLC with NCP51820 HB GaN Driver EVB Installed

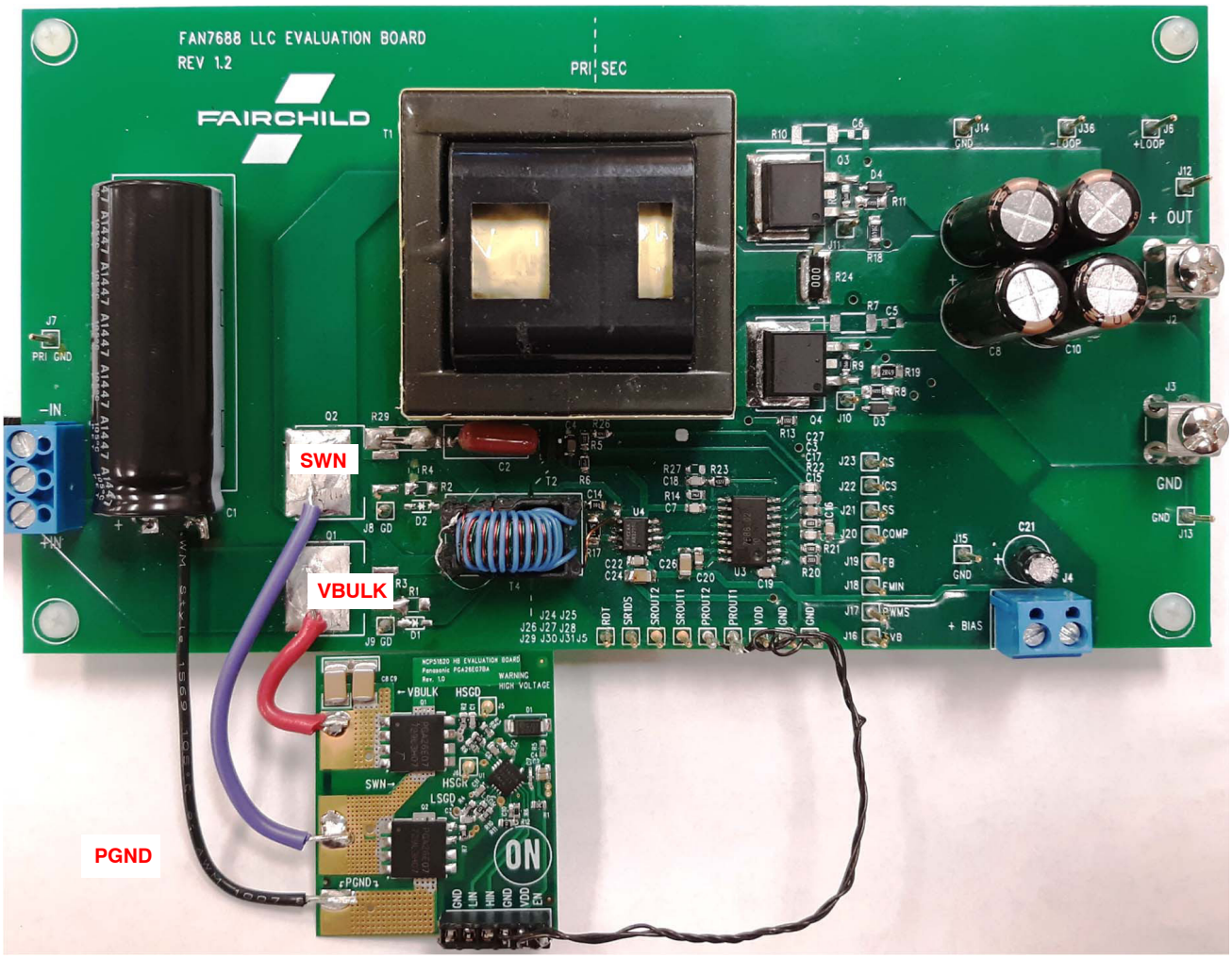


Figure 16. FAN7688 LLC with NCP51820 HB GaN Driver EVB Installed

As shown in Figure 15 and Figure 16, the NCP51820 HB GaN Driver EVB is being used to replace the MOSFETs and driver circuitry in a FAN7688 250 W, 400 V to 12.5 V LLC converter. The FAN7688 board MOSFETs and gate drive resistors were removed. The EVB was wired into the board with the power connections coming from VIN, SWN and Power GND on the main board and VDD, GND, HIN and LIN coming from the FAN7688 PWM controller. Because VDD for the FAN7688 LLC converter is 12 V, the main board VDD was used for the EVB VDD. An external enable was not needed, so the existing pull up resistor, R1 (10 kΩ) on the EVB was left installed. The preset dead−time resistor, R4 (60.4 kΩ) ~ 65 ns was also left as−is on the EVB.

Test Conditions

The FAN7688/NCP51820 HB GaN Driver EVB was powered up using a 12 V bias for VDD, a high−voltage DC source for VIN and an electronic load for VOUT. The test board was operated at 380 VIN, 400 VIN and 12.5 VOUT, with output currents of 2 A, 5 A, 10 A, 15 A and 20 A. No EVB heatsink was needed for this test, as the input RMS currents were less than 2 A for all output conditions. The 380 VIN, 12.5 V, 20 A out waveform measurements are shown in Figure 17. The 400 V, 12.5 V, 20 A out waveform measurements are shown in Figure 18. A thermal image of the EVB running at 400 VIN, 12.5 V at 20 A out, is shown Figure 19.

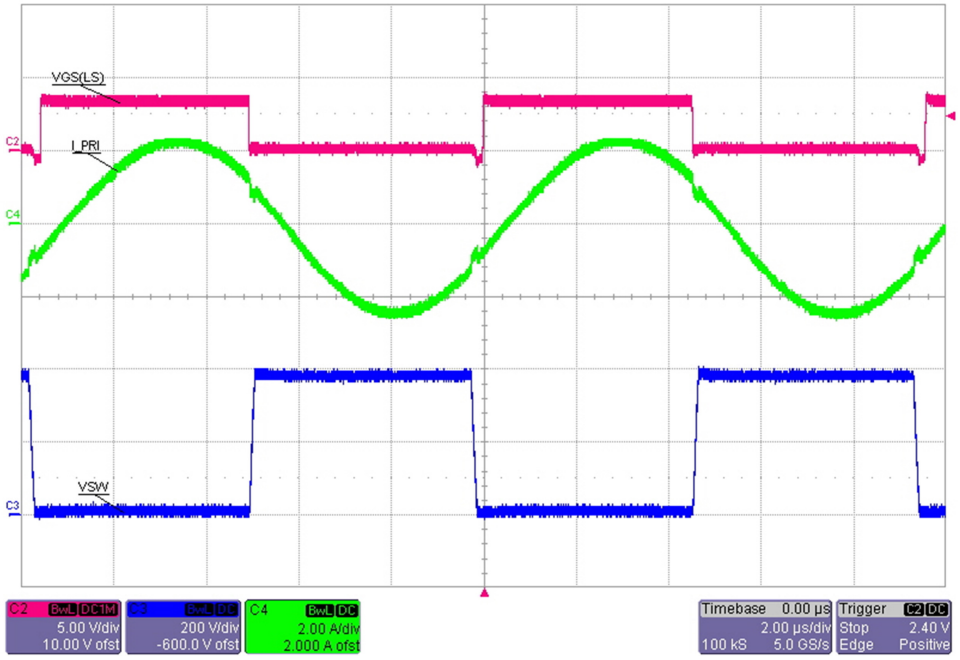


Figure 17. FAN7688 LLC/NCP51820 HB GaN Driver EVB, 380 VIN, 100 kHz, 12.5 V, 20 A

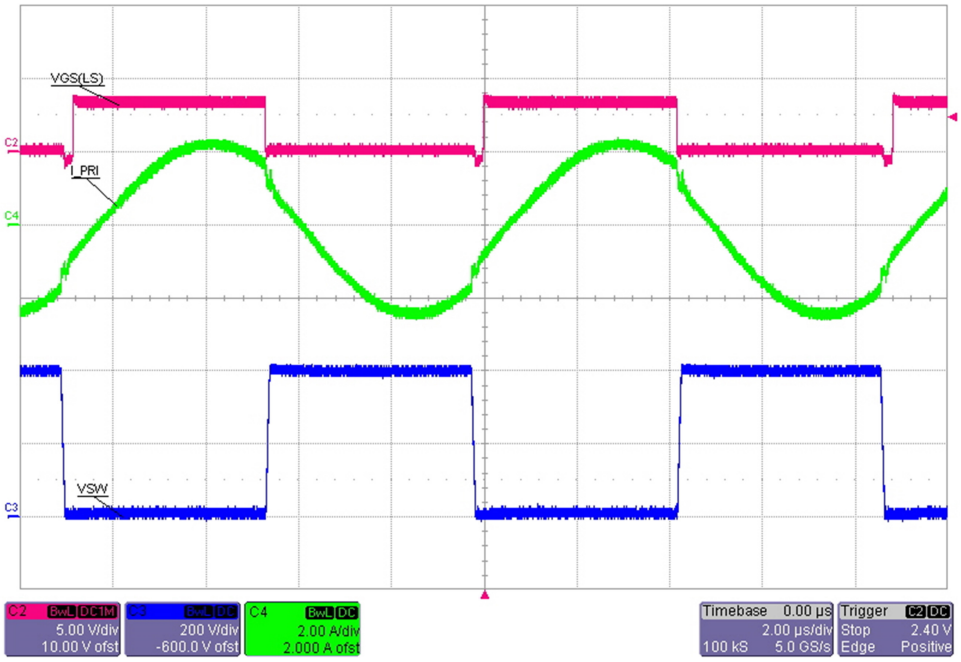


Figure 18. FAN7688 LLC/NCP51820 HB GaN Driver EVB, 400 VIN, 100 kHz, 12.5 V, 20 A

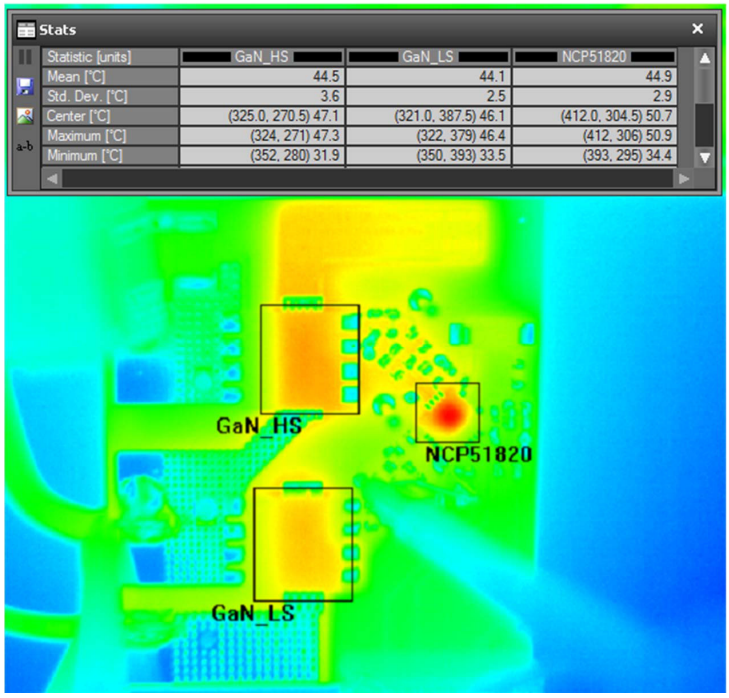


Figure 19. Thermal Image: FAN7688 LLC/NCP51820 HB GaN Driver EVB, 400 VIN, 100 kHz, 12.5 V, 20 A

Figure 19 shows a thermal image of EVB operating at 400 V in, 100 kHz, 12.5 V, 20 A out. This test was performed without an EVB heatsink, and in still air. In this test condition, the HS and LS GaN power switches, as well as the NCP51820 driver do not exceed 40°C.

CONCLUSION

When using this EVB with an existing silicon (Si) half−bridge power stage at normal Si frequencies (40−500 kHz), the true benefits of GaN technology (higher running frequencies, smaller magnetics, higher power density) will not be realized at the lower frequencies that Si typically operates. The goal of this EVB is to easily enable the evaluation of the NCP51820 GaN driver, mating it with existing half−bridge power topologies, and not to significantly change their operation or efficiency. This EVB can be run at high frequencies, but care must be applied to both the input signals and the power connections to be as short as possible to avoid noise injection and ringing. More information on GaN driver PCB design and layout techniques are available at ON Semiconductor/NCP51820.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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