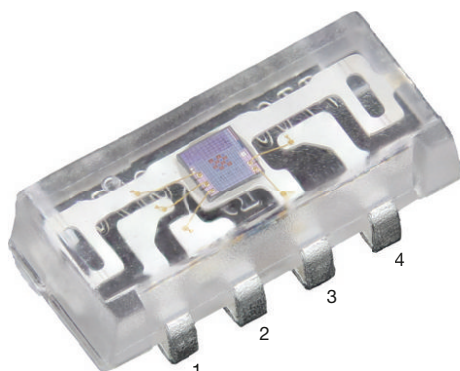


# High Accuracy Ambient Light Sensor With I<sup>2</sup>C Interface



## Pinning

- 1: SCL
- 2: V<sub>DD</sub>
- 3: GND
- 4: SDA

## DESCRIPTION

VEML7700 is a high accuracy ambient light digital 16-bit resolution sensor in a miniature transparent 6.8 mm x 2.35 mm x 3.0 mm package. It includes a high sensitive photo diode, a low noise amplifier, a 16-bit A/D converter and supports an easy to use I<sup>2</sup>C bus communication interface.

The ambient light result is as digital value available.

## FEATURES

- Package type: surface-mount
- Package: side view
- Dimensions (L x W x H in mm): 6.8 x 2.35 x 3.0
- Integrated modules: ambient light sensor (ALS)
- Supply voltage range V<sub>DD</sub>: 2.5 V to 3.6 V
- Communication via I<sup>2</sup>C interface
- Floor life: 72 h, MSL 4, according to J-STD-020
- Low shut down current consumption: typ. 0.5 µA
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



## AMBIENT LIGHT FUNCTION

- 16-bit dynamic range for ambient light detection from 0 lx to about 140 klx with resolution down to 0.0042 lx/ct, supports low transmittance (dark) lens design
- 100 Hz and 120 Hz flicker noise rejection
- Excellent temperature compensation
- High dynamic detection resolution
- Software shutdown mode control

## APPLICATIONS

- Ambient light sensor for backlight dimming of e.g. TV displays, smart phones, touch phones, PDA, GPS
- Ambient light sensor for industrial on- / off-lighting operation
- Optical switch for consumer, computing, and industrial devices and displays

## PRODUCT SUMMARY

| PART NUMBER | OPERATING VOLTAGE RANGE (V) | I <sup>2</sup> C BUS VOLTAGE RANGE (V) | AMBIENT LIGHT RANGE (lx) | AMBIENT LIGHT RESOLUTION (lx) | OUTPUT CODE              | ADC RESOLUTION PROXIMITY / AMBIENT LIGHT |
|-------------|-----------------------------|----------------------------------------|--------------------------|-------------------------------|--------------------------|------------------------------------------|
| VEML7700    | 2.5 to 3.6                  | 1.7 to 3.6                             | 0 to 140 000             | 0.0042                        | 16 bit, I <sup>2</sup> C | - / 0.0042                               |

## ORDERING INFORMATION

| ORDERING CODE | PACKAGING     | VOLUME <sup>(1)</sup>       | REMARKS   |
|---------------|---------------|-----------------------------|-----------|
| VEML7700-TR   | Tape and reel | MOQ: 2300 (MOQ is one reel) | Side view |
| VEML7700-TT   | Tape and reel | MOQ: 2200 (MOQ is one reel) | Top view  |

## Note

- <sup>(1)</sup> MOQ: minimum order quantity

| <b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified) |                                           |           |      |      |                    |
|--------------------------------------------------------------------------------------------------------|-------------------------------------------|-----------|------|------|--------------------|
| PARAMETER                                                                                              | TEST CONDITION                            | SYMBOL    | MIN. | MAX. | UNIT               |
| Supply voltage                                                                                         |                                           | $V_{DD}$  | 0    | 4    | V                  |
| Operation temperature range                                                                            |                                           | $T_{amb}$ | -25  | +85  | $^{\circ}\text{C}$ |
| Storage temperature range                                                                              |                                           | $T_{stg}$ | -25  | +85  | $^{\circ}\text{C}$ |
| Total power dissipation                                                                                | $T_{amb} \leq 25\text{ }^{\circ}\text{C}$ | $P_{tot}$ | -    | 50   | mW                 |
| Junction temperature                                                                                   |                                           | $T_j$     | -    | 100  | $^{\circ}\text{C}$ |

| <b>BASIC CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified) |                                                    |                     |      |         |      |               |
|-----------------------------------------------------------------------------------------------------|----------------------------------------------------|---------------------|------|---------|------|---------------|
| PARAMETER                                                                                           | TEST CONDITION                                     | SYMBOL              | MIN. | TYP.    | MAX. | UNIT          |
| Supply voltage                                                                                      |                                                    | $V_{DD}$            | 2.5  | 3.3     | 3.6  | V             |
| Shut down current <sup>(2)</sup>                                                                    | $V_{DD}$ is 3.3 V                                  | $I_{sd}$            | -    | 0.5     | -    | $\mu\text{A}$ |
| Operation mode current <sup>(1)</sup>                                                               | $V_{DD}$ is 3.3 V, PSM = 11, refresh time 4100 ms  | $I_{DD}$            | -    | 2       | -    | $\mu\text{A}$ |
|                                                                                                     | $V_{DD}$ is 3.3 V, PSM = 00, refresh time 600 ms   | $I_{DD}$            | -    | 8       | -    | $\mu\text{A}$ |
|                                                                                                     | $V_{DD}$ is 3.3 V, PSM_EN = 0, refresh time 100 ms | $I_{DD}$            | -    | 45      | -    | $\mu\text{A}$ |
| I <sup>2</sup> C clock rate range                                                                   |                                                    | $f_{SCL}$           | 10   | -       | 400  | kHz           |
| I <sup>2</sup> C bus input H-level range                                                            | $V_{DD}$ is 3.3 V                                  | $V_{ih}$            | 1.3  | -       | 3.6  | V             |
| I <sup>2</sup> C bus input L-level range                                                            | $V_{DD}$ is 3.3 V                                  | $V_{il}$            | -0.3 | -       | 0.4  | V             |
| Digital current out (low, current sink)                                                             |                                                    | $I_{ol}$            | 3    | -       | -    | mA            |
| Digital resolution (LSB count) <sup>(3)</sup>                                                       | With ALS_GAIN = x 2, ALS_IT = 800 ms               |                     | -    | 0.0042  | -    | lx/step       |
| Detectable maximum illuminance <sup>(3)</sup>                                                       | With ALS_GAIN = x 1/8, ALS_IT = 25 ms              | $E_{V\text{ max.}}$ | -    | 140 000 | -    | lx            |
| Dark offset <sup>(2)</sup>                                                                          | With ALS_GAIN = x 2, ALS_IT = 800 ms               |                     | -    | 3       | -    | step          |

**Notes**

- (1) Light source: white LED  
(2) Light conditions: dark  
(3) Refer to the application note for resolution table at different settings

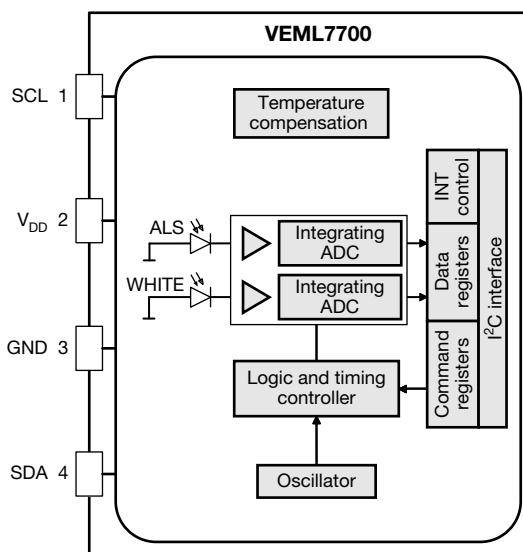
**CIRCUIT BLOCK DIAGRAM**


Fig. 1 - Block Diagram

| <b>I<sup>2</sup>C TIMING CHARACTERISTICS</b> ( $T_{amb} = 25^{\circ}\text{C}$ , unless otherwise specified) |                 |                              |      |                          |      |               |
|-------------------------------------------------------------------------------------------------------------|-----------------|------------------------------|------|--------------------------|------|---------------|
| PARAMETER                                                                                                   | SYMBOL          | STANDARD MODE <sup>(1)</sup> |      | FAST MODE <sup>(1)</sup> |      | UNIT          |
|                                                                                                             |                 | MIN.                         | MAX. | MIN.                     | MAX. |               |
| Clock frequency                                                                                             | $f_{(SMBCLK)}$  | 10                           | 100  | 10                       | 400  | kHz           |
| Bus free time between start and stop condition                                                              | $t_{(BUF)}$     | 4.7                          | -    | 1.3                      | -    | $\mu\text{s}$ |
| Hold time after (repeated) start condition; after this period, the first clock is generated                 | $t_{(HDSTA)}$   | 4.0                          | -    | 0.6                      | -    | $\mu\text{s}$ |
| Repeated start condition setup time                                                                         | $t_{(SUSTA)}$   | 4.7                          | -    | 0.6                      | -    | $\mu\text{s}$ |
| Stop condition setup time                                                                                   | $t_{(SUSTO)}$   | 4.0                          | -    | 0.6                      | -    | $\mu\text{s}$ |
| Data hold time                                                                                              | $t_{(HDDAT)}$   | 0                            | 3450 | 0                        | 900  | ns            |
| Data setup time                                                                                             | $t_{(SUDAT)}$   | 250                          | -    | 100                      | -    | ns            |
| I <sup>2</sup> C clock (SCK) low period                                                                     | $t_{(LOW)}$     | 4.7                          | -    | 1.3                      | -    | $\mu\text{s}$ |
| I <sup>2</sup> C clock (SCK) high period                                                                    | $t_{(HIGH)}$    | 4.0                          | -    | 0.6                      | -    | $\mu\text{s}$ |
| Detect clock / data low timeout                                                                             | $t_{(TIMEOUT)}$ | 25                           | 35   | -                        | -    | ms            |
| Clock / data fall time                                                                                      | $t_{(F)}$       | -                            | 300  | -                        | 300  | ns            |
| Clock / data rise time                                                                                      | $t_{(R)}$       | -                            | 1000 | -                        | 300  | ns            |

**Note**

(1) Data based on standard I<sup>2</sup>C protocol requirement, not tested in production

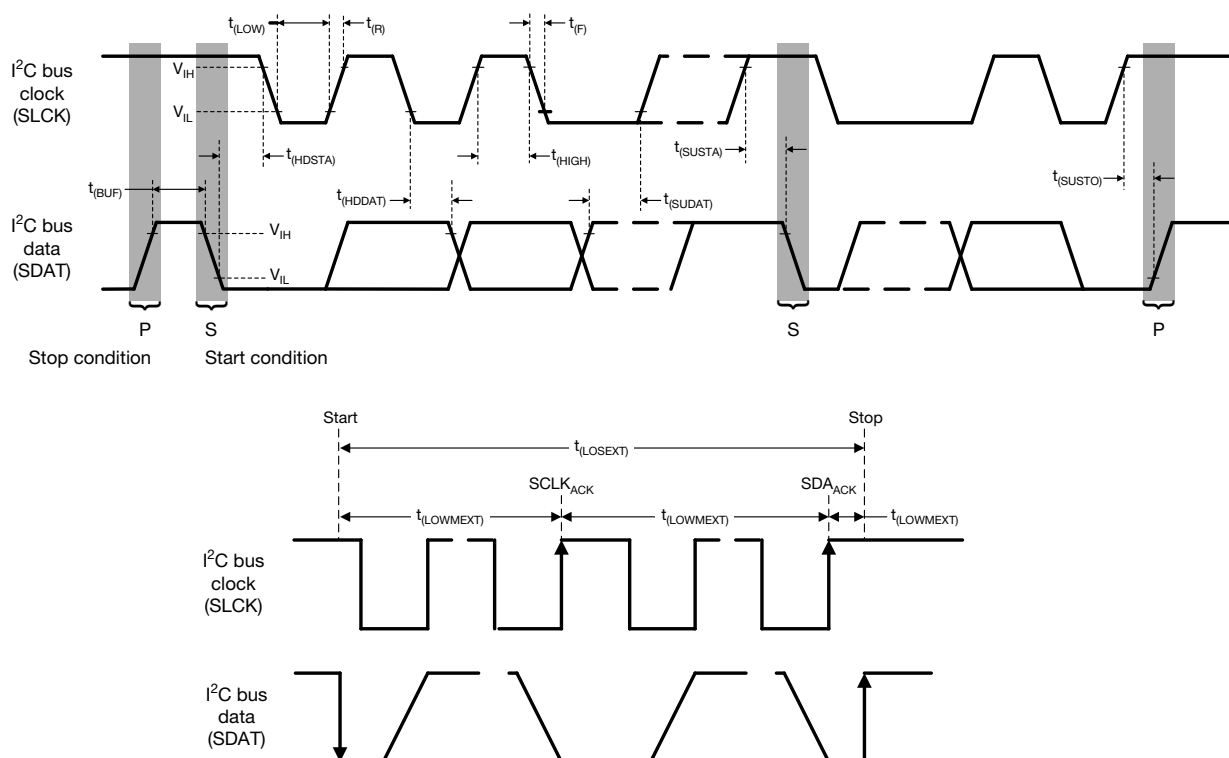


Fig. 2 - I<sup>2</sup>C Timing Diagram

## PARAMETER TIMING INFORMATION

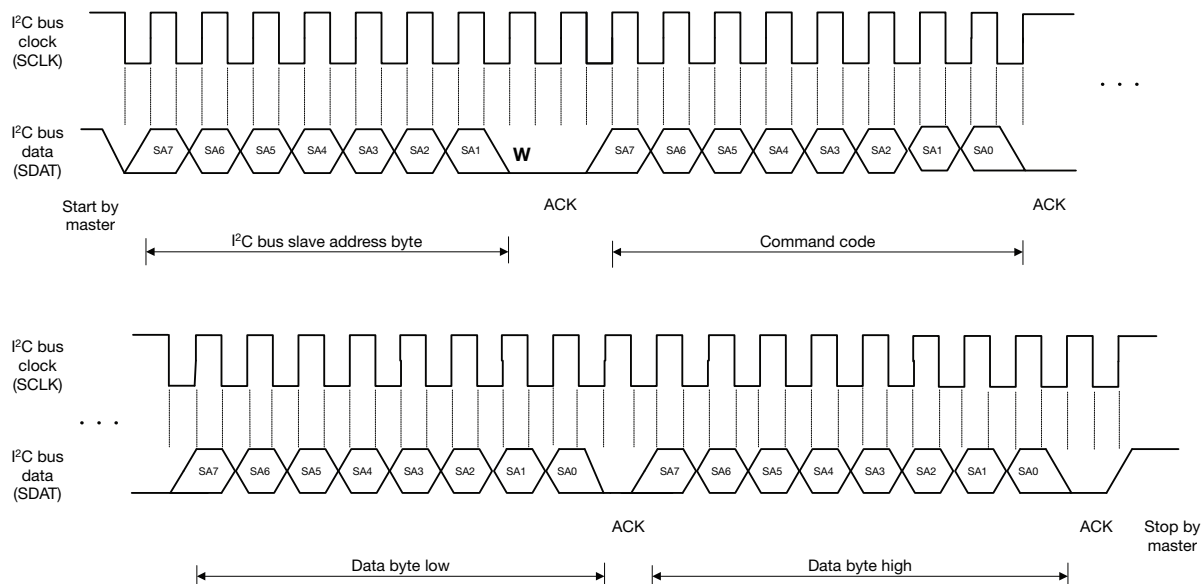


Fig. 3 - I<sup>2</sup>C Bus Timing for Sending Word Command Format

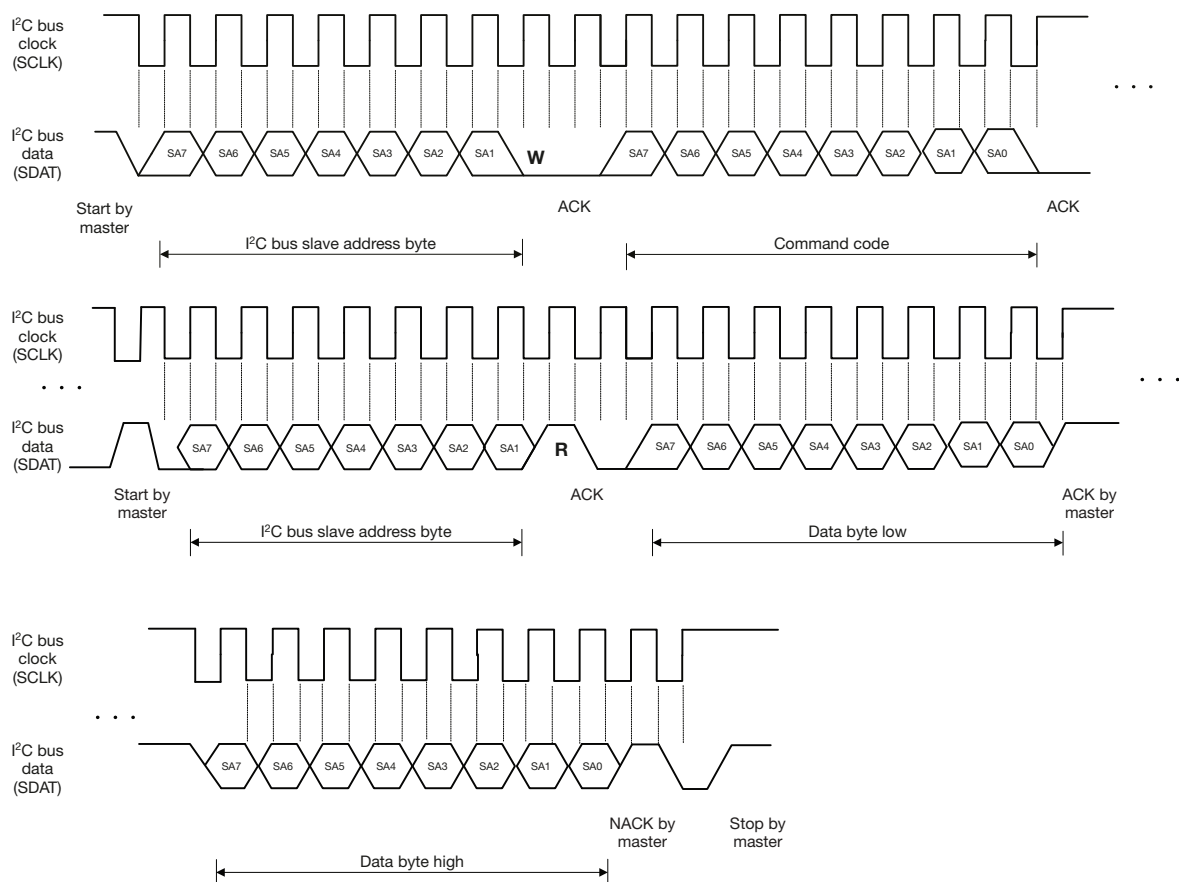
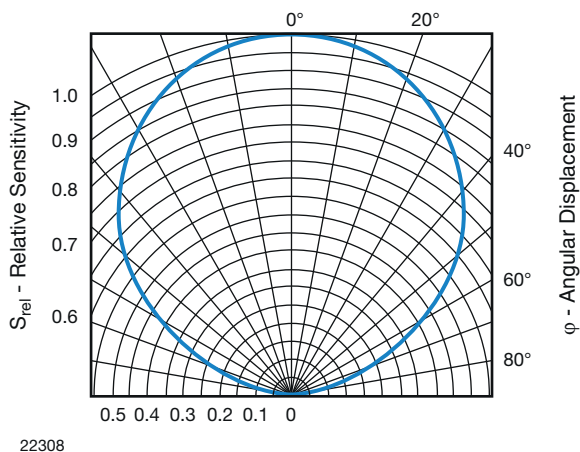
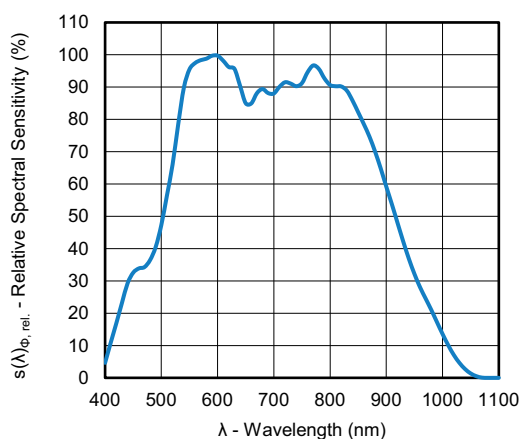
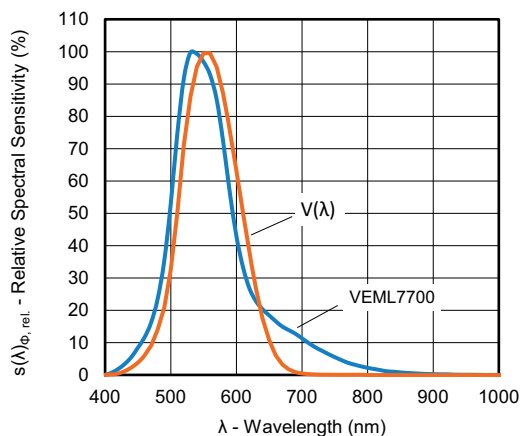


Fig. 4 - I<sup>2</sup>C Bus Timing for Receive Word Command Format

**BASIC CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)


## APPLICATION INFORMATION

VEML7700 is a cost effective solution of ambient light sensor with I<sup>2</sup>C bus interface. The standard serial digital interface is easy to access “Ambient Light Signal” without complex calculation and programming by external controller.

### 1. Application Circuit

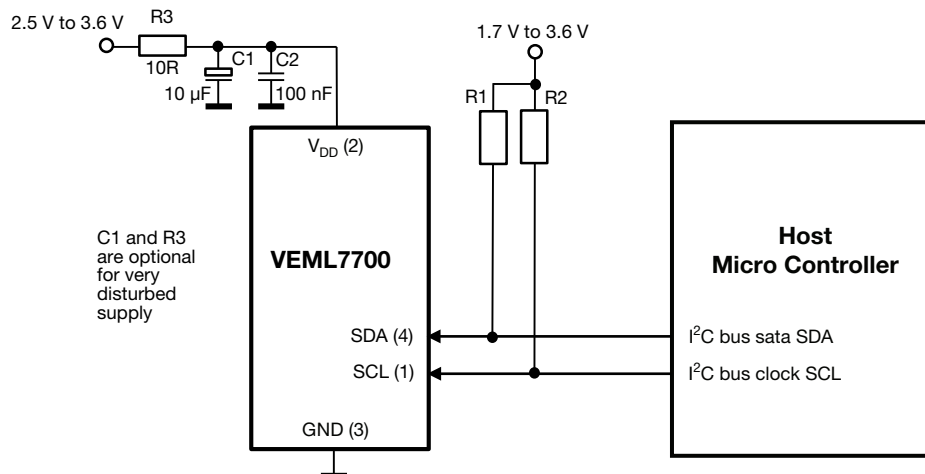


Fig. 8 - Application Diagram

#### Notes

- Proposed values for the pull-up resistor R1 and R2 should be > 1 kΩ, e.g. 2.2 kΩ to 4.7 kΩ.
- For detailed description about set-up and use as well as more application related information see AN: “Designing VEML7700 into an Application”

### 2. I<sup>2</sup>C Interface

The VEML7700 contains actual six 16 bit command codes for operation control, parameter setup, and result buffering. All registers are accessible via I<sup>2</sup>C communication. Fig. 10 shows the basic I<sup>2</sup>C communication with VEML7700.

The built in I<sup>2</sup>C interface is compatible with I<sup>2</sup>C modes “standard” and “fast”: 10 kHz to 400 kHz.

I<sup>2</sup>C H-level range = 1.3 V to 3.6 V.

Please refer to the I<sup>2</sup>C specification from NXP for details.

Send byte Write command to VEML7700

|   |               |    |   |              |   |                 |   |                 |   |   |
|---|---------------|----|---|--------------|---|-----------------|---|-----------------|---|---|
| S | Slave address | Wr | A | Command code | A | Data byte (LSB) | A | Data byte (MSB) | A | P |
|---|---------------|----|---|--------------|---|-----------------|---|-----------------|---|---|

Receive byte Read data from VEML7700

|   |               |    |   |              |   |   |               |    |   |                 |   |                 |   |   |
|---|---------------|----|---|--------------|---|---|---------------|----|---|-----------------|---|-----------------|---|---|
| S | Slave address | Wr | A | Command code | A | S | Slave address | Rd | A | Data byte (LSB) | A | Data byte (MSB) | N | P |
|---|---------------|----|---|--------------|---|---|---------------|----|---|-----------------|---|-----------------|---|---|

S = start condition  
P = stop condition  
A = acknowledge  
N = no acknowledge

☐ Host action  
☒ VEML7700 response

Fig. 9 - Send Byte / Receive Byte Protocol

#### Register Addresses

VEML7700 has actual six user accessible 16 bit command codes.

The addresses are 00h to 06h (03h not defined / reserved).

#### Device Address

The VEML7700 has a fix slave address for the host programming and accessing selection.

The slave address (7 bit) is set to 0010000 = 0x10.

The least significant bit (LSB) defines read or write mode.

According 8 bit the bus address is then 0010 0000 = 20h for write and 0010 0001 = 21h for read.

#### Auto-Memorization

VEML7700 can memorize the last ambient data before shutdown and keep this data before waking up.

When VEML7700 is in shutdown mode, the host can freely read this data via read command directly.

When VEML7700 wakes up, the data will be refreshed by new detection.



Interrupt pin not available for VEML7700

| COMMAND REGISTER FORMAT |               |        |                                                     |       |
|-------------------------|---------------|--------|-----------------------------------------------------|-------|
| COMMAND CODE            | REGISTER NAME | BIT    | FUNCTION / DESCRIPTION                              | R / W |
| 00                      | ALS_CONF_0    | 15 : 0 | ALS gain, integration time, interrupt, and shutdown | R / W |
| 01                      | ALS_WH        | 15 : 8 | ALS high threshold window setting (MSB)             | R / W |
|                         |               | 7 : 0  | ALS high threshold window setting (LSB)             | R / W |
| 02                      | ALS_WL        | 15 : 8 | ALS low threshold window setting (MSB)              | R / W |
|                         |               | 7 : 0  | ALS low threshold window setting (LSB)              | R / W |
| 03                      | Power saving  | 15 : 0 | Set (15 : 3) 0000 0000 0000 0b                      | R / W |
| 04                      | ALS           | 15 : 8 | MSB 8 bits data of whole ALS 16 bits                | R     |
|                         |               | 7 : 0  | LSB 8 bits data of whole ALS 16 bits                | R     |
| 05                      | WHITE         | 15 : 8 | MSB 8 bits data of whole WHITE 16 bits              | R     |
|                         |               | 7 : 0  | LSB 8 bits data of whole WHITE 16 bits              | R     |
| 06                      | ALS_INT       | 15 : 0 | ALS INT trigger event                               | R     |
| 07                      | ID            | 15 : 0 | Device ID                                           | R     |

**Note**

- Command code 0 default value is 01 = devices is shut down

**Command Code #0: Configuration Register**

Register address = 00h

The command code #0 is for configuration of the ambient light measurements.

| TABLE 1 - CONFIGURATION REGISTER #0 |         |                                                                                                                                  |       |
|-------------------------------------|---------|----------------------------------------------------------------------------------------------------------------------------------|-------|
| REGISTER NAME                       | BIT     | FUNCTION / DESCRIPTION                                                                                                           | R / W |
| Reserved                            | 15 : 13 | Set 000b                                                                                                                         | R / W |
| ALS_GAIN                            | 12 : 11 | Gain selection<br>00 = ALS gain x 1<br>01 = ALS gain x 2<br>10 = ALS gain x (1/8)<br>11 = ALS gain x (1/4)                       | R / W |
| reserved                            | 10      | Set 0b                                                                                                                           | R / W |
| ALS_IT                              | 9 : 6   | ALS integration time setting<br>1100 = 25 ms<br>1000 = 50 ms<br>0000 = 100 ms<br>0001 = 200 ms<br>0010 = 400 ms<br>0011 = 800 ms | R / W |
| ALS_PERS                            | 5 : 4   | ALS persistence protect number setting<br>00 = 1<br>01 = 2<br>10 = 4<br>11 = 8                                                   | R / W |
| Reserved                            | 3 : 2   | Set 00b                                                                                                                          | R / W |
| ALS_INT_EN                          | 1       | ALS interrupt enable setting<br>0 = ALS INT disable<br>1 = ALS INT enable                                                        | R / W |
| ALS_SD                              | 0       | ALS shut down setting<br>0 = ALS power on<br>1 = ALS shut down                                                                   | R / W |

**Note**

- Light level [lx] is (ALS OUTPUT DATA [dec.] / ALS Gain x responsivity). Please study also the application note

**Command Code #1: High Threshold Windows Setting**

Command code address = 01h. Once enable INT function and use high / low windows threshold, bit 15:0 provides 16 bit register for high bound threshold windows setting.

| TABLE 2 - HIGH THRESHOLD WINDOWS SETTING #1                          |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|----------------------------------------------------------------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15                                                               | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Description                                                          |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| ALS high threshold window setting (15:8 MSB 8 bits of whole 16 bits) |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| ALS high threshold window setting (7:0 LSB 8 bits of whole 16 bits)  |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |

**Command Code #2: Low Threshold Windows Setting**

Command code address = 02h. Once enable INT function and use high / low windows threshold, bit 15:0 provides 16 bit register for low bound threshold windows setting.

| TABLE 3 - LOW THRESHOLD WINDOWS SETTING #2                          |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|---------------------------------------------------------------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15                                                              | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Description                                                         |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| ALS low threshold window setting (15:8 MSB 8 bits of whole 16 bits) |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| ALS low threshold window setting (7:0 LSB 8 bits of whole 16 bits)  |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |

**Command Code #3: Power Saving Mode: PSM**

Command code address = 03h. Bits 2 and 1 define the power saving modes. Bits 15 : 3 are reserved.

| TABLE 4 - POWER SAVING MODES |       |                                                                                                         |       |
|------------------------------|-------|---------------------------------------------------------------------------------------------------------|-------|
| REGISTER NAME                | BIT   | FUNCTION / DESCRIPTION                                                                                  | R / W |
| PSM                          | 2 : 1 | Power saving mode; see table "Refresh time"<br>00 = mode 1<br>01 = mode 2<br>10 = mode 3<br>11 = mode 4 | R / W |
| PSM_EN                       | 0     | Power saving mode enable setting<br>0 = disable<br>1 = enable                                           | R / W |

**Command Code #4: ALS High Resolution Output Data**

Command code address = 04h. To access 16 bit high resolution ALS output, it is suitable to follow read protocol to read from command code 04 16 bits register.

| TABLE 5 - ALS HIGH RESOLUTION OUTPUT DATA #4                         |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|----------------------------------------------------------------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15                                                               | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Description                                                          |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| ALS high resolution output data (15 : 8 MSB 8 bits of whole 16 bits) |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| ALS high resolution output data (7 : 0 LSB 8 bits of whole 16 bits)  |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |

**Command Code #5: White Channel Output Data**

Command code address = 05h. To access 16 bit WHITE output, it is suitable to follow read protocol to read from command code 05 16 bits register.

| TABLE 6 - WHITE CHANNEL OUTPUT DATA #5                 |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|--------------------------------------------------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15                                                 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Description                                            |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| WHITE output data (15 : 8 MSB 8 bits of whole 16 bits) |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| WHITE output data (7 : 0 LSB 8 bits of whole 16 bits)  |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |



**Command Code #6: Interrupt Status**

Command code address = 06h. Bit 15 defines interrupt flag while trigger occurred due to data crossing low threshold windows. Bit 14 defines interrupt flag while trigger occurred due to data crossing high threshold windows.

| TABLE 7 - INTERRUPT STATUS #6 |                                          |             |
|-------------------------------|------------------------------------------|-------------|
| Bit 15                        | Bit 14                                   | Bit 13 to 0 |
| int_th_low                    | int_th_high                              | reserved    |
| Description                   |                                          |             |
| int_th_low                    | R bit. Indicated a low threshold exceed  |             |
| int_th_high                   | R bit. Indicated a high threshold exceed |             |

**Command Code #7: ID Register**

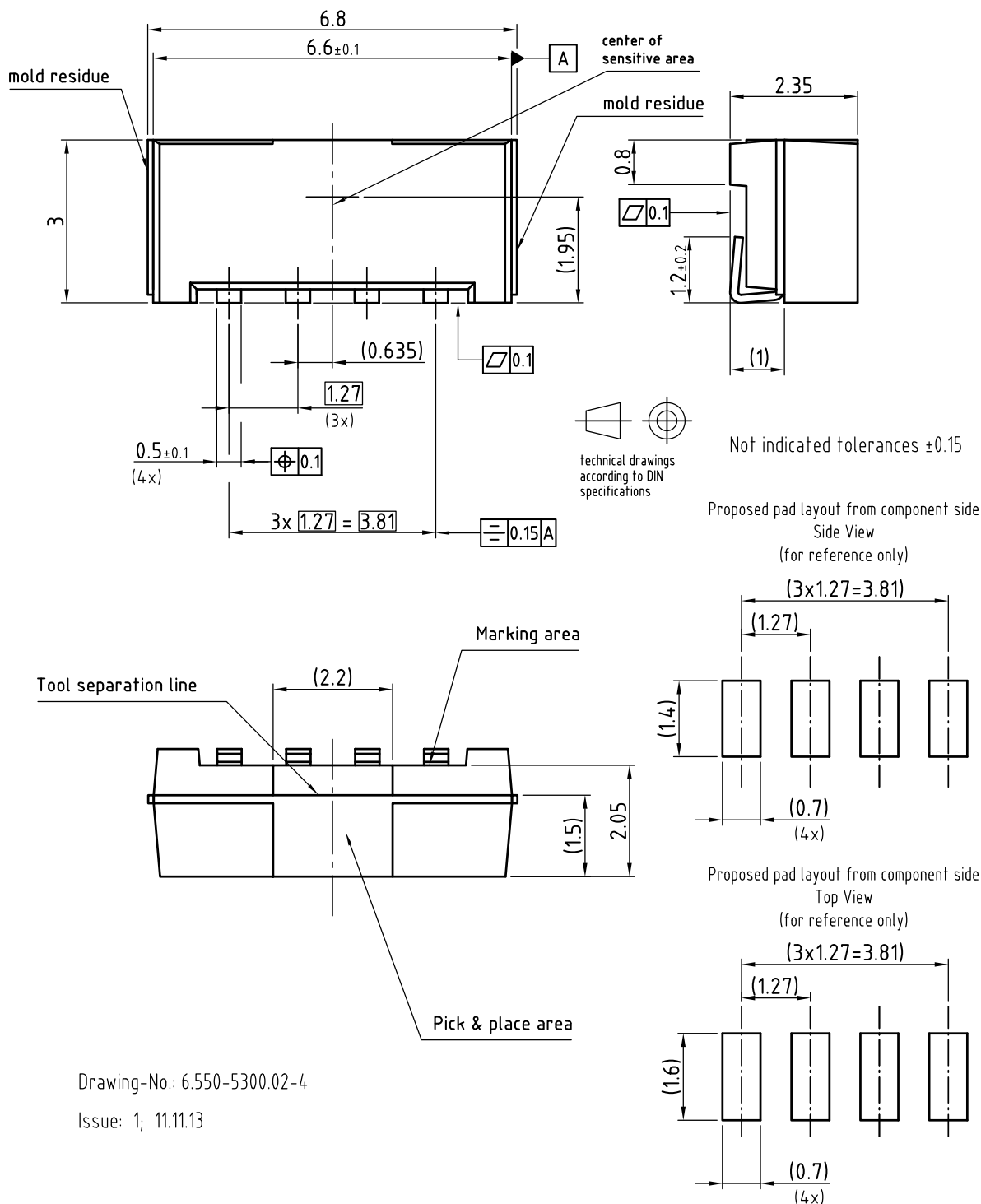
Command code address = 07h. The low byte of the ID register contains the device specific ID code 81h. The high byte contains a code that depends on the chosen slave address option: either 0xC4 for a device with slave address 0x20, or 0xD4 for a device with slave address 0x90

| TABLE 8 - DEVICE ID #7    |                                                                                                                               |
|---------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| Bit 15 to 8               | Bit 7 to 0                                                                                                                    |
| Slave address option code | Device ID code                                                                                                                |
| Description               |                                                                                                                               |
| Slave address option code | Slave address specific ID<br>For slave address option 0x20: 11000100 = 0xC4<br>For slave address option 0x90: 11010100 = 0xD4 |
| Device ID code            | Fixed device ID: 10000001 = 0x81                                                                                              |

**REFRESH TIME DETERMINATION OF PSM**

VEML7700's refresh time can be determined by PSM and ALS\_IT setting in power saving mode (PSM). Cooperating with the command register setting, the designer has a flexible method in defining the timing, power consumption, and sensitivity for light data collection.

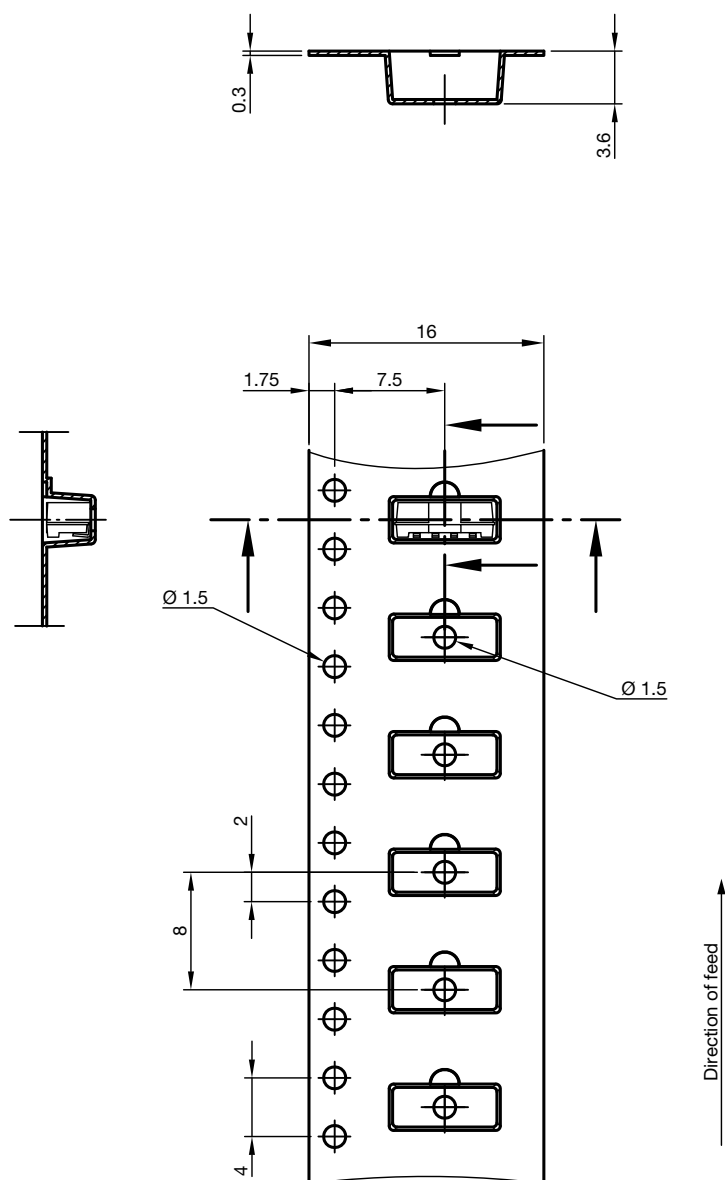
| REFRESH TIME, I <sub>DD</sub> , AND RESOLUTION RELATION |        |             |                   |                      |                     |
|---------------------------------------------------------|--------|-------------|-------------------|----------------------|---------------------|
| ALS_GAIN                                                | PSM    | ALS_IT (ms) | REFRESH TIME (ms) | I <sub>DD</sub> (μA) | RESOLUTION (lx/bit) |
| x2                                                      | Mode 1 | 100         | 600               | 8                    | 0.0336              |
| x2                                                      | Mode 2 | 100         | 1100              | 5                    | 0.0336              |
| x2                                                      | Mode 3 | 100         | 2100              | 3                    | 0.0336              |
| x2                                                      | Mode 4 | 100         | 4100              | 2                    | 0.0336              |
| x2                                                      | Mode 1 | 200         | 700               | 13                   | 0.0168              |
| x2                                                      | Mode 2 | 200         | 1200              | 8                    | 0.0168              |
| x2                                                      | Mode 3 | 200         | 2200              | 5                    | 0.0168              |
| x2                                                      | Mode 4 | 200         | 4200              | 3                    | 0.0168              |
| x2                                                      | Mode 1 | 400         | 900               | 20                   | 0.0084              |
| x2                                                      | Mode 2 | 400         | 1400              | 13                   | 0.0084              |
| x2                                                      | Mode 3 | 400         | 2400              | 8                    | 0.0084              |
| x2                                                      | Mode 4 | 400         | 4400              | 5                    | 0.0084              |
| x2                                                      | Mode 1 | 800         | 1300              | 28                   | 0.0042              |
| x2                                                      | Mode 2 | 800         | 1800              | 20                   | 0.0042              |
| x2                                                      | Mode 3 | 800         | 2800              | 13                   | 0.0042              |
| x2                                                      | Mode 4 | 800         | 4800              | 8                    | 0.0042              |

**PACKAGE DIMENSIONS** in millimeters


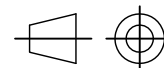
Drawing-No.: 6.550-5300.02-4

Issue: 1; 11.11.13

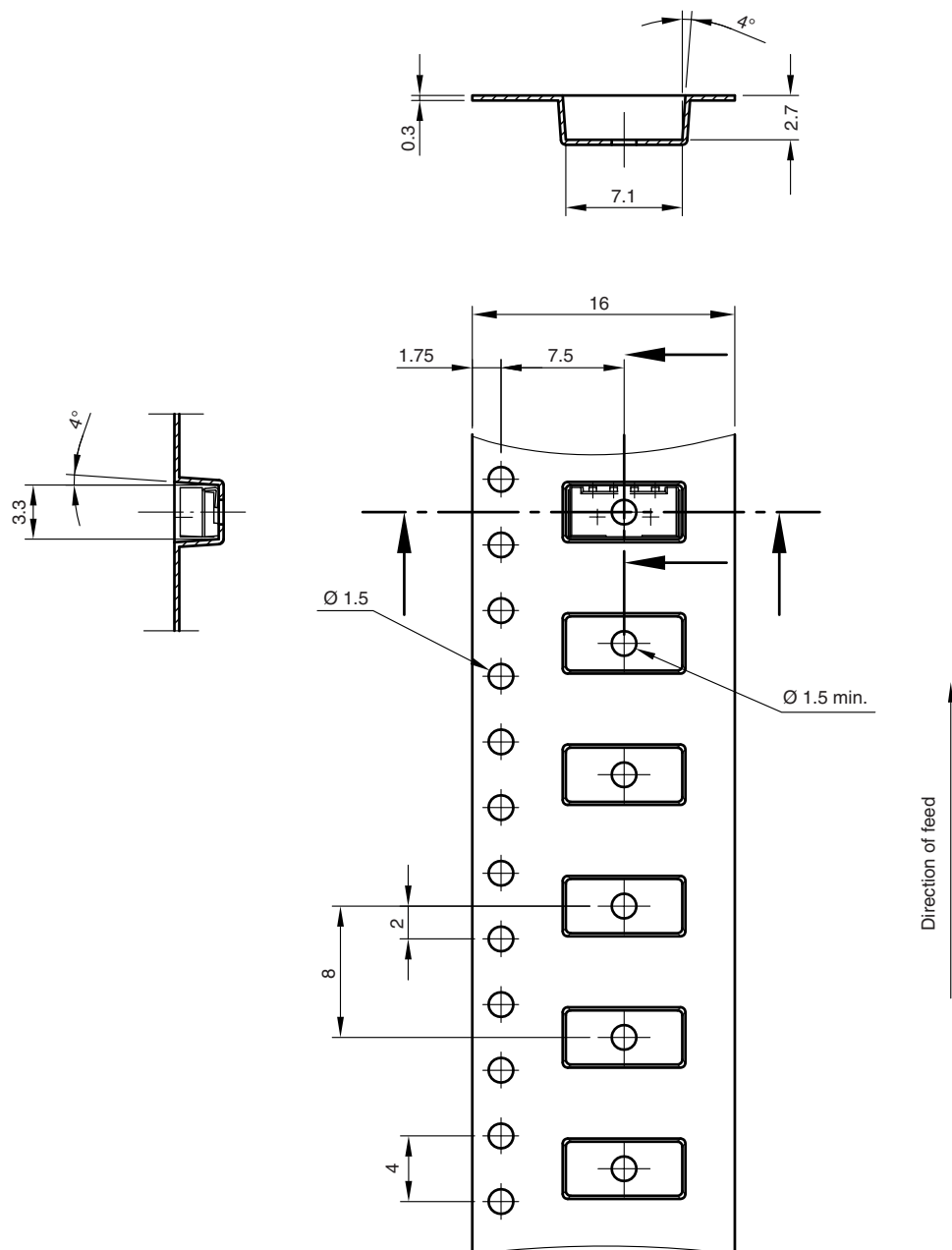
**TAPING SIDE VIEW (-TR VERSION)** in millimeters



Drawing-No.: 9.700-5342.01-4  
Issue: 2; 12.06.13



technical drawings  
according to DIN  
specifications

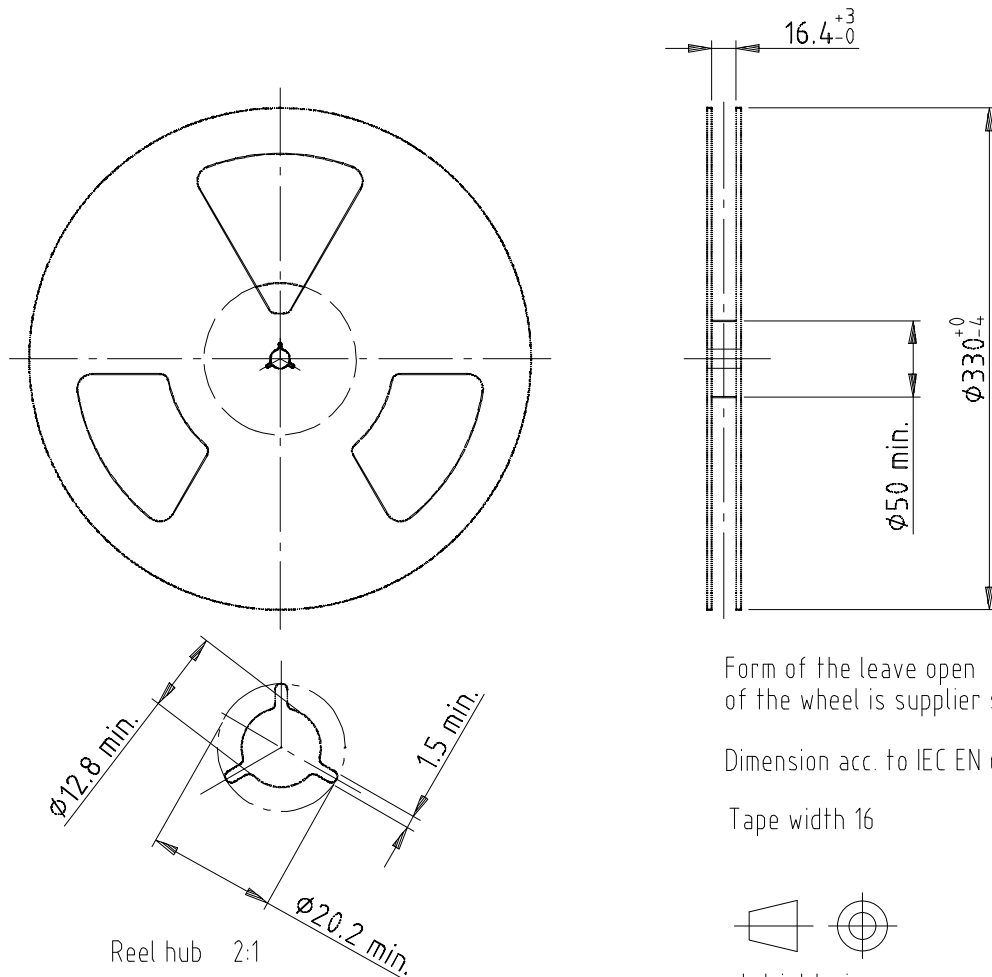
**TAPING TOP VIEW (-TT VERSION) in millimeters**


technical drawings  
according to DIN  
specifications

Drawing-No.: 9.700-5341.01-4

Issue: 2: 23.03.09

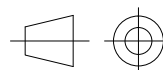
21666

**REEL DIMENSIONS** in millimeters


Form of the leave open of the wheel is supplier specific.

Dimension acc. to IEC EN 60 286-3

Tape width 16

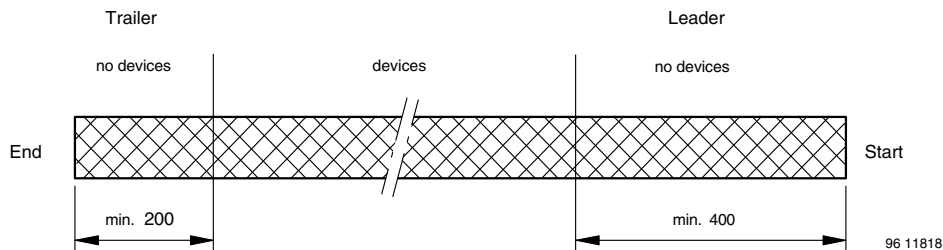


technical drawings according to DIN specifications

Drawing-No.: 9.800-5052.V2-4

Issue: 1; 07.05.02

16734

**LEADER AND TRAILER DIMENSIONS** in millimeters


## REFLOW SOLDER PROFILE

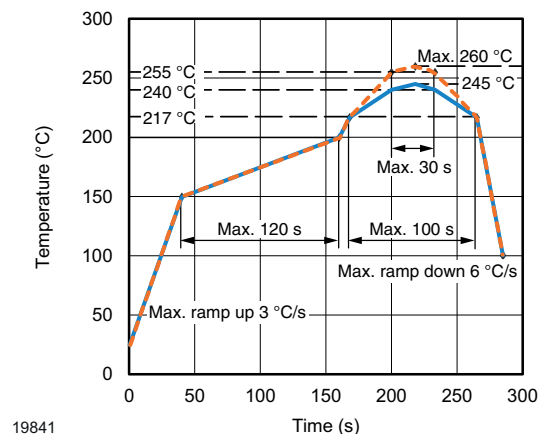


Fig. 10 - Lead (Pb)-free Reflow Solder Profile  
According to J-STD-020

## DRYPACK

Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.

## FLOOR LIFE

Floor life (time between soldering and removing from MBB) must not exceed the time indicated on MBB label:

Floor life: 72 h

Conditions:  $T_{amb} < 30\text{ °C}$ ,  $RH < 60\%$

Moisture sensitivity level 4, according to J-STD-020.

## DRYING

In case of moisture absorption devices should be baked before soldering. Conditions see J-STD-020 or label. Devices taped on reel dry using recommended conditions 192 h at  $40\text{ °C} (+ 5\text{ °C})$ ,  $RH < 5\%$ .



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