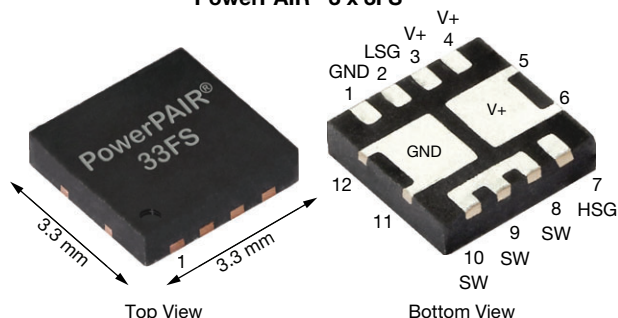


Dual N-Channel 30 V (D-S) MOSFET

PowerPAIR® 3 x 3FS


FEATURES

- TrenchFET® Gen V power MOSFET
- Symmetric dual N-channel
- Flip chip technology optimal thermal design
- High side and low side MOSFETs form optimized combination for 50 % duty cycle
- Optimized $R_{DS} - Q_g$ and $R_{DS} - Q_{gd}$ FOM elevates efficiency for high frequency switching
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

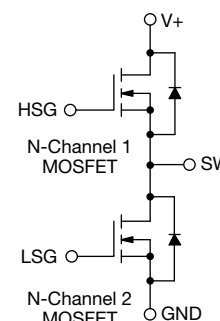

RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY

V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0032
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0053
Q_g typ. (nC)	6.7
I_D (A)	100 ^a
Configuration	Dual

APPLICATIONS

- Synchronous buck
- Computer / server peripherals
- Half bridge
- POL
- Telecom DC/DC



ORDERING INFORMATION

Package	PowerPAIR 3 x 3FS
Lead (Pb)-free and halogen-free	SiZF5302DT-T1-RE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	+16 / -12	V
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	100
		$T_C = 70$ °C	80
		$T_A = 25$ °C	28.1 ^{b, c}
		$T_A = 70$ °C	22.5 ^{b, c}
Pulsed drain current ($t = 100$ μ s)	I_{DM}	150	A
Continuous source current (MOSFET diode conduction)	I_S	$T_C = 25$ °C	40.1
		$T_A = 25$ °C	3.2 ^{b, c}
Single pulse avalanche current	I_{AS}	17	A
Single pulse avalanche energy	E_{AS}	14.45	mJ
Maximum power dissipation	P_D	$T_C = 25$ °C	48.1
		$T_C = 70$ °C	30.8
		$T_A = 25$ °C	3.8 ^{b, c}
		$T_A = 70$ °C	2.4 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature)		260	°C

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s

**THERMAL RESISTANCE RATINGS**

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	26	33	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	2	2.6	

Notes

a. Surface mounted on 1" x 1" FR4 board

b. Maximum under steady state conditions is 67 °C/W

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	30	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +16 V / -12 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55 °C	-	-	5	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	-	0.0027	0.0032	Ω
		V _{GS} = 4.5 V, I _D = 7 A	-	0.0044	0.0053	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 10 A	-	57	-	S
Dynamic ^b						
Input capacitance	C _{ISS}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	1030	-	pF
Output capacitance	C _{OSS}		-	340	-	
Reverse transfer capacitance	C _{RSS}		-	30	-	
C _{RSS} /C _{ISS} ratio			-	0.028	0.055	
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A	-	14.8	22.2	nC
			-	6.7	10.0	
Gate-source charge	Q _{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A	-	3.8	-	
Gate-drain charge	Q _{gd}		-	1.12	-	
Gate resistance	R _g	f = 1 MHz	0.24	1.2	2.4	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1 Ω, I _D ≅ 15 A, V _{GEN} = 10 V, R _g = 1 Ω	-	10	20	ns
Rise time	t _r		-	6	12	
Turn-off delay time	t _{d(off)}		-	23	46	
Fall time	t _f		-	6	12	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1 Ω, I _D ≅ 15 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	20	40	
Rise time	t _r		-	45	90	
Turn-off delay time	t _{d(off)}		-	20	40	
Fall time	t _f		-	12	24	
Drain-source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25°C	-	-	40.1	A
Pulse diode forward current	I _{SM}		-	-	150	
Body diode voltage	V _{SD}	I _S = 15 A, V _{GS} = 0 V	-	0.85	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 15 A, di/dt = 100 A/μs, T _J = 25 °C	-	13	26	ns
Body diode reverse recovery charge	Q _{rr}		-	3	6	nC
Reverse recovery fall time	t _a		-	6	-	ns
Reverse recovery rise time	t _b		-	7	-	

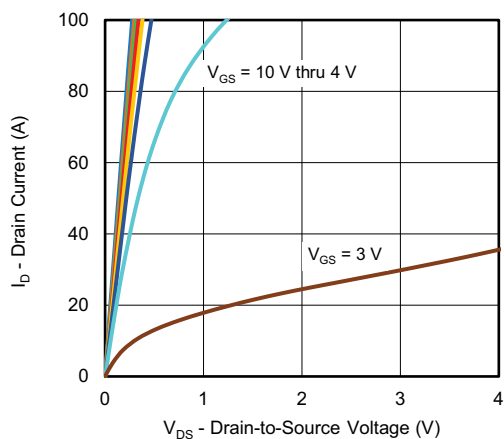
Notesa. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

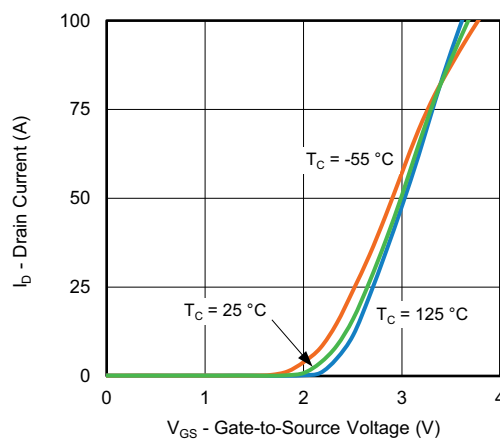
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



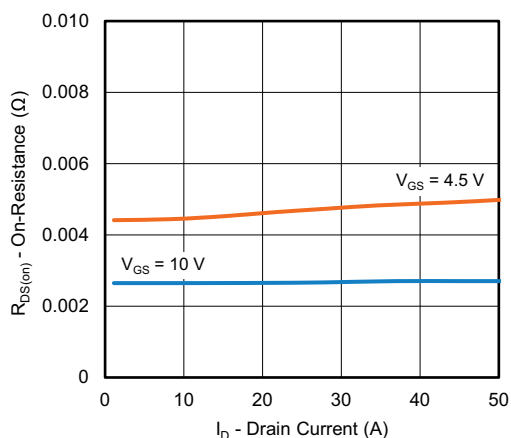
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



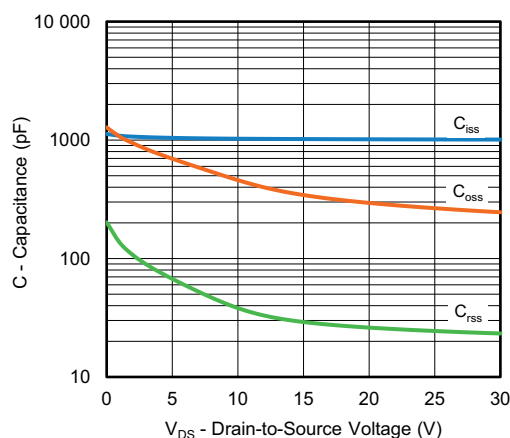
Output Characteristics



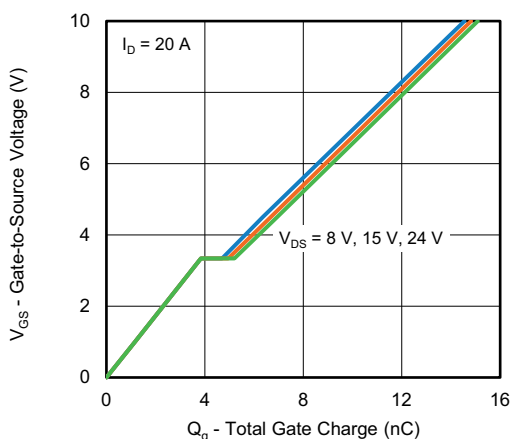
Transfer Characteristics



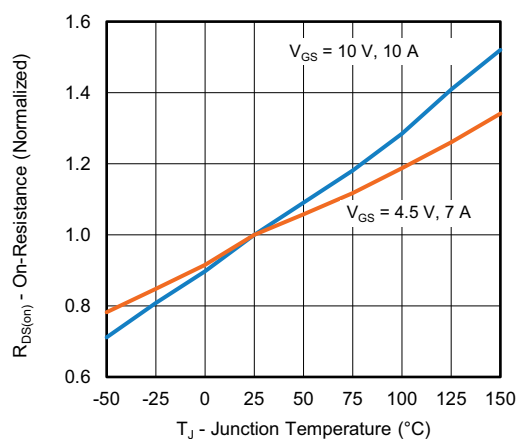
On-Resistance vs. Drain Current and Gate



Capacitance



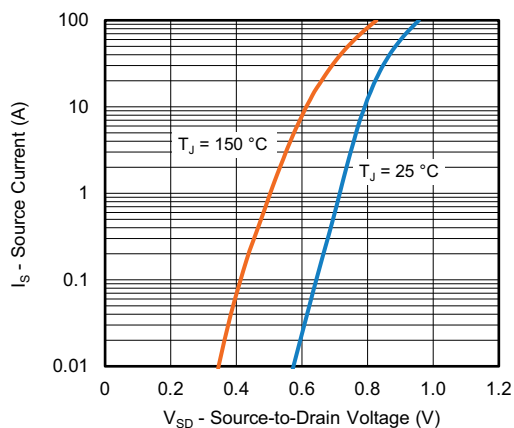
Gate Charge



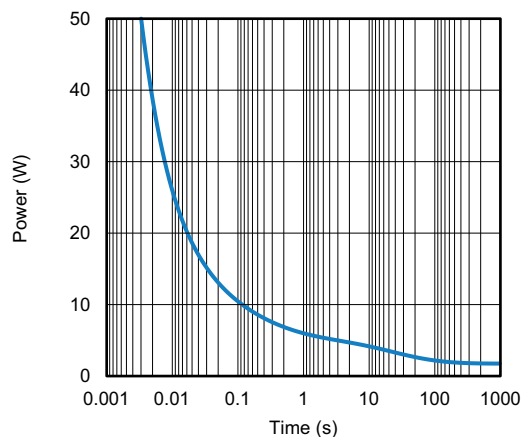
On-Resistance vs. Junction Temperature



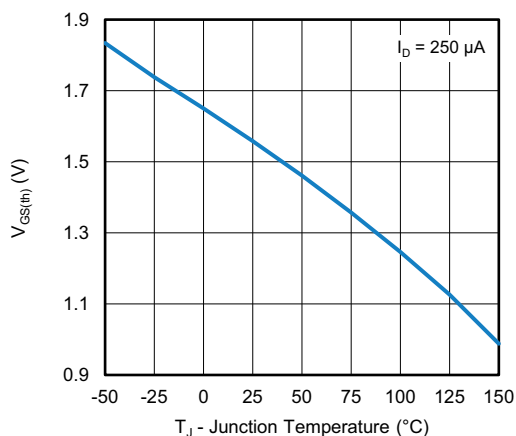
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



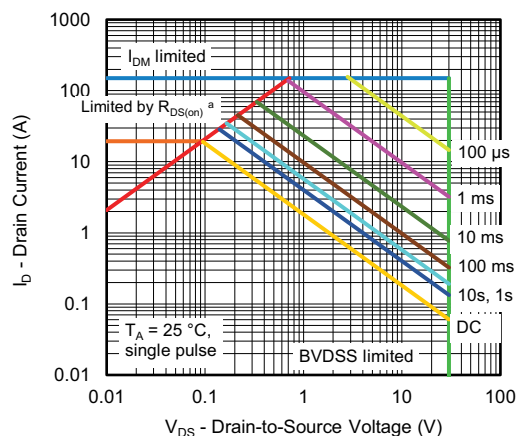
Source-Drain Diode Forward Voltage



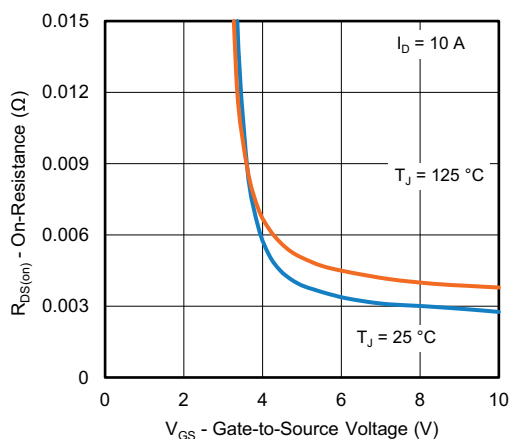
Single Pulse Power



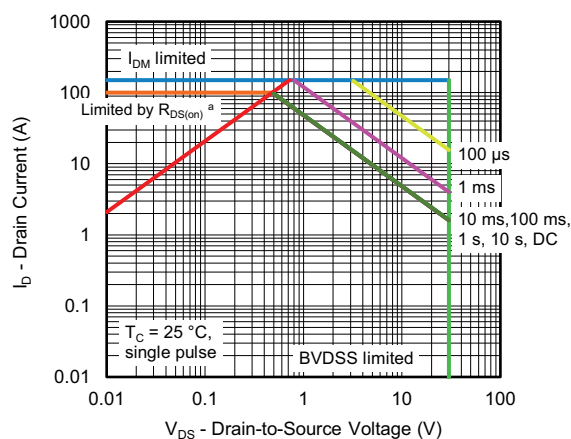
Threshold Voltage



Safe Operating Area, Junction-to-Ambient



On-Resistance vs. Gate-to-Source Voltage



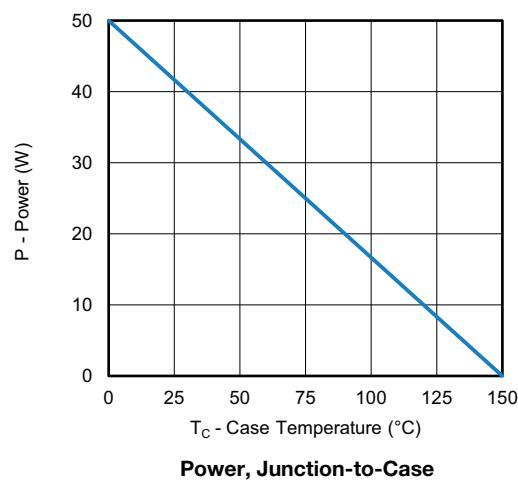
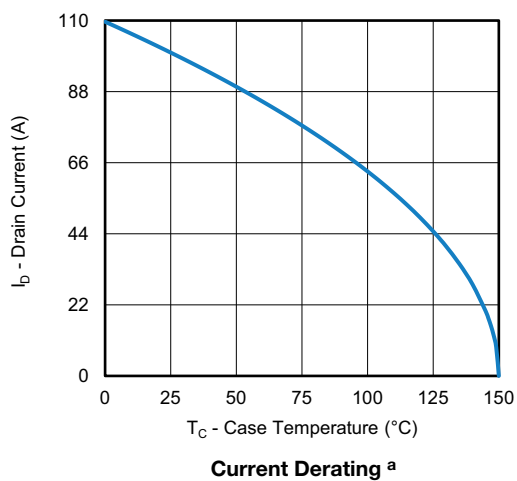
Safe Operating Area, Junction-to-Case

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

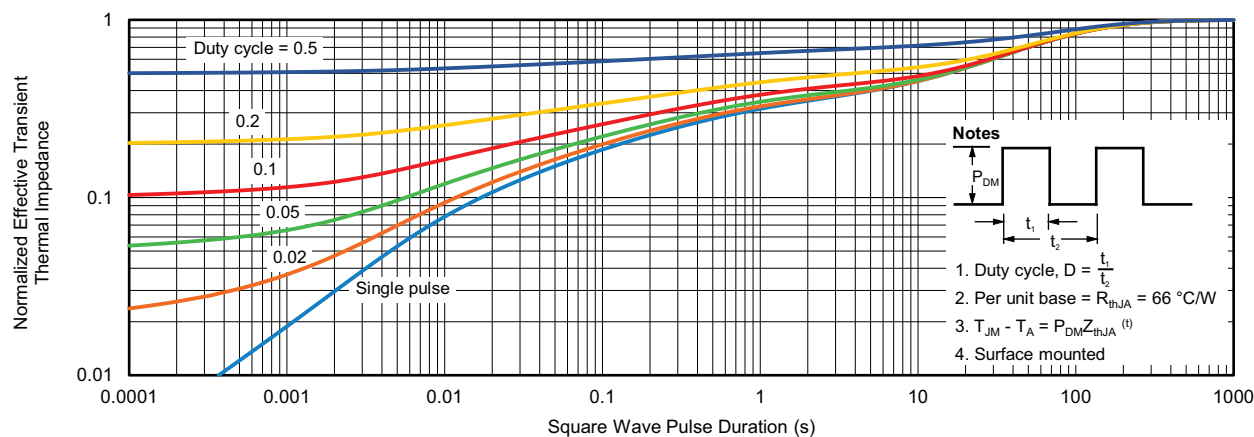


Notes

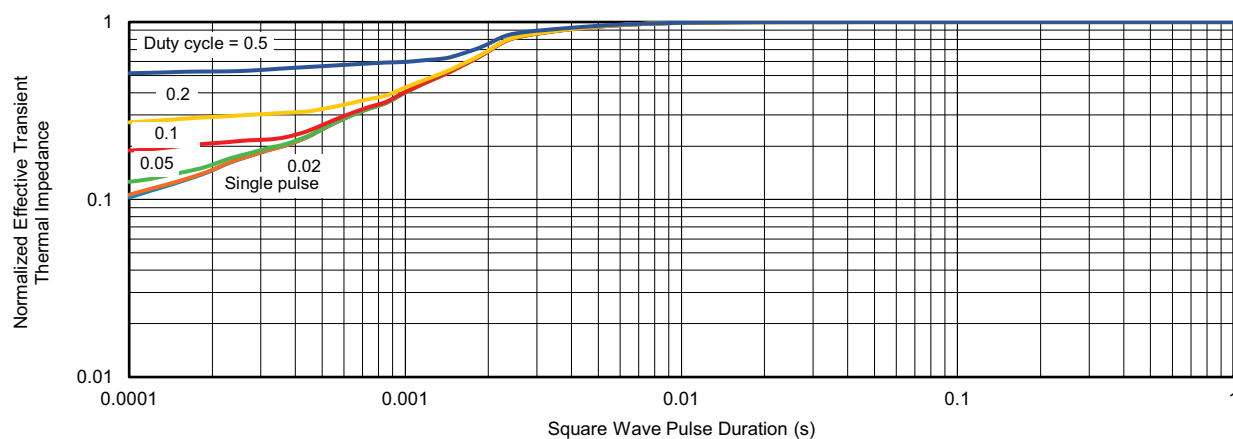
- The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit
- $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



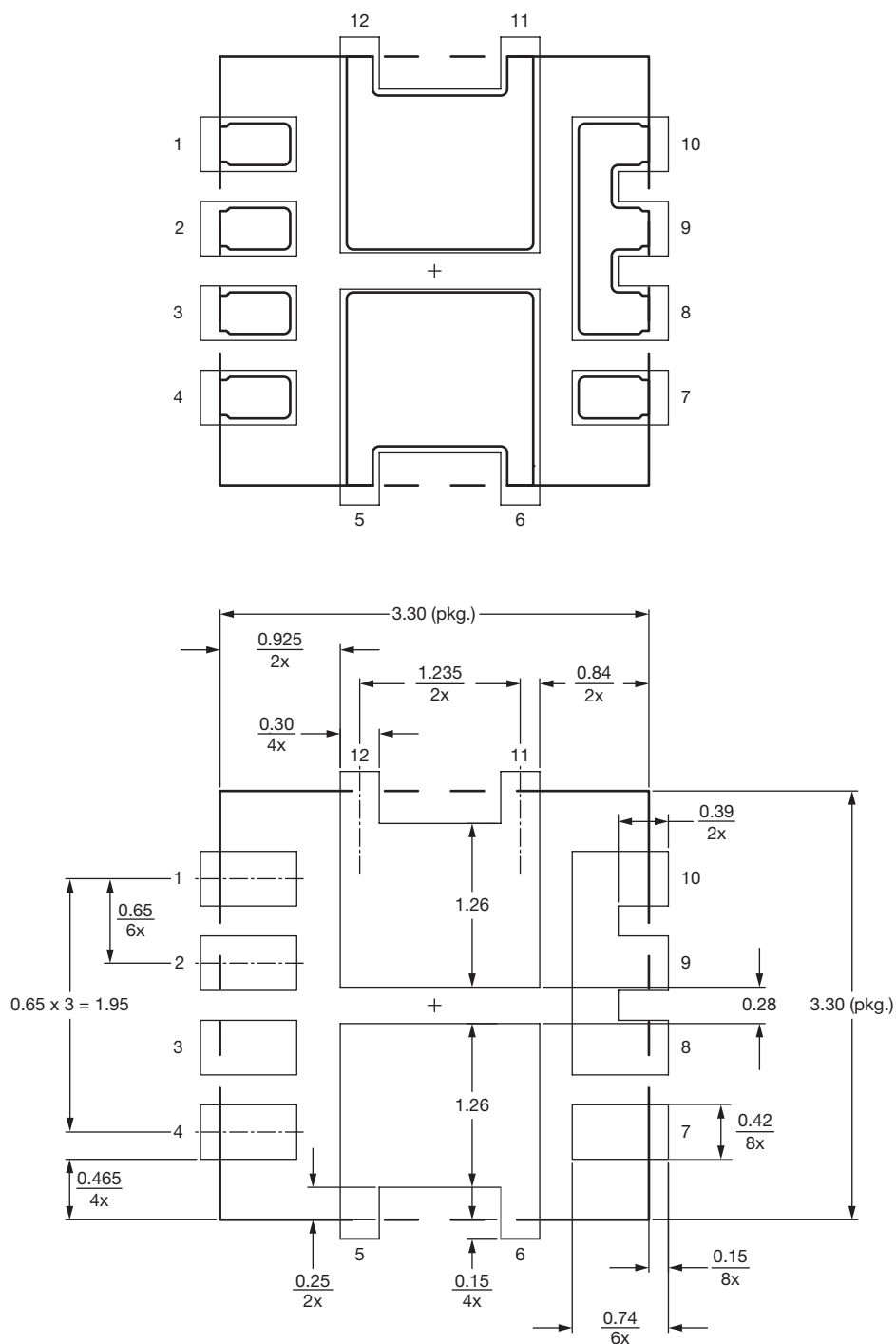
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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Recommended Land Pattern



Note

- Dimensions in mm

ECN: T23-0180-Rev. B, 16-May-2023
DWG: 3006



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