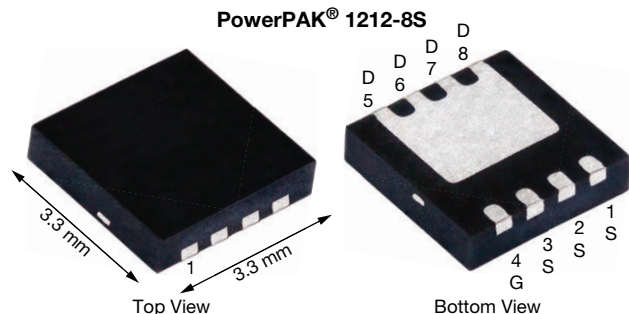


N-Channel 70 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	70
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0058
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0078
Q_g typ. (nC)	15
I_D (A)	66.7
Configuration	Single

FEATURES

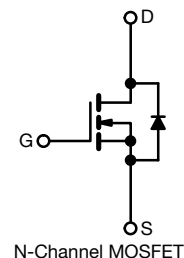
- TrenchFET® Gen IV power MOSFET
- Very low $R_{DS} \times Q_g$ figure-of-merit (FOM)
- Tuned for the lowest $R_{DS} \times Q_{oss}$ FOM
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- DC/DC conversion topologies
- Bus converters
- Synchronous rectification
- Primary side switch



N-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiSS78LDN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	70	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	66.7	A
	$T_C = 70$ °C	53.3	
	$T_A = 25$ °C	19.4 ^{b, c}	
	$T_A = 70$ °C	15.5 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	120	A
Continuous source-drain diode current	$T_C = 25$ °C	51.8	A
	$T_A = 25$ °C	4.3 ^{b, c}	
Single pulse avalanche current	$L = 0.1$ mH	25	mJ
Single pulse avalanche energy	E_{AS}	31.2	
Maximum power dissipation	$T_C = 25$ °C	57	W
	$T_C = 70$ °C	36	
	$T_A = 25$ °C	4.8 ^{b, c}	
	$T_A = 70$ °C	3 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) °		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	21	26	°C/W
Maximum junction-to-case (drain)	R_{thJC}	1.7	2.2	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W
- $T_C = 25$ °C

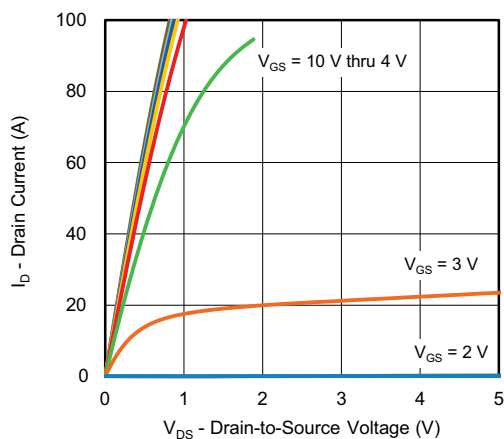
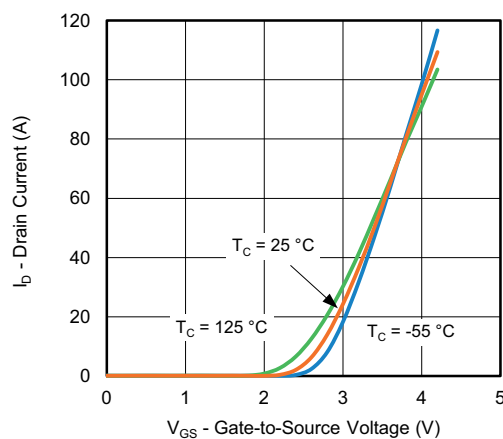
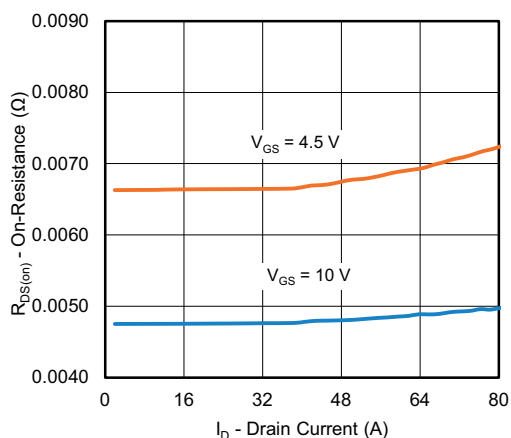
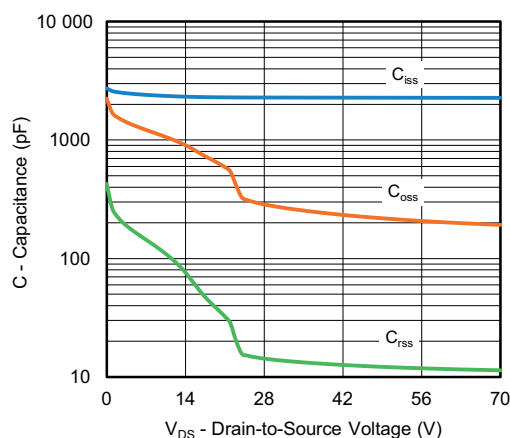
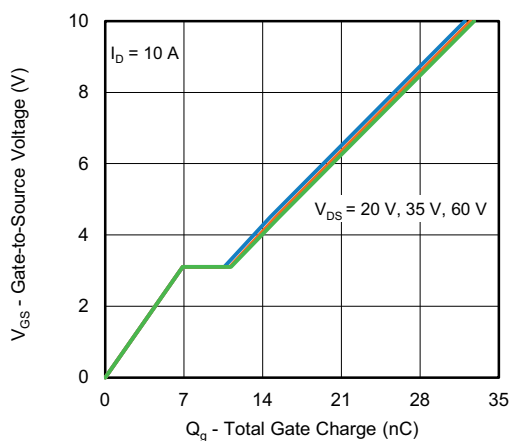
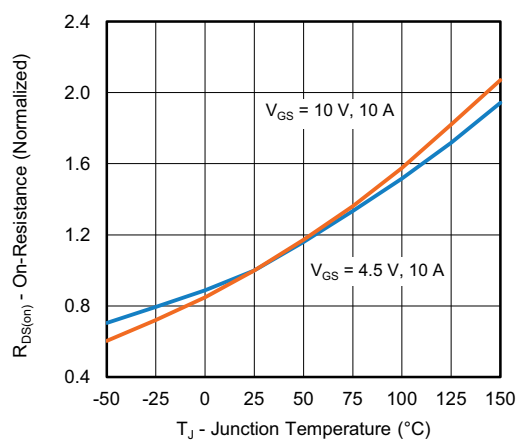


SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	70	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	47	-	mV/ $^{\circ}\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-4.6	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	-	2.3	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 70\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 70\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 70\text{ }^{\circ}\text{C}$	-	-	15	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}$, $V_{GS} = 10\text{ V}$	40	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$	-	0.0048	0.0058	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$	-	0.0065	0.0078	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 10\text{ A}$	-	37	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 35\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	-	2280	-	pF
Output capacitance	C_{oss}		-	260	-	
Reverse transfer capacitance	C_{rss}		-	13.5	-	
Total gate charge	Q_g	$V_{DS} = 35\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$	-	32	50	nC
Gate-source charge	Q_{gs}	$V_{DS} = 35\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$	-	15	23	
Gate-drain charge	Q_{gd}		-	6.9	-	
Output charge	Q_{oss}		-	3.9	-	
Gate resistance	R_g	$V_{DS} = 35\text{ V}$, $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	-	27.5	-	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 35\text{ V}$, $R_L = 4\text{ }\Omega$, $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	0.3	0.82	1.5	ns
Rise time	t_r		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	6	12	
Fall time	t_f		-	21	42	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 35\text{ V}$, $R_L = 4\text{ }\Omega$, $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	-	7	14	
Rise time	t_r		-	21	42	
Turn-off delay time	$t_{d(off)}$		-	58	110	
Fall time	t_f		-	28	56	
			-	12	24	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$	-	-	51.8	A
Pulse diode forward current	I_{SM}		-	-	120	
Body diode voltage	V_{SD}	$I_S = 5\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.77	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 10\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$	-	32	64	ns
Body diode reverse recovery charge	Q_{rr}		-	27	54	nC
Reverse recovery fall time	t_a		-	17	-	ns
Reverse recovery rise time	t_b		-	15	-	

Notes

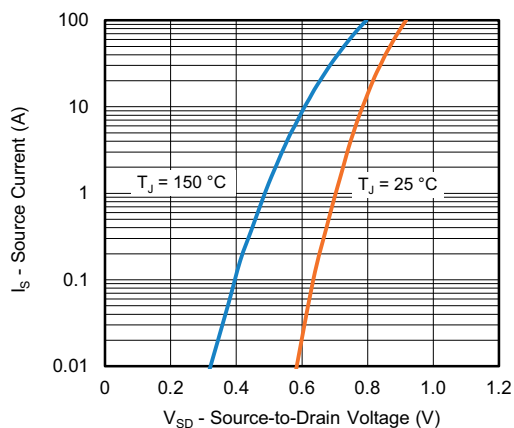
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

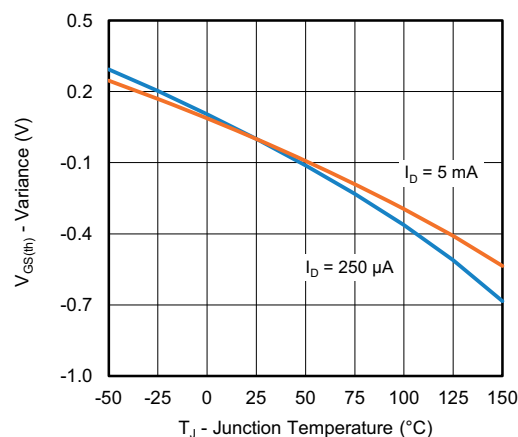
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



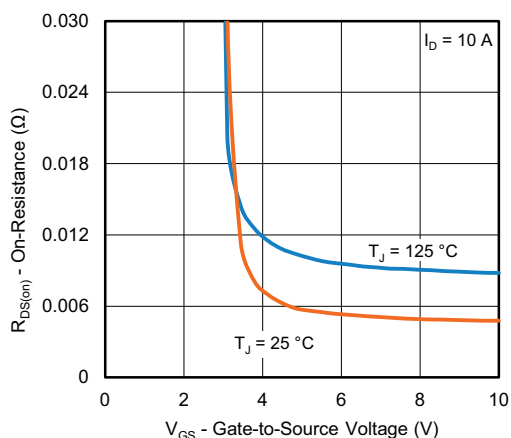
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



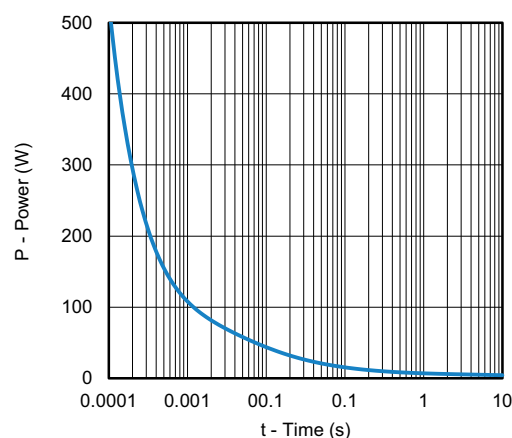
Source-Drain Diode Forward Voltage



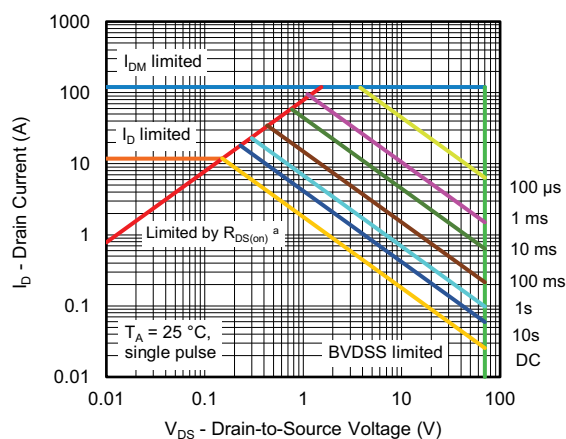
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



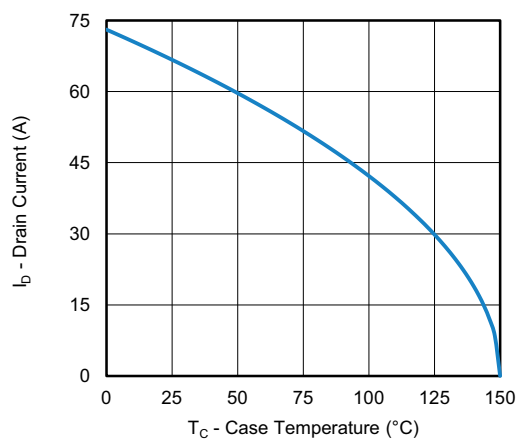
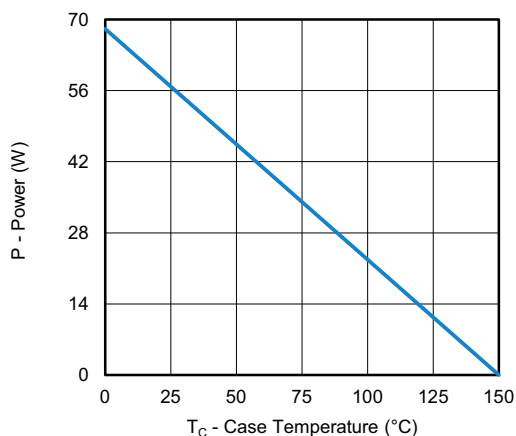
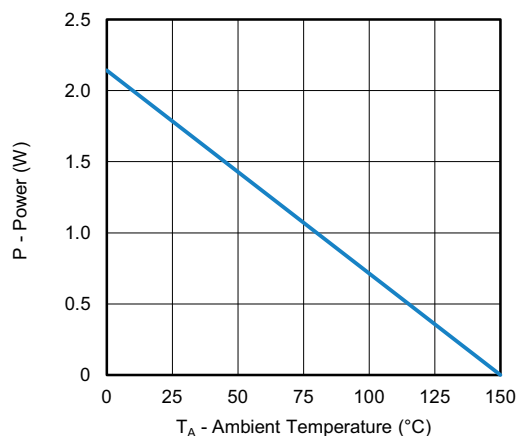
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

Note

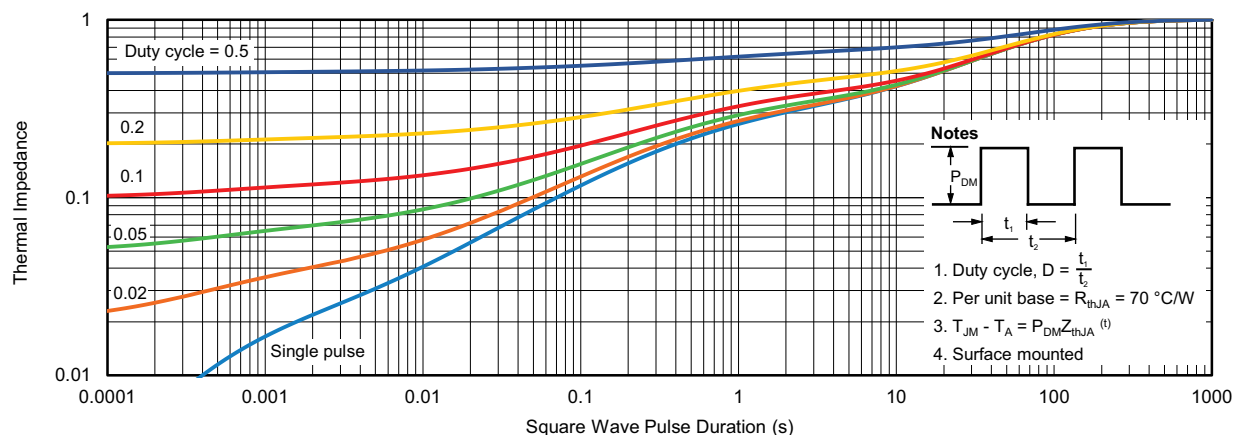
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

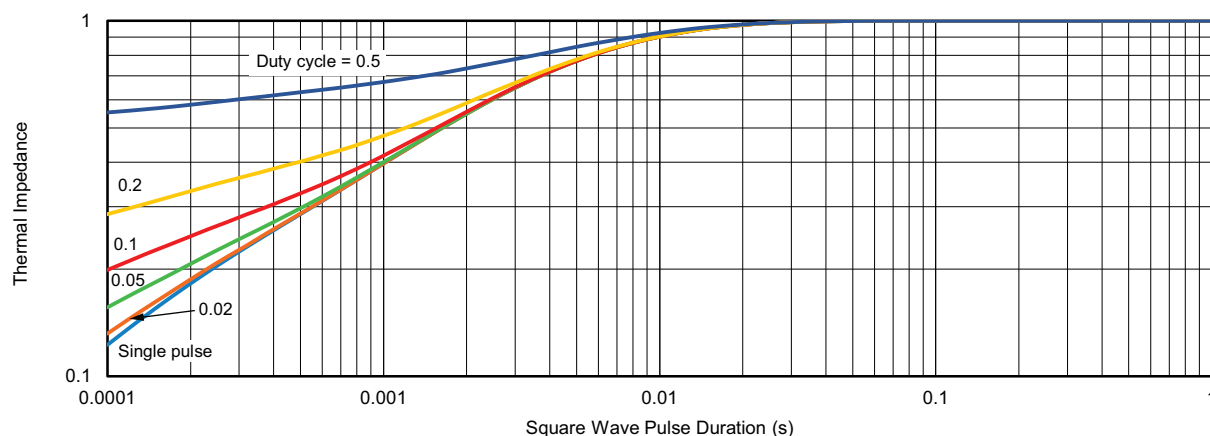
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



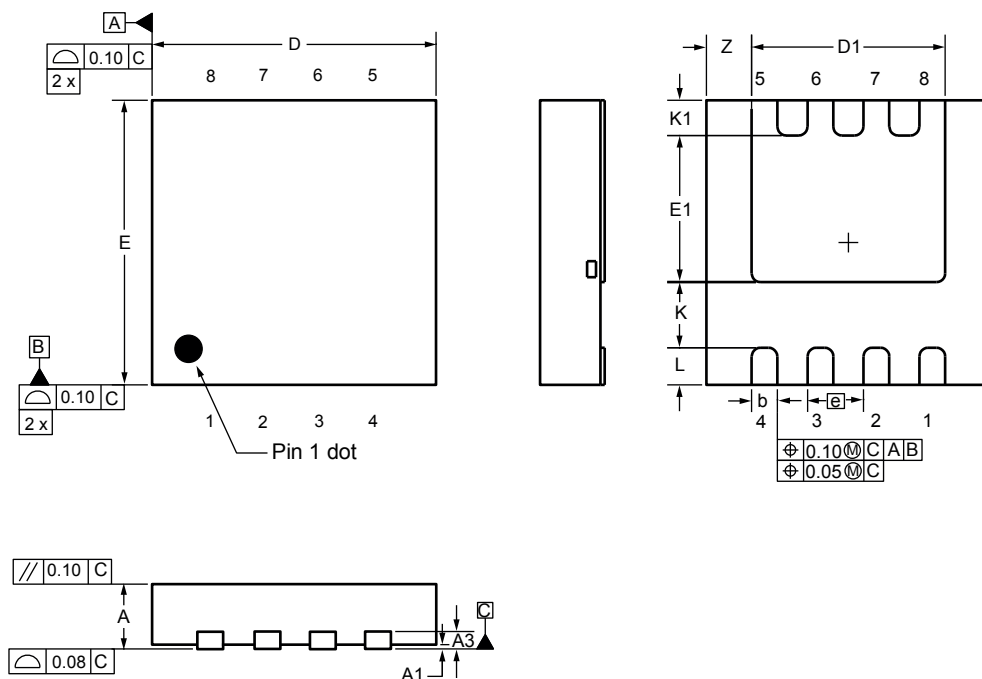
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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Case Outline for PowerPAK® 1212-8S



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.026	0.030	0.033
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		
ECN: C20-0862-Rev. B, 20-Jul-2020						
DWG: 6008						



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