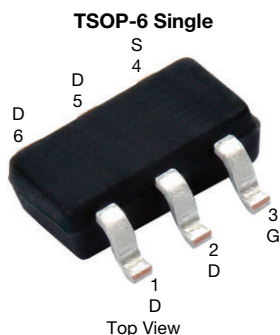


P-Channel 80 V (D-S) MOSFET



Marking Code: BU

PRODUCT SUMMARY

V_{DS} (V)	-80
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.0827
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.1242
Q_g typ. (nC)	5.6
I_D (A) ^a	-5.4
Configuration	Single

ORDERING INFORMATION

Package	TSOP-6 Single
Lead (Pb)-free and halogen-free	Si3129DV-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-80	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current ($T_J = 150\text{ }^{\circ}\text{C}$)	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	-5.4	A
	$T_C = 70\text{ }^{\circ}\text{C}$		-4.4	
	$T_A = 25\text{ }^{\circ}\text{C}$		-3.8 ^{b, c}	
	$T_A = 70\text{ }^{\circ}\text{C}$		-3.0 ^{b, c}	
Pulsed drain current ($t = 300\text{ }\mu\text{s}$)		I_{DM}	-20	
Continuous source-drain diode current	$T_C = 25\text{ }^{\circ}\text{C}$	I_S	-3.5	
	$T_A = 25\text{ }^{\circ}\text{C}$		-1.7 ^{b, c}	
Single pulse avalanche energy	$L = 0.1\text{ mH}$	I_{AS}	15	
		E_{AS}	11	
Maximum power dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	4.2	W
	$T_C = 70\text{ }^{\circ}\text{C}$		2.7	
	$T_A = 25\text{ }^{\circ}\text{C}$		2 ^{b, c}	
	$T_A = 70\text{ }^{\circ}\text{C}$		1.3 ^{b, c}	
Operating junction and storage temperature range		T_J, T_{sta}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	45	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R_{thJF}	25	30	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 5$ s
- Maximum under steady state conditions is 110 °C/W

FEATURES

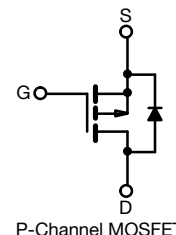
- TrenchFET® power MOSFET
- 100 % R_g tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912

APPLICATIONS

- Power management for portable and consumer
 - Load switches
 - DC/DC converters



RoHS
COMPLIANT
HALOGEN
FREE



P-Channel MOSFET



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-80	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -10 mA	-	-115	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	4.8	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1.5	-	-2.5	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -80 V, V _{GS} = 0 V	-	-	-10	μA
		V _{DS} = -80 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-50	
On-state drain current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-5	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -3.8 A	-	0.0689	0.0827	Ω
		V _{GS} = -4.5 V, I _D = -3.1 A	-	0.0994	0.1242	
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = -40 V, V _{GS} = 0 V, f = 1 MHz	-	805	-	pF
Output capacitance	C _{oss}		-	265	-	
Reverse transfer capacitance	C _{rss}		-	10	-	
Total gate charge	Q _g	V _{DS} = -40 V, V _{GS} = -10 V, I _D = -3.8 A	-	12	18	nC
		V _{DS} = -40 V, V _{GS} = -4.5 V, I _D = -3.8 A	-	5.6	8.4	
Gate-source charge	Q _{gs}		-	3.1	-	
Gate-drain charge	Q _{gd}		-	1.4	-	
Gate resistance	R _g	f = 1 MHz	0.8	4.4	8.8	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = -40 V, R _L = 13.3 Ω I _D ≅ -3 A, V _{GEN} = - 10 V, R _g = 1 Ω	-	15	30	ns
Rise time	t _r		-	8	16	
Turn-off delay time	t _{d(off)}		-	25	50	
Fall time	t _f		-	12	24	
Turn-on delay time	t _{d(on)}	V _{DD} = -40 V, R _L = 13.3 Ω I _D ≅ -3 A, V _{GEN} = - 4.5, R _g = 1 Ω	-	28	56	
Rise time	t _r		-	42	84	
Turn-off delay time	t _{d(off)}		-	24	48	
Fall time	t _f		-	15	30	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-3.5	A
Pulse diode forward current	I _{SM}		-	-	-20	
Body diode voltage	V _{SD}	I _S = -3 A, V _{GS} = 0 V	-	-0.8	-1.2	V
Body diode reverse recovery time	t _{rr}	I _F = -3 A, dI/dt = 100 A/μs, T _J = 25 °C	-	38	57	ns
Body diode reverse recovery charge	Q _{rr}		-	50	75	nC
Reverse recovery fall time	t _a		-	26	-	ns
Reverse recovery rise time	t _b		-	12	-	

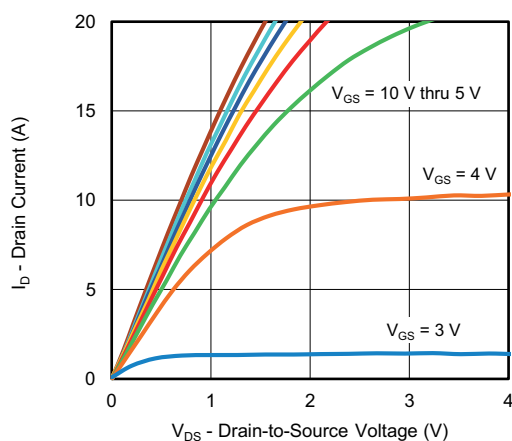
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

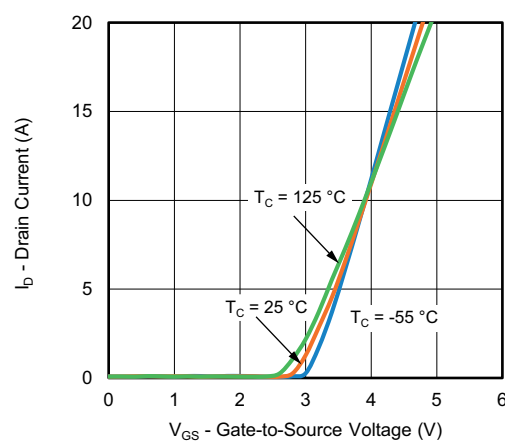
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



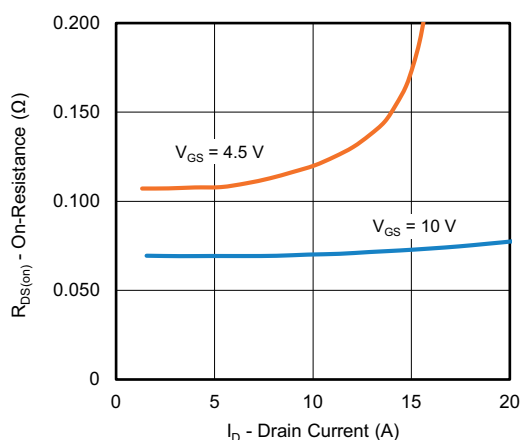
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



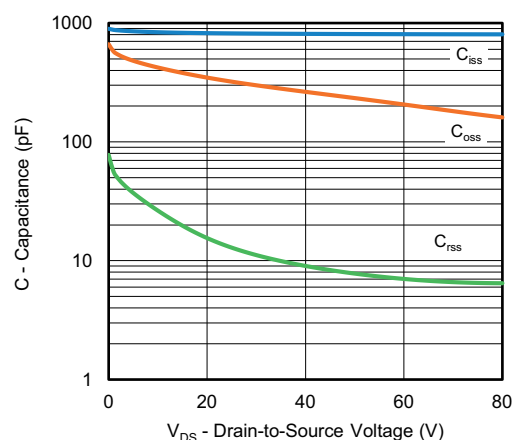
Output Characteristics



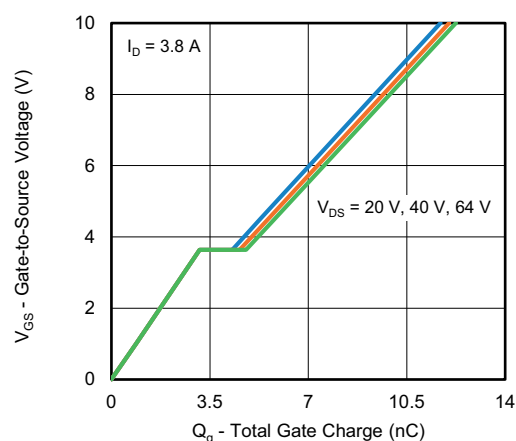
Transfer Characteristics



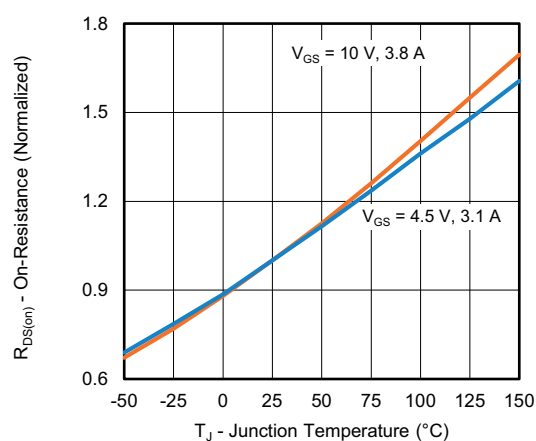
On-Resistance vs. Drain Current



Capacitance



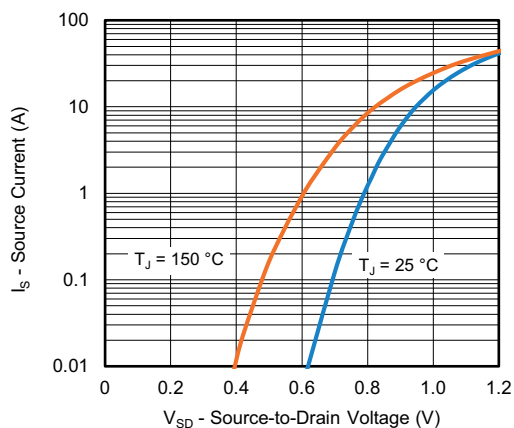
Gate Charge



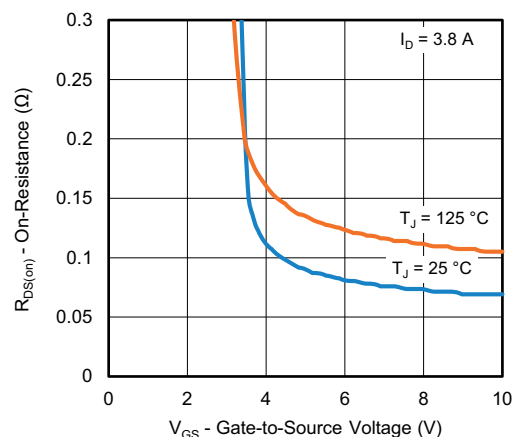
On-Resistance vs. Junction Temperature



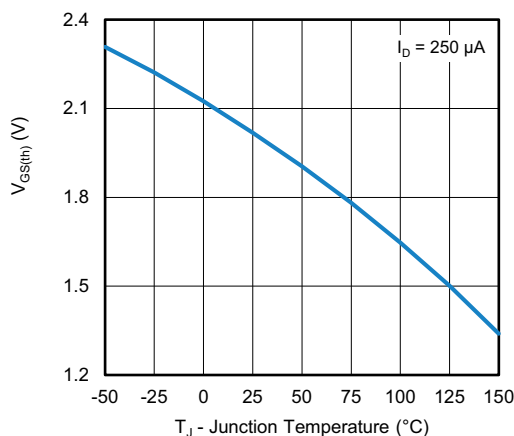
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



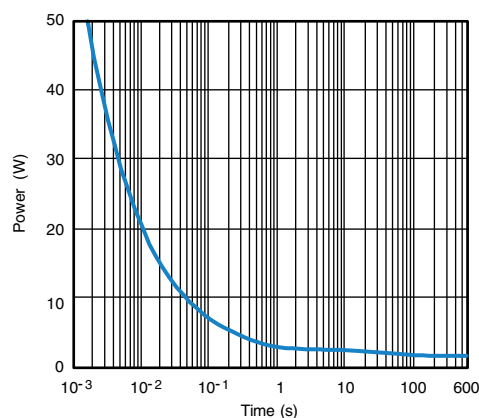
Source-Drain Diode Forward Voltage



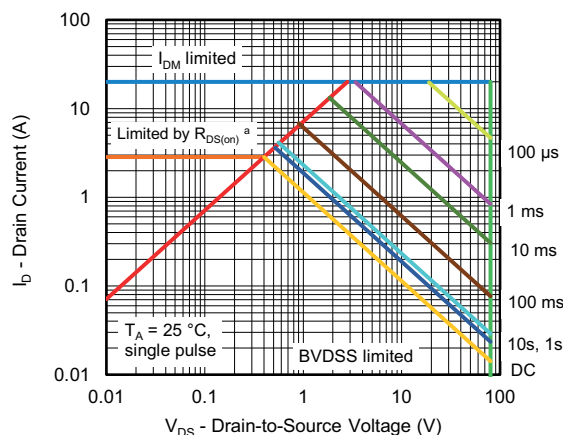
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



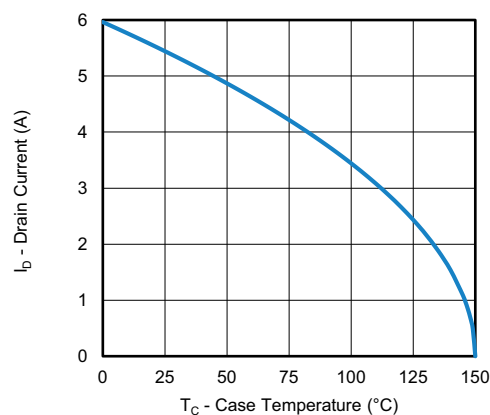
Safe Operating Area

Note

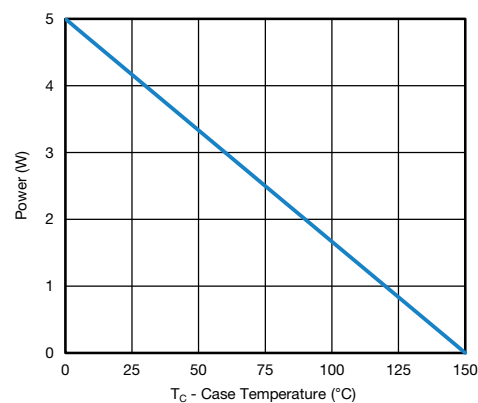
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



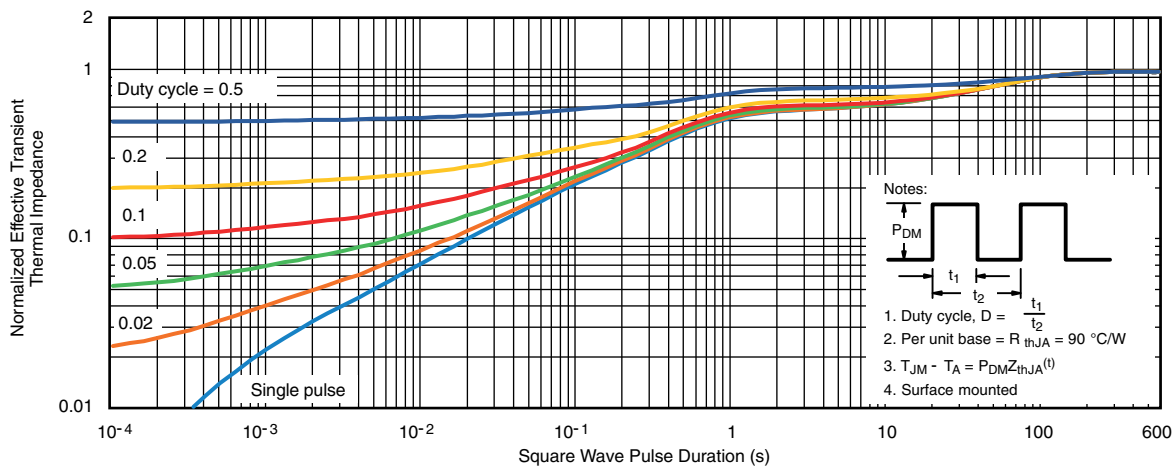
Power Junction-to-Case

Note

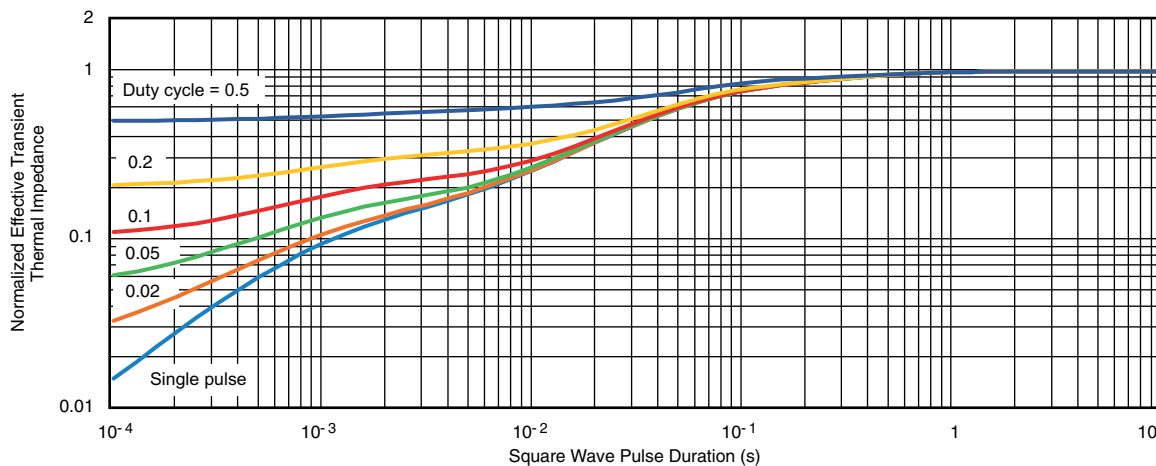
- a. The power dissipation P_D is based on $T_{J \text{ max.}} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

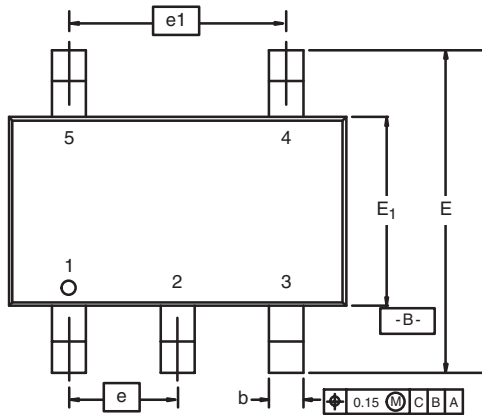


Normalized Thermal Transient Impedance, Junction-to-Foot

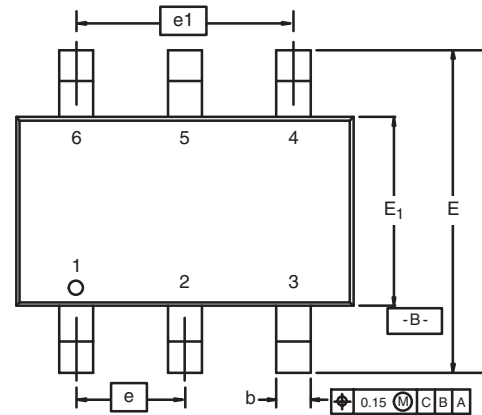
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?78984.

TSOP: 5/6-LEAD

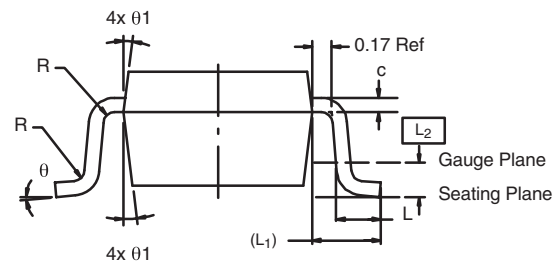
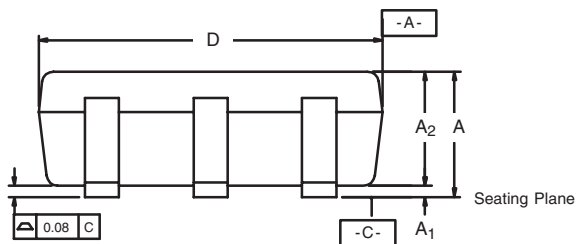
JEDEC Part Number: MO-193C



5-LEAD TSOP

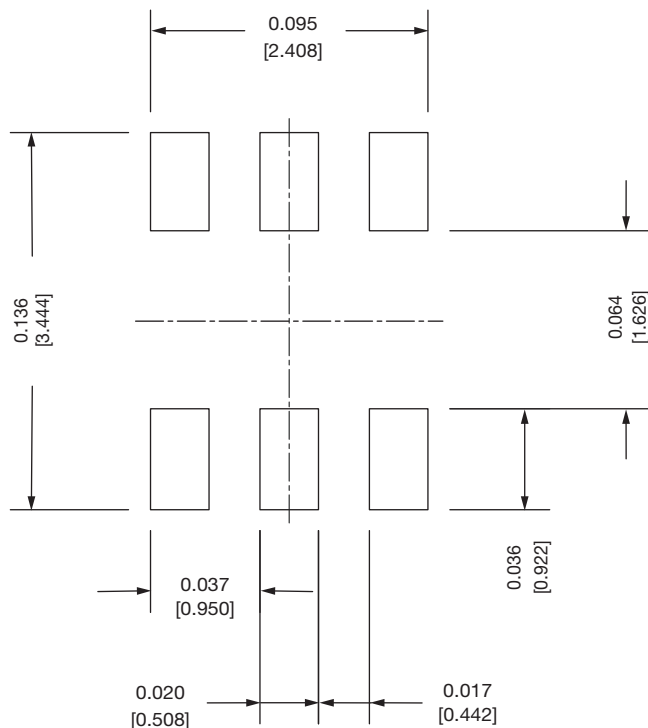
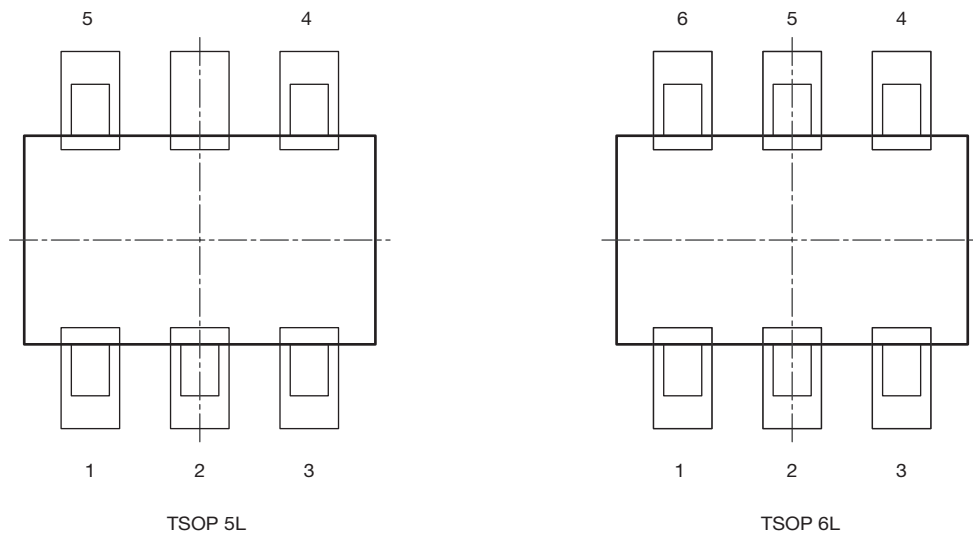


6-LEAD TSOP



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

Recommended Land Pattern For TSOP-5L / TSOP-6L


Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
DWG: 3010



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