Precision Rail-to-Rail Input and Output Operational Amplifiers

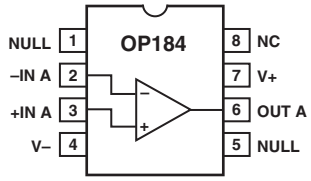
OP184/OP284/OP484

FEATURES
Single-Supply Operation
Wide Bandwidth: 4 MHz
Low Offset Voltage: 65 μV
Unity-Gain Stable
High Slew Rate: 4.0 V/μs
Low Noise: 3.9 nV/√Hz

APPLICATIONS
Battery Powered Instrumentation
Power Supply Control and Protection
Telecom
DAC Output Amplifier
ADC Input Buffer

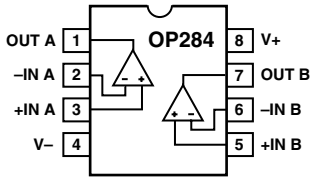
PIN CONFIGURATIONS

8-Lead Epoxy DIP
(P Suffix)
8-Lead SO
(S Suffix)

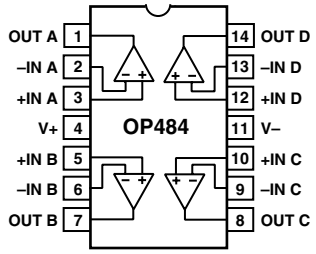


NC = NO CONNECT

8-Lead Epoxy DIP
(P Suffix)
8-Lead SO
(S Suffix)



14-Lead Epoxy DIP
(P Suffix)
14-Lead Narrow-Body SO
(S Suffix)



GENERAL DESCRIPTION

The OP184/OP284/OP484 are single, dual and quad single-supply, 4 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. They are guaranteed to operate from 3 to 36 (or ±1.5 to ±18) volts and will function with a single supply as low as 1.5 volts.

These amplifiers are superb for single-supply applications requiring both ac and precision dc performance. The combination of bandwidth, low noise and precision makes the OP184/OP284/OP484 useful in a wide variety of applications, including filters and instrumentation.

Other applications for these amplifiers include portable telecom equipment, power supply control and protection, and as amplifiers or buffers for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezo electric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios.

The OP184/OP284/OP484 are specified over the HOT extended industrial (–40°C to +125°C) temperature range. The single and dual are available in 8-lead plastic DIP plus SO surface mount packages. The quad OP484 is available in 14-lead plastic DIPs and 14-lead narrow-body SO packages.

REV. B

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703
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OP184/OP284/OP484–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage "OP184/284E" Grade	V_{OS}	(Note 1)			65	µV
		–40°C ≤ T_A ≤ +125°C			165	µV
Offset Voltage "OP184/284F" Grade	V_{OS}				125	µV
		–40°C ≤ T_A ≤ +125°C			350	µV
Offset Voltage "OP484E" Grade	V_{OS}				75	µV
		–40°C ≤ T_A ≤ +125°C			175	µV
Offset Voltage "OP484F" Grade	V_{OS}				150	µV
		–40°C ≤ T_A ≤ +125°C			450	µV
Input Bias Current	I_B			60	450	nA
		–40°C ≤ T_A ≤ +125°C			600	nA
Input Offset Current	I_{OS}			2	50	nA
		–40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	60			dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.0 V to 4.0 V, –40°C ≤ T_A ≤ +125°C	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 1 V ≤ V_O ≤ 4 V	50	240		V/mV
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +125°C	25			V/mV
Bias Current Drift	$\Delta I_B/\Delta T$			150		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	4.85			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			125	mV
Output Current	I_{OUT}		±6.5			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.0 V to 10 V, –40°C ≤ T_A ≤ +125°C	76			dB
Supply Current/Amplifier	I_{SY}	V_O = 2.5 V, –40°C ≤ T_A ≤ +125°C			1.45	mA
Supply Voltage Range	V_S		3		36	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	1.65	2.4		V/µs
Settling Time	t_S	To 0.01%, 1.0 V Step		2.5		µs
Gain Bandwidth Product	GBP			3.25		MHz
Phase Margin	Øo			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		0.3		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		3.9		nV/$\sqrt{Hz}$
Current Noise Density	i_N			0.4		pA/$\sqrt{Hz}$

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = 3.0 V, V_{CM} = 1.5 V, T_A = 25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage "OP184/284E" Grade	V_{OS}	(Note 1)			65	µV
		–40°C ≤ T_A ≤ +125°C			165	µV
Offset Voltage "OP184/284F" Grade	V_{OS}				125	µV
		–40°C ≤ T_A ≤ +125°C			350	µV
Offset Voltage "OP484E" Grade	V_{OS}				100	µV
		–40°C ≤ T_A ≤ +125°C			200	µV
Offset Voltage "OP484F" Grade	V_{OS}				150	µV
		–40°C ≤ T_A ≤ +125°C			450	µV
Input Bias Current	I_B			60	450	nA
		–40°C ≤ T_A ≤ +125°C			600	nA
Input Offset Current	I_{OS}	–40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	60			dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V, –40°C ≤ T_A ≤ +125°C	56			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	2.85			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			125	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.25 V to ±1.75 V	76			dB
Supply Current/Amplifier	I_{SY}	V_O = 1.5 V, –40°C ≤ T_A ≤ +125°C			1.35	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP			3		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f = 1 kHz		3.9		nV/√Hz

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, V_{CM} = 0 V, T_A = 25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage "OP184/284E" Grade	V_{OS}	(Note 1)			100	µV
		–40°C ≤ T_A ≤ +125°C			200	µV
Offset Voltage "OP284F" Grade	V_{OS}				175	µV
		–40°C ≤ T_A ≤ +125°C			375	µV
Offset Voltage "OP484E" Grade	V_{OS}				150	µV
		–40°C ≤ T_A ≤ +125°C			300	µV
Offset Voltage "OP484F" Grade	V_{OS}				250	µV
		–40°C ≤ T_A ≤ +125°C			500	µV
Input Bias Current	I_B			80	450	nA
		–40°C ≤ T_A ≤ +125°C			575	nA
Input Offset Current	I_{OS}	–40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			–15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –14.0 V to +14.0 V, –40°C ≤ T_A ≤ +125°C	86	90		dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = –15.0 V to +15.0 V	80			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, –10 V ≤ V_O ≤ 10 V	150	1000		V/mV
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +125°C	75			V/mV
Offset Voltage Drift "E" Grade	$\Delta V_{OS}/\Delta T$			0.2	2.00	µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			150		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	14.8			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			–14.875	V
Output Current	I_{OUT}		±10			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.0 V to ±18 V, –40°C ≤ T_A ≤ +125°C	90			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V, –40°C ≤ T_A ≤ +125°C			2.0	mA
Supply Current/Amplifier	I_{SY}	V_S = ±18 V, –40°C ≤ T_A ≤ +125°C			2.25	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.4	4.0		V/µs
Full-Power Bandwidth	BW_p	1% Distortion, R_L = 2 kΩ, V_O = 29 V p-p		35		kHz
Settling Time	t_S	To 0.01%, 10 V Step		4		µs
Gain Bandwidth Product	GBP			4.25		MHz
Phase Margin	Øo			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		0.3		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_N			0.4		pA/√Hz

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±0.6 V
Output Short-Circuit Duration to GND[3] . . . . . Indefinite
Storage Temperature Range
P, S Packages . . . . . –65°C to +150°C
Operating Temperature Range
OP184/OP284/OP484E, F . . . . . –40°C to +125°C
Junction Temperature Range
P, S Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
8-Lead Plastic DIP (P)	103	43	°C/W
8-Lead SOIC (S)	158	43	°C/W
14-Lead Plastic DIP (P)	83	39	°C/W
14-Lead SOIC (S)	92	27	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts unless otherwise noted.
[2]For input voltages greater than 0.6 volts, the input current should be limited to less than 5 mA to prevent degradation or destruction of the input devices.
[3]θ_{JA} is specified for the worst case conditions; i.e., θ_{JA} is specified for device in socket for cerdip and P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP184EP*	–40°C to +125°C	8-Lead Plastic DIP	N-8
OP184ES	–40°C to +125°C	8-Lead SOIC	R-8
OP184FP*	–40°C to +125°C	8-Lead Plastic DIP	N-8
OP184FS	–40°C to +125°C	8-Lead SOIC	R-8
OP284EP	–40°C to +125°C	8-Lead Plastic DIP	N-8
OP284ES	–40°C to +125°C	8-Lead SOIC	R-8
OP284FP*	–40°C to +125°C	8-Lead Plastic DIP	N-8
OP284FS	–40°C to +125°C	8-Lead SOIC	R-8
OP484ES	–40°C to +125°C	14-Lead SOIC	R-14
OP484FP	–40°C to +125°C	14-Lead Plastic DIP	N-14
OP484FS	–40°C to +125°C	14-Lead SOIC	R-14

NOTES
*Not for new design; obsolete April 2002.

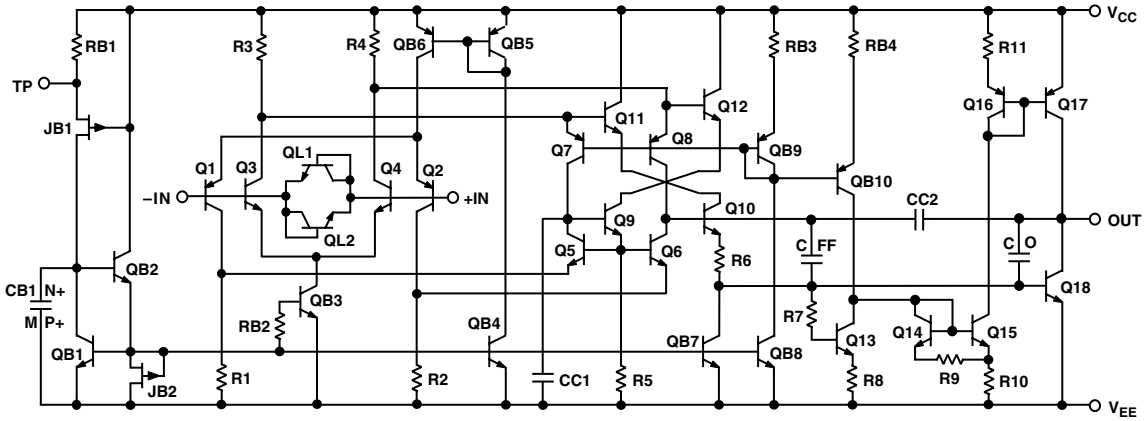


Figure 3. Simplified Schematic