LITE-ON SEMICONDUCTOR

L30ESDL5V0C6-4

ESD PROTECTION DEVICE

STAND-OFF VOLTAGE - **5.0** Volts
POWER DISSIPATION - **300** WATTS

GENERAL DESCRIPTION

The L30ESDL5V0C6-4 is low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

FEATURES

- Protects up to four I/O lines & power line
- Low capacitance: 1.5pF typical (I/O to I/O)
- IEC 61000-4-5 (Lighting), 12A (8/20us)
- IEC 61000-4-2 (ESD), > ±27KV (air) ; > ±27KV (contact).

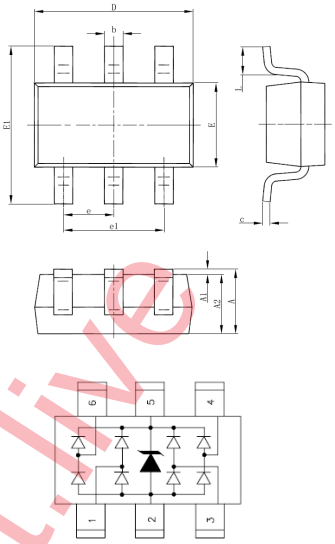
APPLICATION

- Digital Visual Interface (DVI)
- Monitors and Flat Panel Displays
- USB 2.0
- 10/100/1000 Ethernet
- IEEE 1394 Firewire Port

MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/E

SOT23-6L



4 lines Protection

SOT23-6L		
DIM.	MIN.	MAX.
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.08	0.22
D	2.45	3.00
E	1.50	1.75
E1	2.65	2.95
e	0.95 typ.	
e1	1.90 typ.	
L	0.30	0.60
All Dimensions in millimeter		

PIN ASSIGNMENT	
1, 3, 4, 6	I/O Lines
5	V_{CC}
2	Ground

MAXIMUM RATINGS (Tj= 25℃ unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20us)	P_{pk}	300	W
Peak Pulse Current (tp = 8/20us)	Ipp	12	A
Operating Junction Temperature Range	T_J	-55 to + 125	℃
Storage Temperature Range	Tstg	-55 to + 150	℃
Soldering Temperature, t max = 10s	T_L	260	℃

ELECTRICAL CHARACTERISTICS (Tj= 25℃ unless otherwise noticed)

Parameter	Symbol	Conditions	Mln	Typ	Max	Unit
Reverse standoff voltage	V_{RWM}	Any pin to ground	---	---	5.0	V
Breakdown voltage	V_{BR}	I_R = 1 mA	6.0	---	---	V
Reverse leakage current	I_{RM}	V_{DRM} = 5V	---	---	5	uA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20μs, Any I /O pin to ground	---	---	12.5	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20μs, Any I/O pin to ground	---	---	17.5	V
Clamping Voltage	V_C	I_{PP} = 12A, tp = 8/20μs, Any I/O pin to ground	---	---	25	V
Junction capacitance	C_J	V_R = 2.5V, f = 1MHz, Any I/O pin to ground	---	3.5	5.0	pF
Junction capacitance	C_J	V_R = 2.5V, f = 1MHz, Between I/O pins	---	1.5	2.5	pF

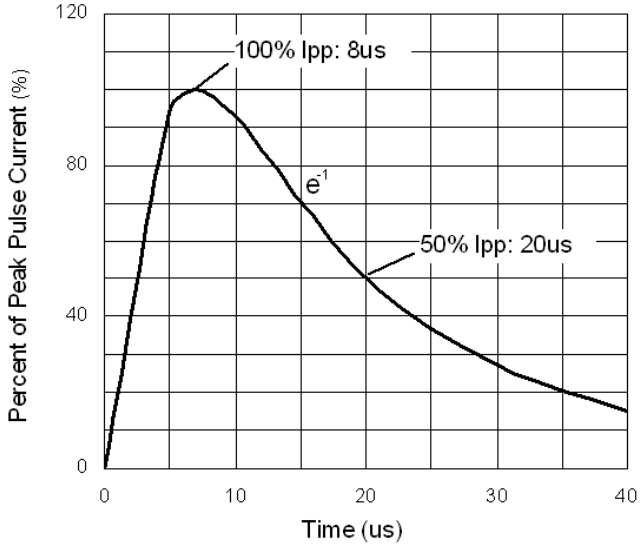


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

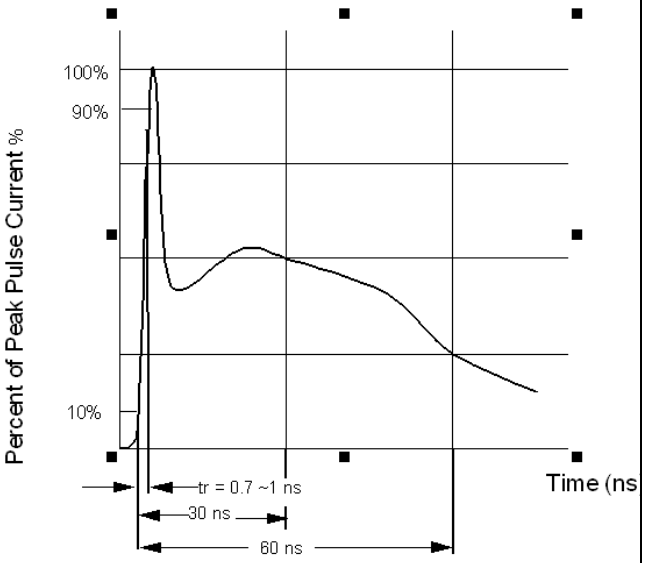


Figure 2. ESD pulse waveform according to IEC 61000-4-2

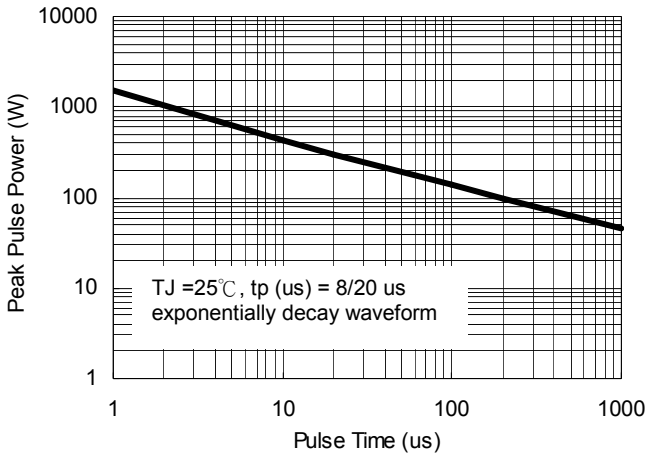


Figure 3. Power Dissipation versus Pulse Time

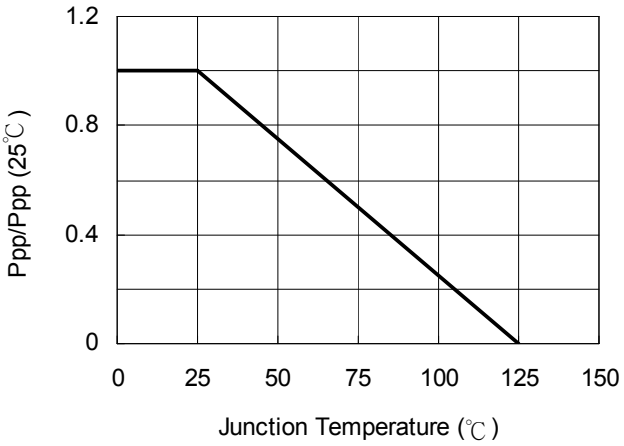


Figure 4. Peak pulse power versus TJ

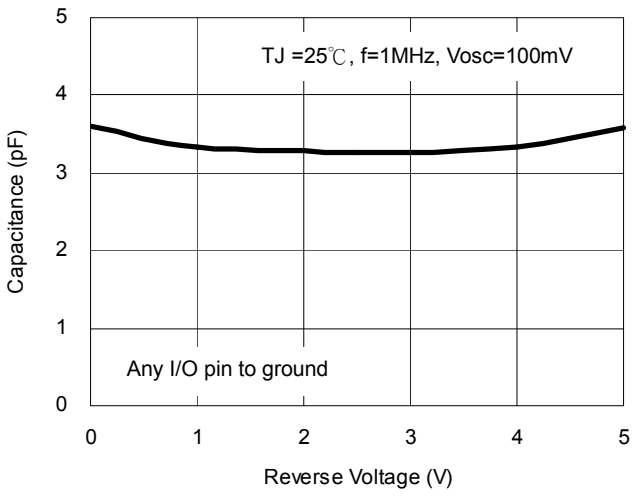


Figure 5. Typical Junction Capacitance

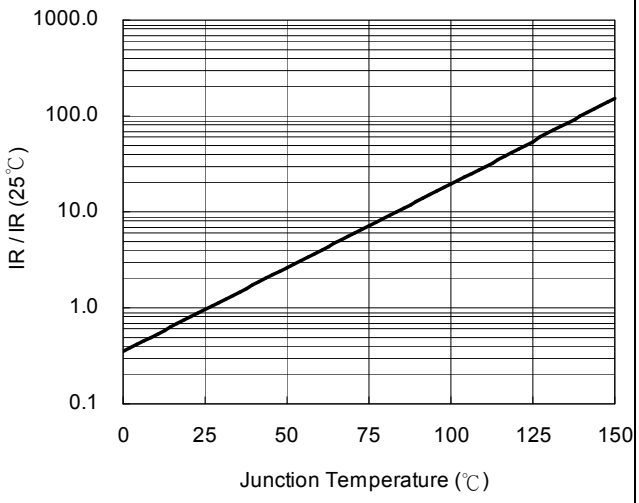


Figure 6. Reverse Leakage Current versus TJ

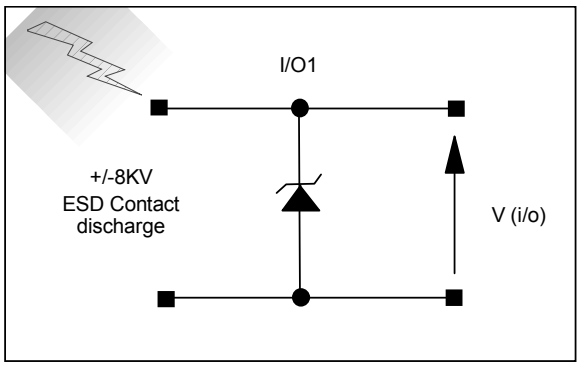


Figure 7. ESD Test Configuration

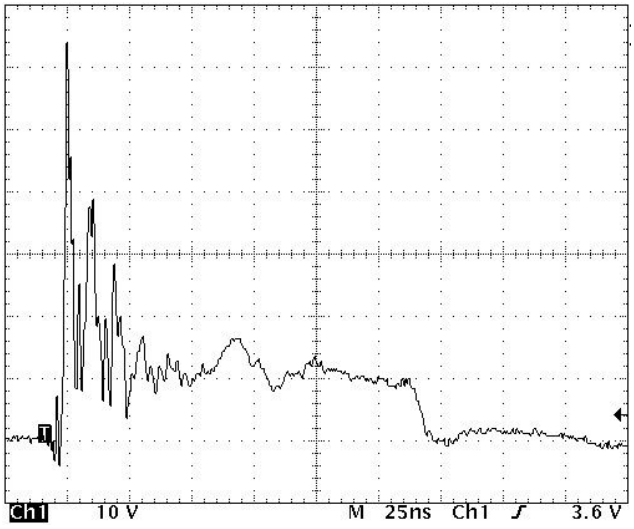


Figure 8. Clamped +8 kV ESD voltage waveform

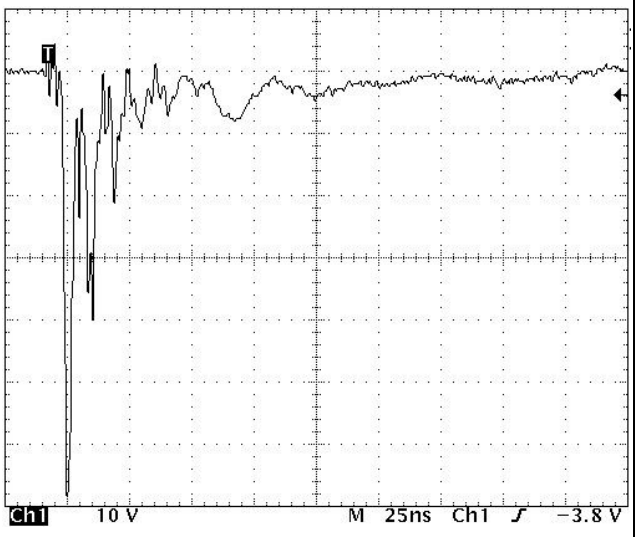


Figure 9. Clamped -8 kV ESD voltage waveform

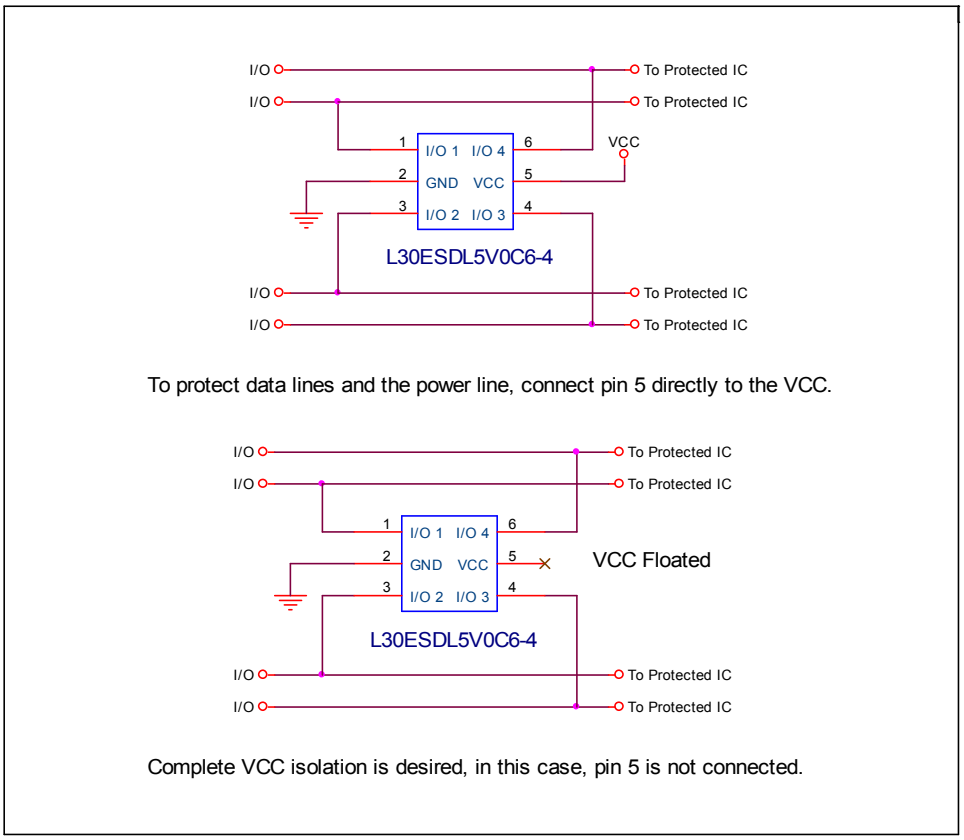


Figure 10. Device Connection Options

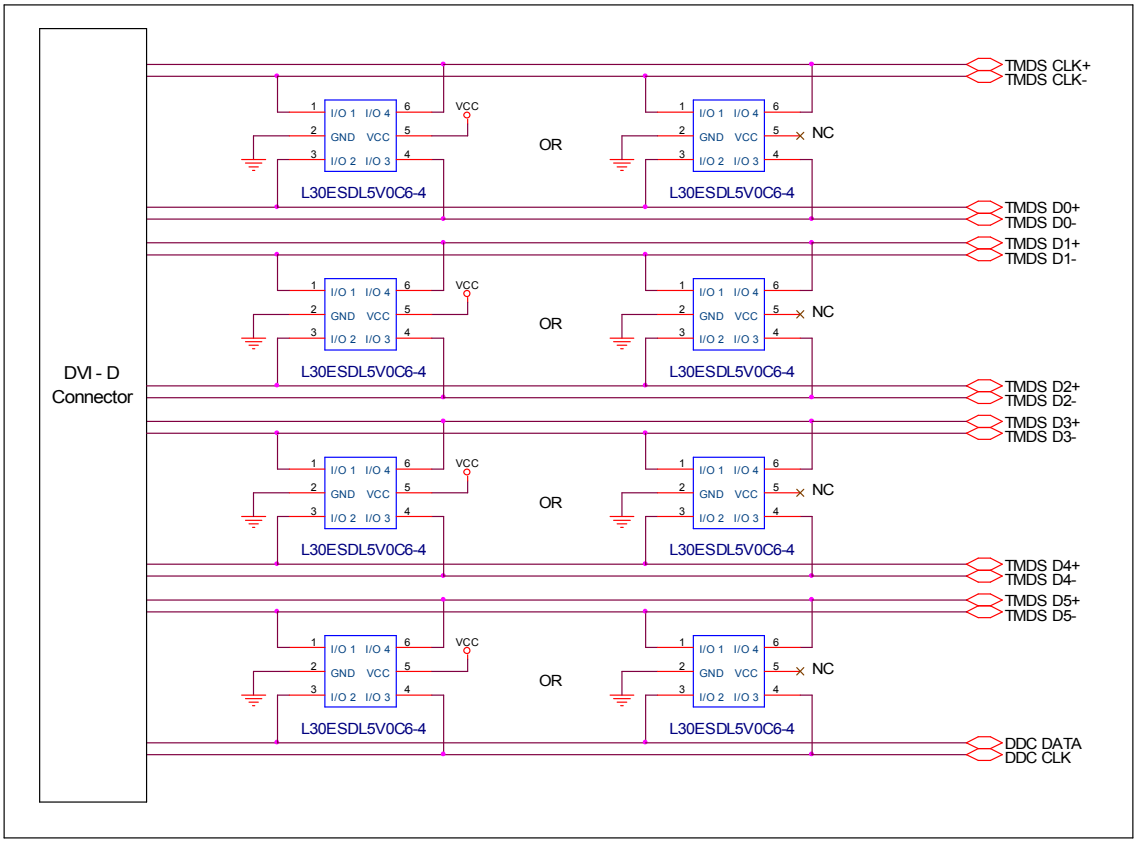


Figure 11. DVI Interface ESD Protection

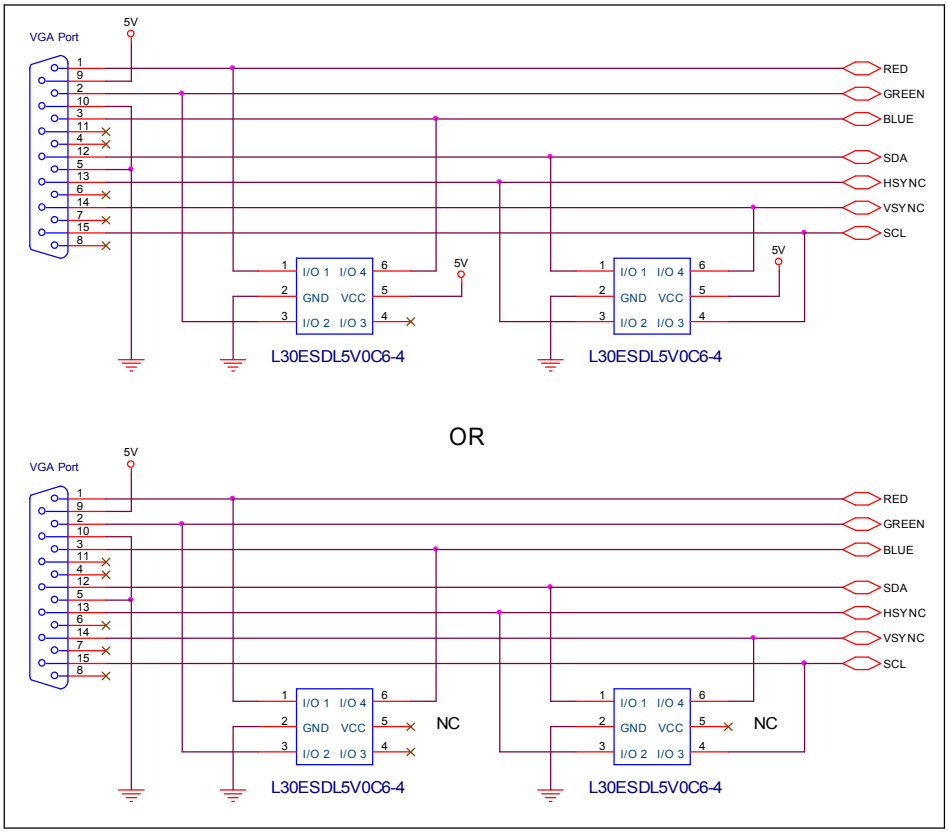


Figure 12. VGA Interface ESD Protection

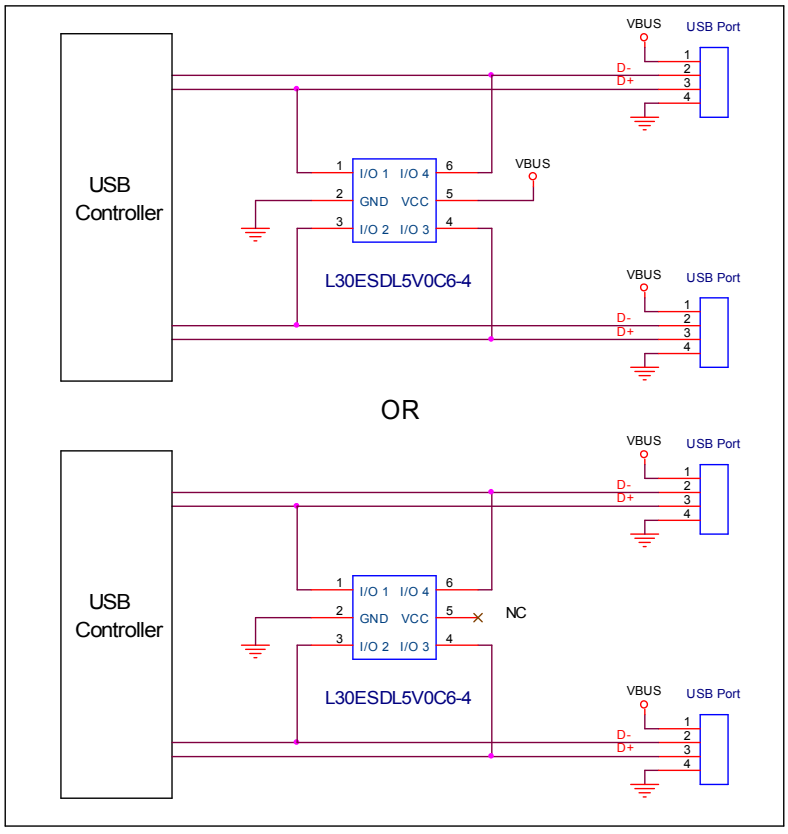


Figure 13. USB2.0 Interface ESD Protection

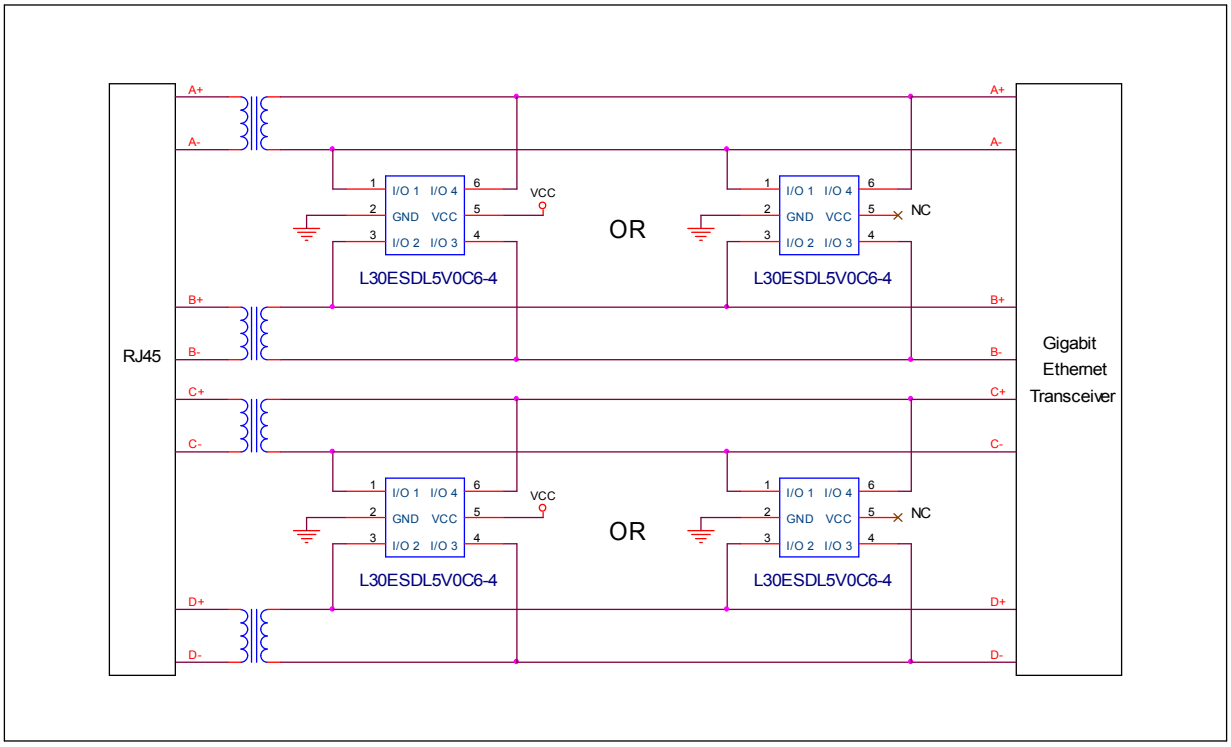


Figure 14. 10/100/1000 Ethernet ESD Protection

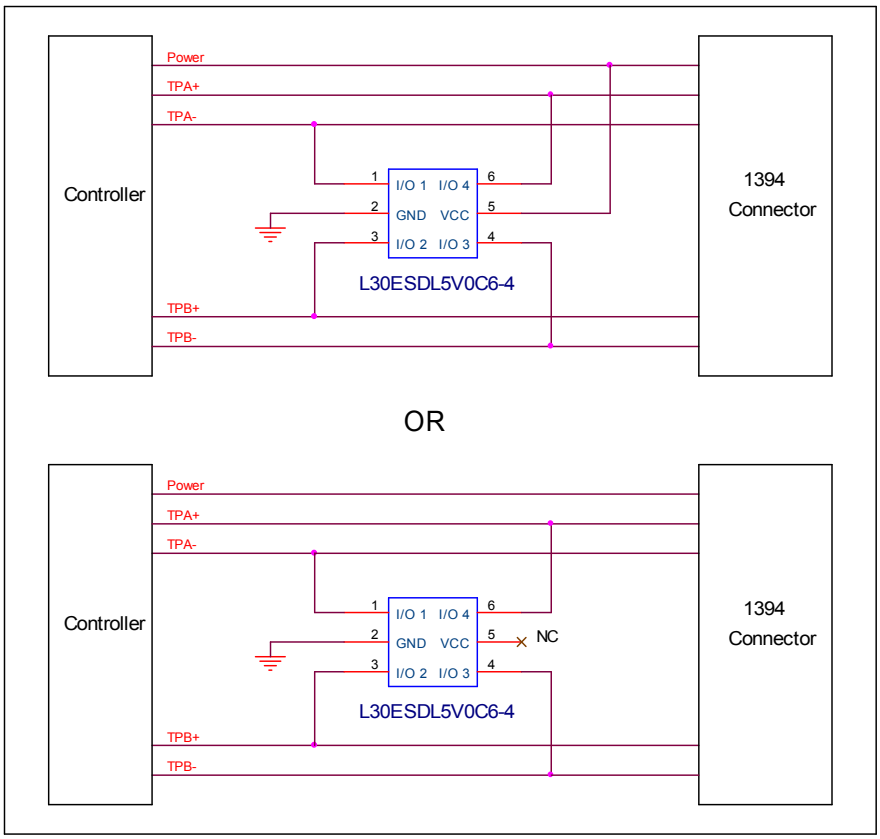
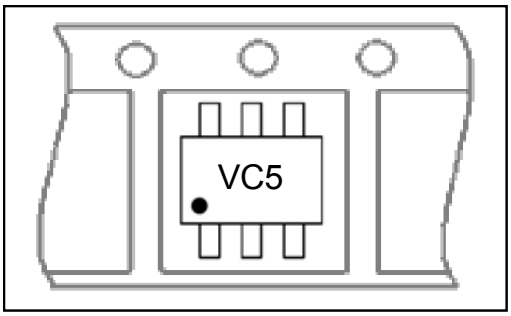


Figure 15. IEEE1394 Interface ESD Protection

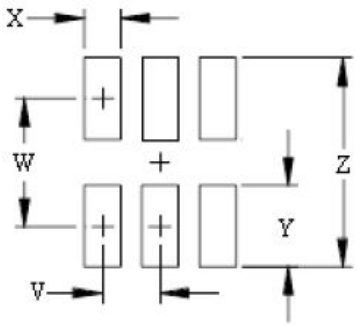
Marking & Orientation



Packaging Information

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L30ESDL5V0C6-4	3000	7	45000	90K/180K

SOT23-6L Soldering Pad Layout



Dim.	Millimeters	Inches
Z	3.60	0.141
X	0.80	0.031
W	2.60	0.102
Y	1.00	0.039
V	0.95	0.037

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