

MOSFET – Small Signal, Complementary, XLLGA6, 0.65mm x 0.90mm x 0.4mm

20 V

NTND31225CZ

Features

- Advanced Trench Complementary MOSFET
- Offers a Low $R_{DS(ON)}$ Solution in the Ultra Small 0.65 mm x 0.90 mm Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Small Signal Load Switch with Level Shift
- Analog Switch
- High Speed Interfacing
- Optimized for Power Management in Ultra Portable Products

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter			Value	Unit
V _{DSS}	Drain-to-Source Voltage		NMOS	20	V
			PMOS	−20	
V _{GSS}	Gate-to-Source Voltage		NMOS	±8	V
			PMOS	±8	
I _D	N–Channel Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	220	mA
			T _A = 85°C	158	
		t ≤ 5 s	T _A = 25°C	253	
I _D	P–Channel Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	−127	mA
			T _A = 85°C	−91	
		t ≤ 5 s	T _A = 25°C	−146	
P _D	Power Dissipation (Note 1)	Steady State	T _A = 25°C	125	mW
				t ≤ 5 s	
I _{DM}	Pulsed Drain Current	NMOS	t _p = 10 μs	846	mA
		PMOS		−488	
I _S	Source Current (Body Diode)			200	mA
				−200	
T _J , T _{STG}	Operating Junction and Storage Temperature			−55 to 150	°C
T _L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

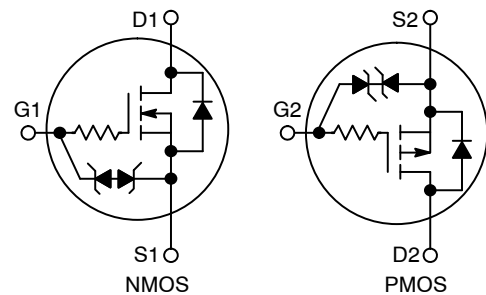
- Surface-mounted on FR4 board using the minimum recommended pad size, 1 oz Cu.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ Max}$
N-Channel 20 V	1.5 Ω @ 4.5 V	220 mA
	2.0 Ω @ 2.5 V	
	3.0 Ω @ 1.8 V	
	4.5 Ω @ 1.5 V	
P-Channel -20 V	5.0 Ω @ -4.5 V	-127 mA
	6.0 Ω @ -2.5 V	
	7.0 Ω @ -1.8 V	
	10.0 Ω @ -1.5 V	

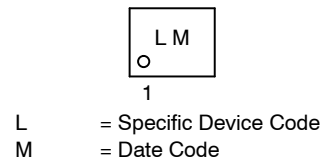


XLLGA6
Case 713AC

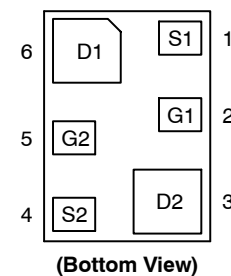
DEVICE SYMBOL



MARKING DIAGRAM



PINOUT DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

NTND31225CZ

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Junction-to-Ambient (Note 2) Steady State $t \leq 5$ s	998 751	$^{\circ}\text{C/W}$

2. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq), 1 oz copper

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	FET	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N	$V_{GS} = 0$ V, $I_D = 250$ μA	20			V
		P	$V_{GS} = 0$ V, $I_D = -250$ μA	-20			
I_{DSS}	Zero Gate Voltage Drain Current	N	$V_{GS} = 0$ V, $V_{DS} = 5$ V	$T_J = 25^{\circ}\text{C}$		50	nA
				$T_J = 85^{\circ}\text{C}$		200	
			$V_{GS} = 0$ V, $V_{DS} = 16$ V	$T_J = 25^{\circ}\text{C}$		100	
		P	$V_{GS} = 0$ V, $V_{DS} = -5$ V	$T_J = 25^{\circ}\text{C}$		-50	
				$T_J = 85^{\circ}\text{C}$		-200	
			$V_{GS} = 0$ V, $V_{DS} = -16$ V	$T_J = 25^{\circ}\text{C}$		-100	
I_{GSS}	Gate-to-Source Leakage Current	N	$V_{GS} = 0$ V, $V_{DS} = \pm 5$ V			± 100	nA
		P	$V_{GS} = 0$ V, $V_{DS} = \pm 5$ V			± 100	

ON CHARACTERISTICS

$V_{GS(TH)}$	Gate Threshold Voltage	N	$V_{GS} = V_{DS}$, $I_D = 250$ μA	0.4		1.0	V
		P	$V_{GS} = V_{DS}$, $I_D = -250$ μA	-0.4		-1.0	
$R_{DS(ON)}$	Drain-to-Source On Resistance	N	$V_{GS} = 4.5$ V, $I_D = 100$ mA		0.8	1.5	Ω
			$V_{GS} = 2.5$ V, $I_D = 50$ mA		1.1	2.0	
			$V_{GS} = 1.8$ V, $I_D = 20$ mA		1.4	3.0	
			$V_{GS} = 1.5$ V, $I_D = 10$ mA		1.8	4.5	
		P	$V_{GS} = -4.5$ V, $I_D = -100$ mA		2.1	5.0	
			$V_{GS} = -2.5$ V, $I_D = -50$ mA		2.7	6.0	
			$V_{GS} = -1.8$ V, $I_D = -20$ mA		3.6	7.0	
			$V_{GS} = -1.5$ V, $I_D = -10$ mA		4.2	10.0	
g_{FS}	Forward Transconductance	N	$V_{DS} = 5$ V, $I_D = 125$ mA		0.48		S
		P	$V_{DS} = -5$ V, $I_D = -125$ mA		0.35		
V_{SD}	Forward Diode Voltage	N	$V_{GS} = 0$ V, $I_S = 10$ mA		0.6	1.0	V
		P	$V_{GS} = 0$ V, $I_S = -10$ mA		-0.6	-1.0	

CAPACITANCES

C_{ISS}	Input Capacitance	N	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = 15$ V		12.3		pF
C_{OSS}	Output Capacitance				3.4		
C_{RSS}	Reverse Capacitance				2.5		
C_{ISS}	Input Capacitance	P	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = -15$ V		12.8		
C_{OSS}	Output Capacitance				2.8		
C_{RSS}	Reverse Capacitance				2.0		

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified) (continued)

Symbol	Parameter	FET	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$

$t_{d(ON)}$	Turn-On Delay Time	N	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 200\text{ mA}, R_G = 2\ \Omega$		16.5		ns
t_r	Rise Time				25.5		
$t_{d(OFF)}$	Turn-Off Delay Time				142		
t_f	Fall Time				80		
$t_{d(ON)}$	Turn-On Delay Time	P	$V_{GS} = -4.5\text{ V}, V_{DS} = -15\text{ V},$ $I_D = -200\text{ mA}, R_G = 2\ \Omega$		37		
t_r	Rise Time				71		
$t_{d(OFF)}$	Turn-Off Delay Time				280		
t_f	Fall Time				171		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS – P-CHANNEL

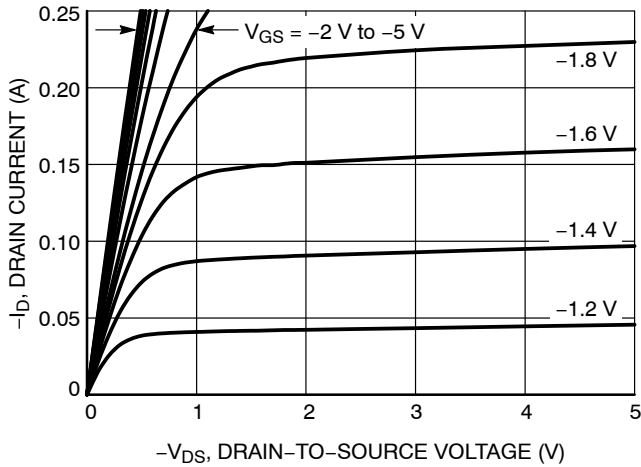


Figure 1. On-Region Characteristics

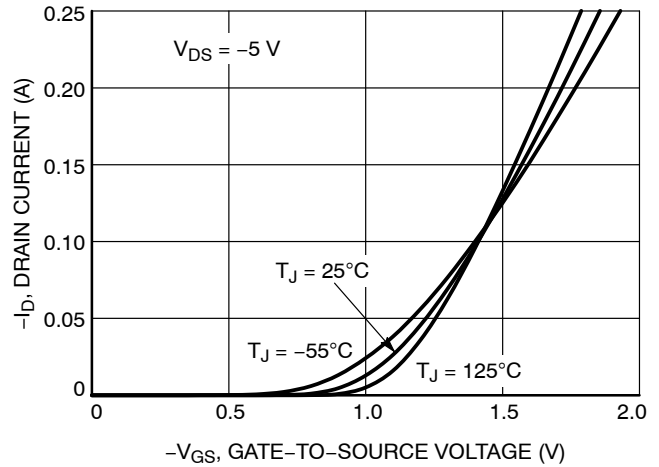


Figure 2. Transfer Characteristics

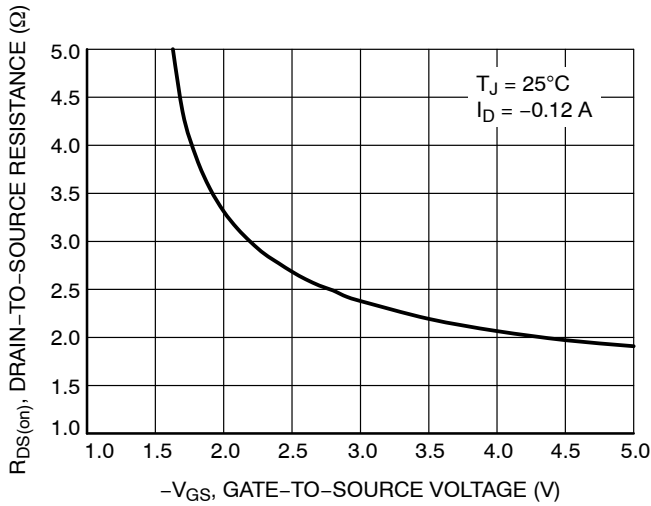


Figure 3. On-Resistance vs. Gate-to-Source Voltage

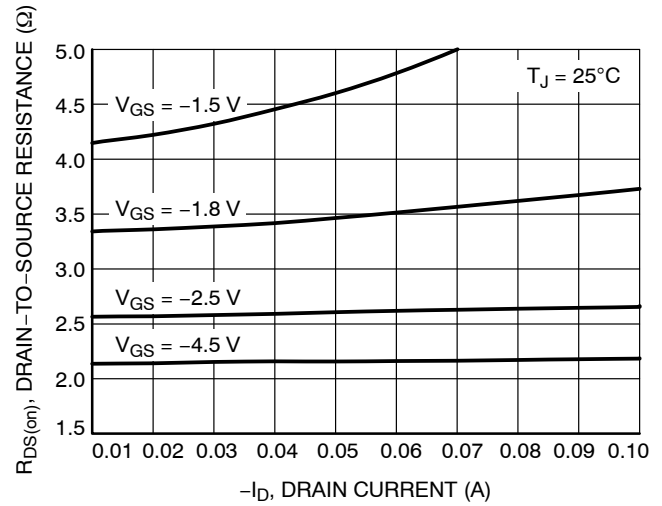


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

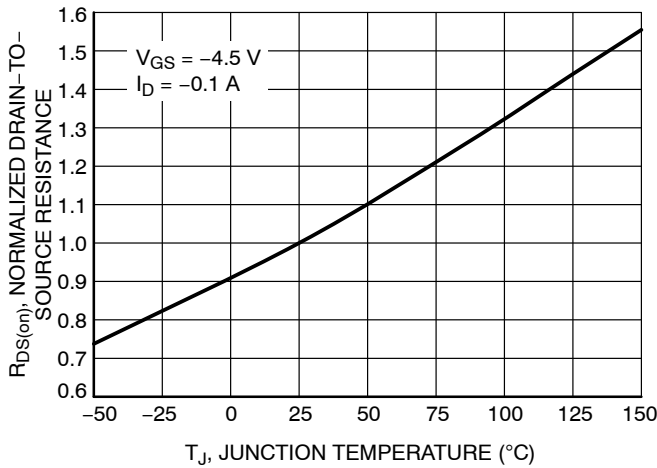


Figure 5. On-Resistance Variation with Temperature

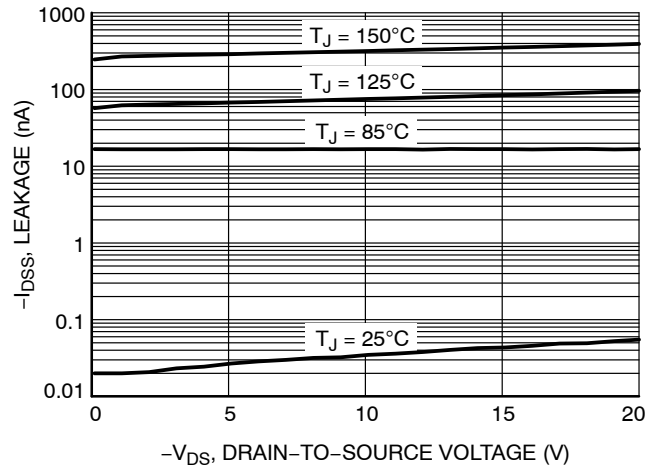


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – P-CHANNEL (continued)

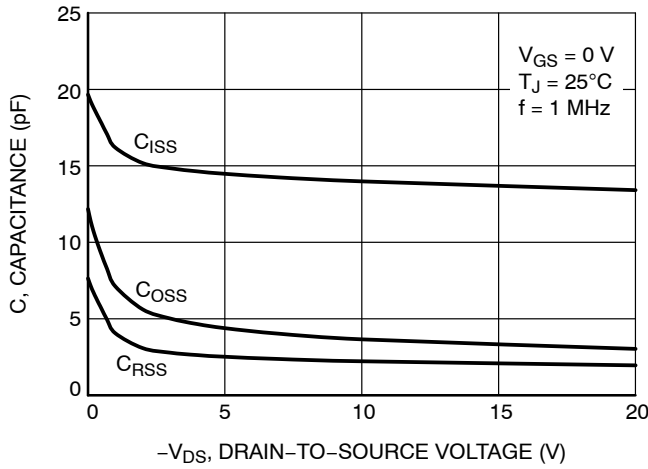


Figure 7. Capacitance Variation

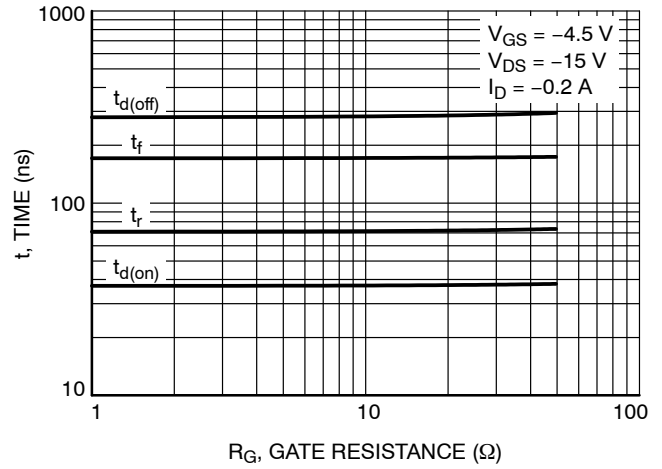


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

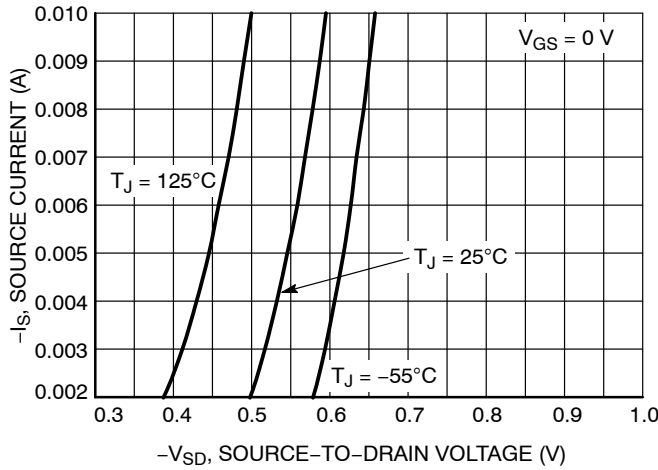


Figure 9. Diode Forward Voltage vs. Current

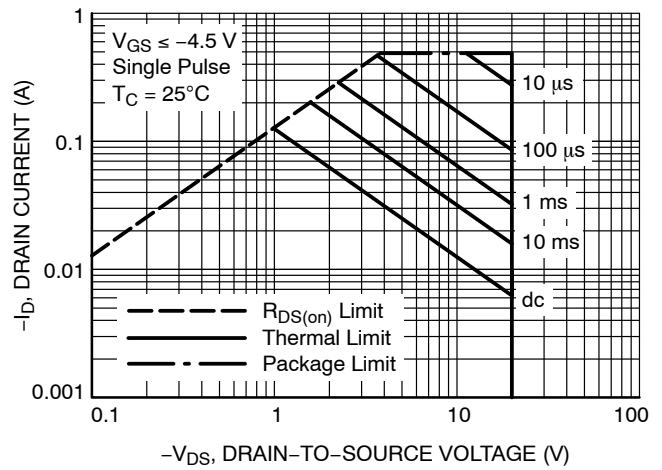


Figure 10. Maximum Rated Forward Biased Safe Operating Area

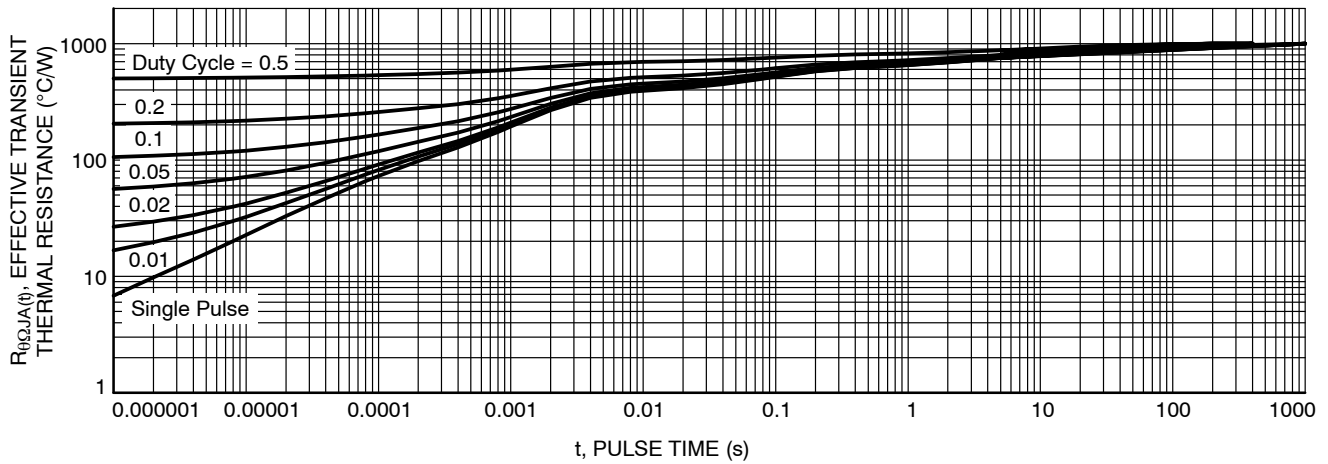


Figure 11. Thermal Response

TYPICAL CHARACTERISTICS – N-CANNEL

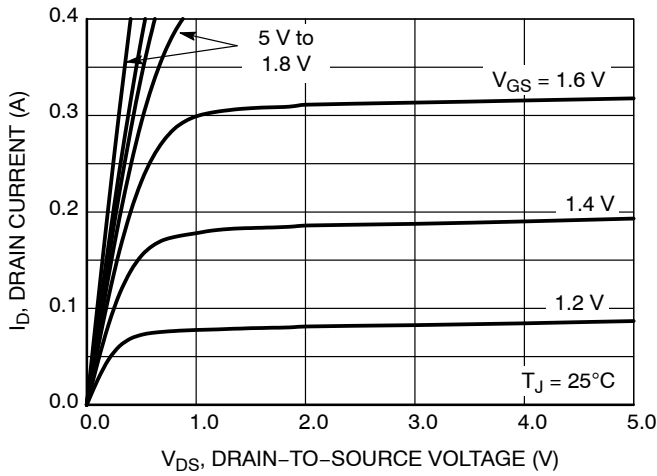


Figure 12. On-Region Characteristics

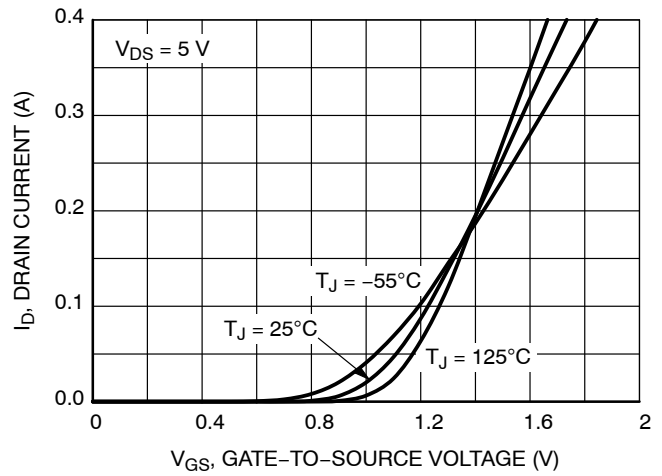


Figure 13. Transfer Characteristics

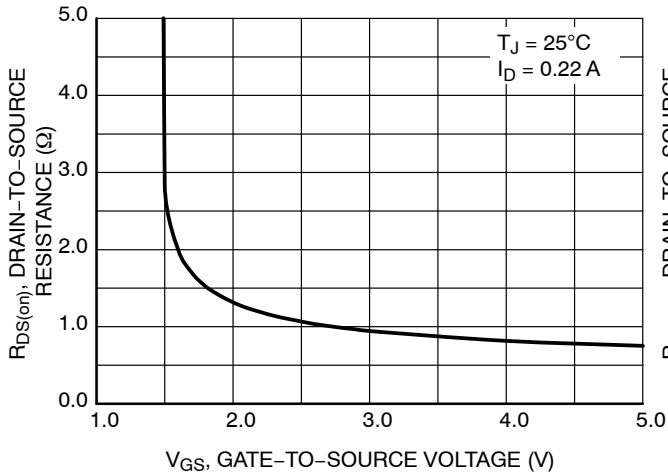


Figure 14. On-Resistance vs. Gate-to-Source Voltage

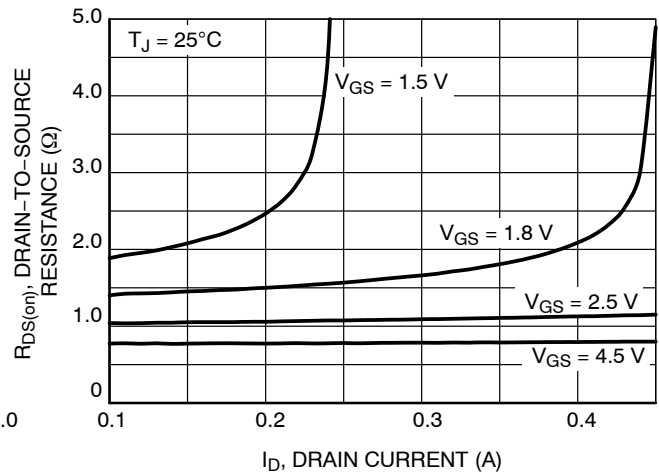


Figure 15. On-Resistance vs. Drain Current and Gate Voltage

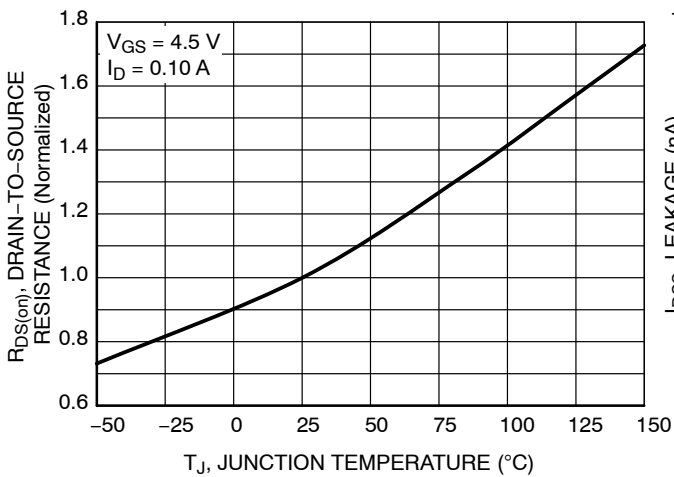


Figure 16. On-Resistance Variation with Temperature

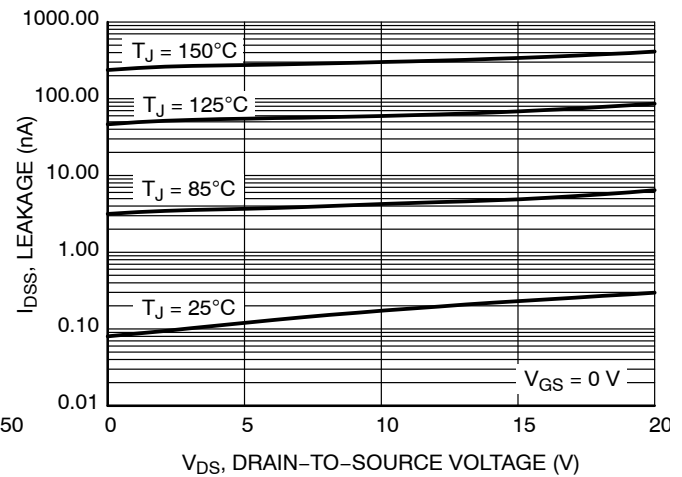


Figure 17. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS – N-CHANNEL (continued)

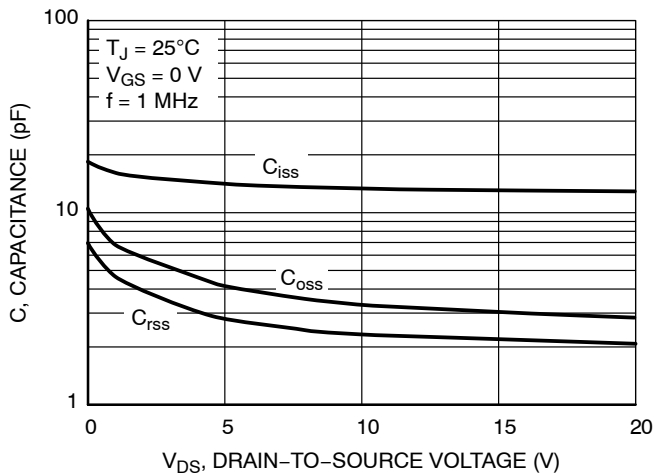


Figure 18. Capacitance Variation

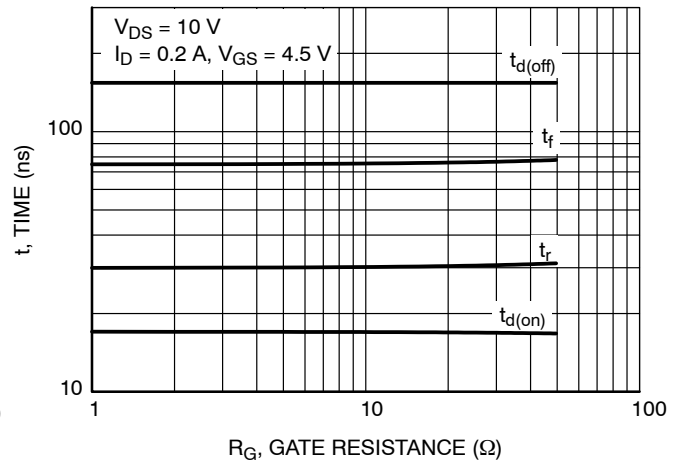


Figure 19. Resistive Switching Time Variation vs. Gate Resistance

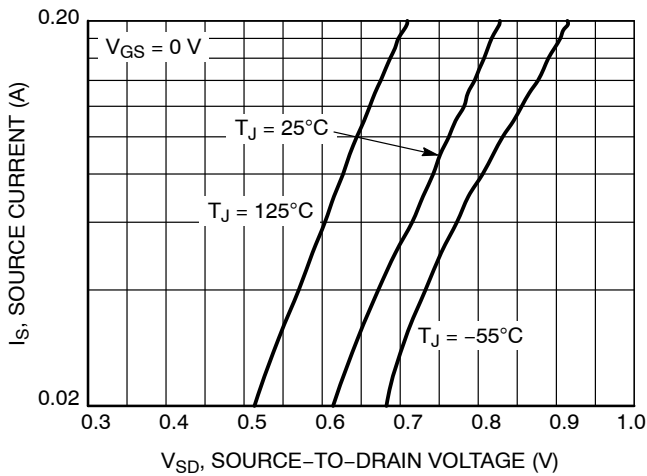


Figure 20. Diode Forward Voltage vs. Current

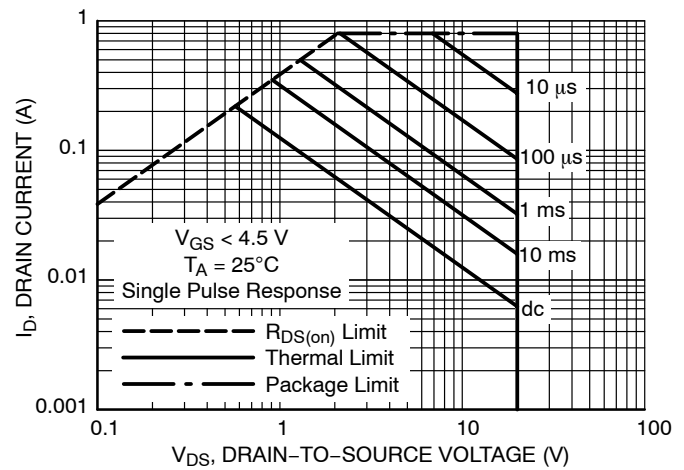


Figure 21. Maximum Rated Forward Biased Safe Operating Area

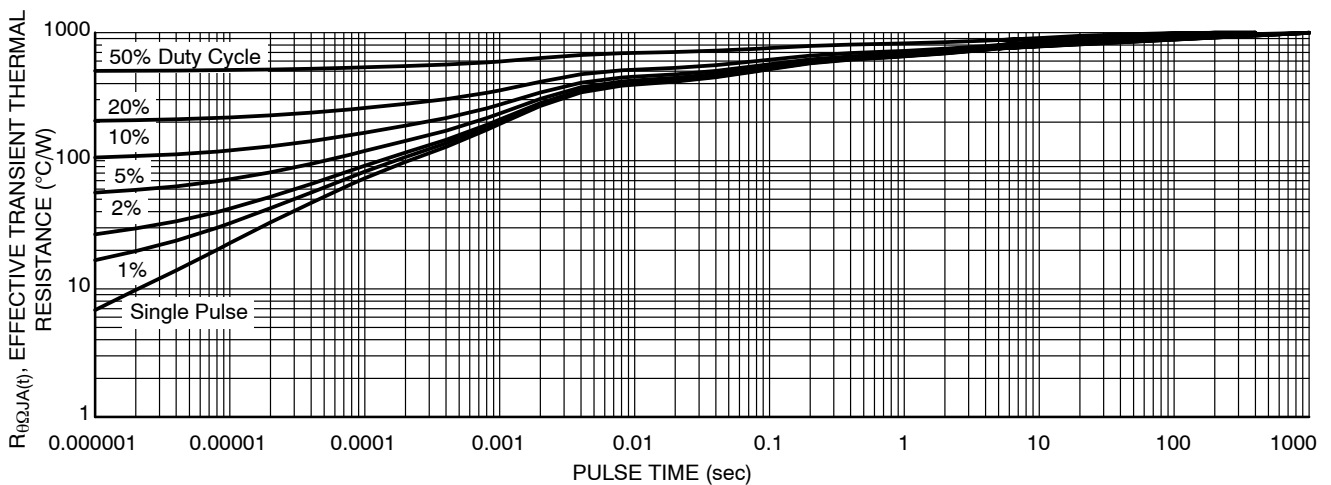


Figure 22. Thermal Response

NTND31225CZ

ORDERING INFORMATION

Device	Package	Shipping†
NTND31225CZTAG	XLLGA6 (Pb-Free)	8,000 / Tape & Reel

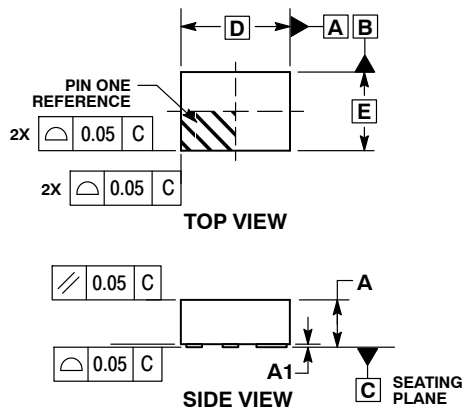
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



SCALE 8:1

XLLGA6 0.90x0.65
CASE 713AC
ISSUE O

DATE 19 JUN 2014



NOTES:

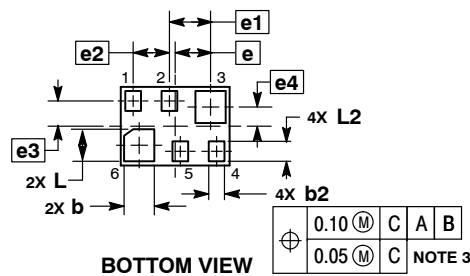
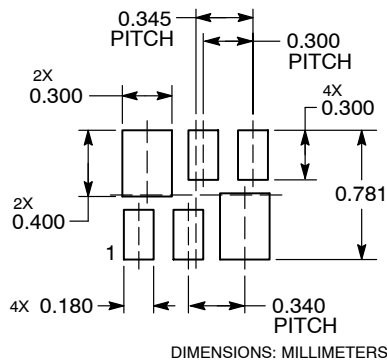
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. POSITIONAL TOLERANCE APPLIES TO ALL SIX LEADS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.340	0.440
A1	0.000	0.050
b	0.200	0.300
b2	0.080	0.180
D	0.900 BSC	
E	0.650 BSC	
e	0.295 BSC	
e1	0.340 BSC	
e2	0.300 BSC	
e3	0.208 BSC	
e4	0.158 BSC	
L	0.215	0.315
L2	0.115	0.215

GENERIC MARKING DIAGRAM*


- X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.


RECOMMENDED SOLDERING FOOTPRINT*


*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, [SOLDDRRM/D](#).

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DESCRIPTION:	XLLGA6 0.90X0.65	PAGE 1 OF 1

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