

MOSFET - Power, Single N-Channel, DFNW8, DUAL COOL®

80 V, 1.56 mΩ, 287 A

NTMTSC1D5N08MC

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	80	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	I_D	287	A
Power Dissipation $R_{\theta JC}$ (Note 2)			
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	I_D	33	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			
Pulsed Drain Current	I_{DM}	3500	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to $+150$	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 31$ A, $L = 3$ mH)	E_{AS}	1441	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

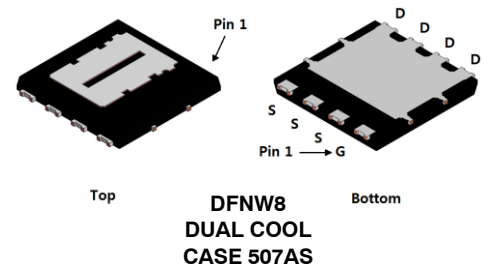
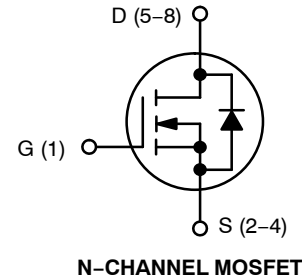
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

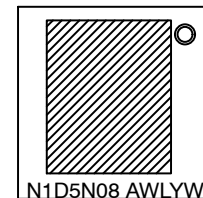
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.5	$^\circ\text{C}/\text{W}$
Junction-to-Top Source – Steady State (Note 2)	$R_{\theta JC}$	0.8	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	38	

1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	1.56 mΩ @ 10 V	287 A
	4.0 mΩ @ 6 V	



MARKING DIAGRAM



N1D5N08 = Specific Device Code
A = Assembly Location
WL = 2-digit Wafer Lot Code
Y = Year Code
W = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTMTSC1D5N08MC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 250 μA, ref to 25°C		82		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 80 V	T _J = 25°C		1	μA
			T _J = 125°C		250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 650 μA	2.0	3.0	4.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 650 μA, ref to 25°C		-8.3		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 80 A		1.10	1.56	mΩ
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 6 V, I _D = 58 A		1.75	4.0	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 80 A		219		S
Gate Resistance	R _G	T _A = 25°C		0.9		Ω

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 40 V		7420	10,400	pF
Output Capacitance	C _{OSS}			2555	3600	
Reverse Transfer Capacitance	C _{RSS}			101	175	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 40 V; I _D = 80 A		101	140	nC
Threshold Gate Charge	Q _{G(TH)}			20	28	
Gate-to-Source Charge	Q _{GS}			32		
Gate-to-Drain Charge	Q _{GD}			21		
Output Charge	Q _{OSS}			141		
Sync Charge	Q _{sync}			82		
Plateau Voltage	V _{plateau}			5		V

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 40 V, I _D = 80 A, R _G = 6 Ω		30		ns
Rise Time	t _r			24		
Turn-Off Delay Time	t _{d(OFF)}			69		
Fall Time	t _f			31		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2 A		0.7	1.2	V
		V _{GS} = 0 V, I _S = 80 A		0.8	1.3	
Reverse Recovery Time	t _{RR}	I _F = 40 A, di/dt = 300 A/μs		39	62	ns
Reverse Recovery Charge	Q _{RR}			89	142	nC
Reverse Recovery Time	t _{RR}	I _F = 40 A, di/dt = 1000 A/μs		31	50	ns
Reverse Recovery Charge	Q _{RR}			209	335	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

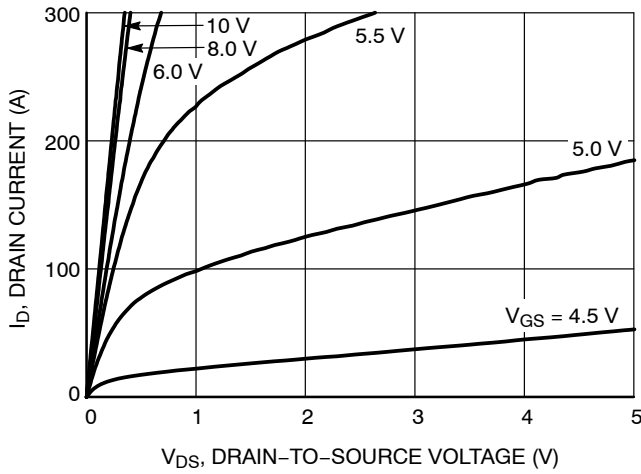


Figure 1. On-Region Characteristics

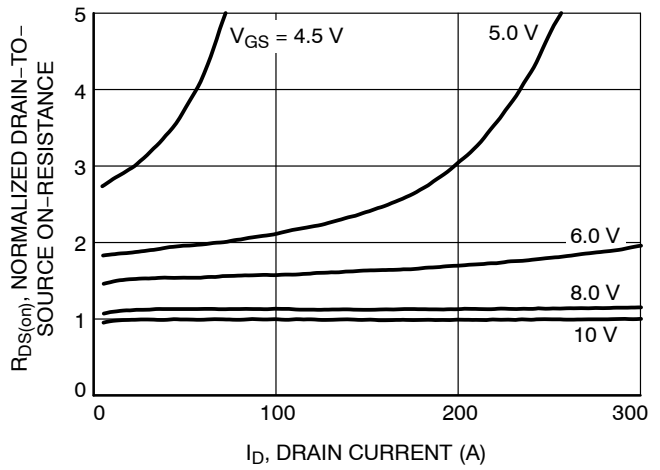


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

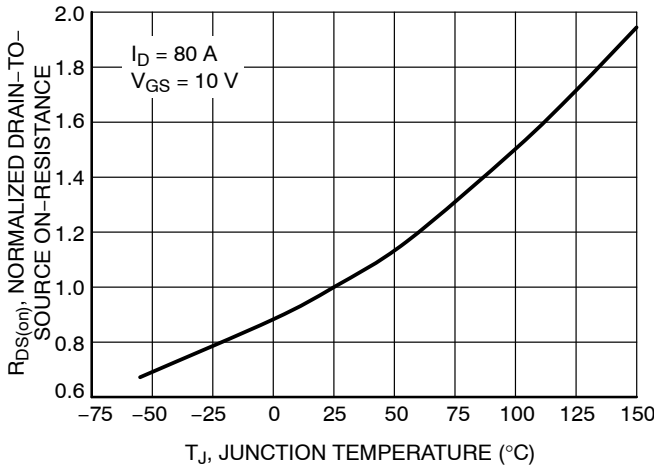


Figure 3. Normalized On Resistance vs. Junction Temperature

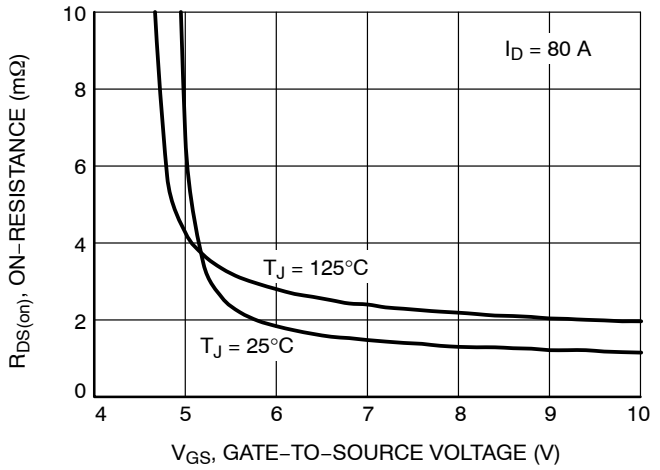


Figure 4. On-Resistance vs. Gate-to-Source Voltage

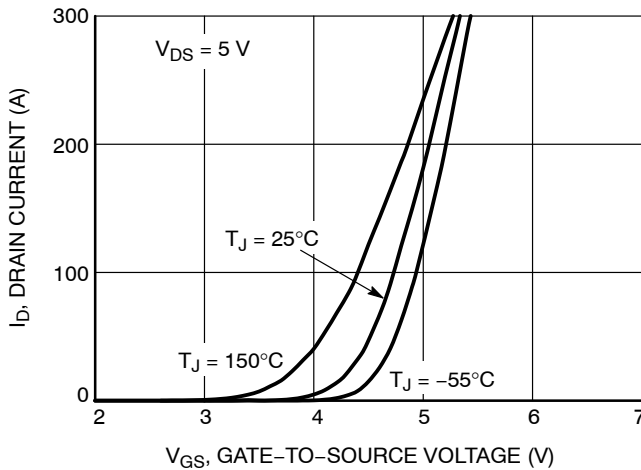


Figure 5. Transfer Characteristics

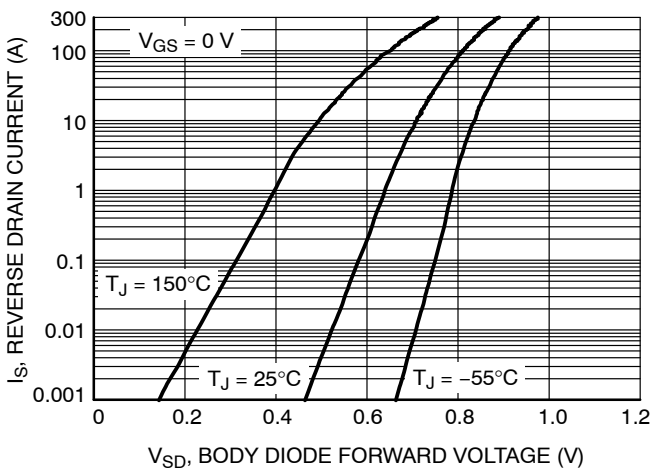


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

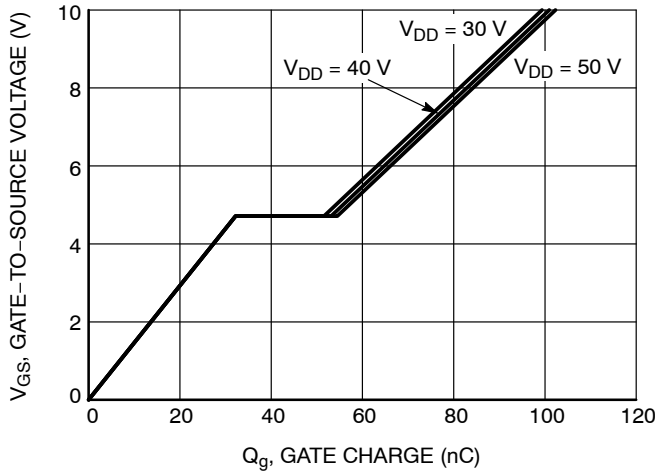


Figure 7. Gate Charge Characteristics

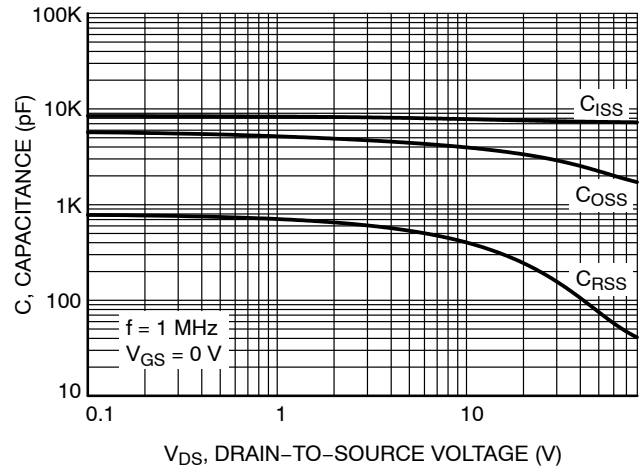


Figure 8. Capacitance vs. Drain-to-Source Voltage

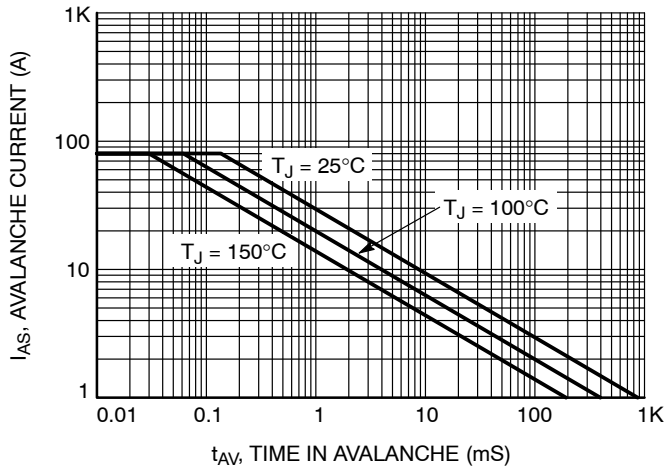


Figure 9. Unclamped Inductive Switching Capability

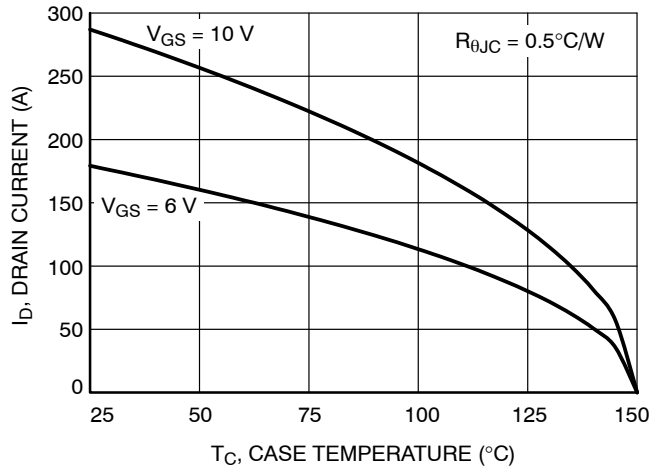


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

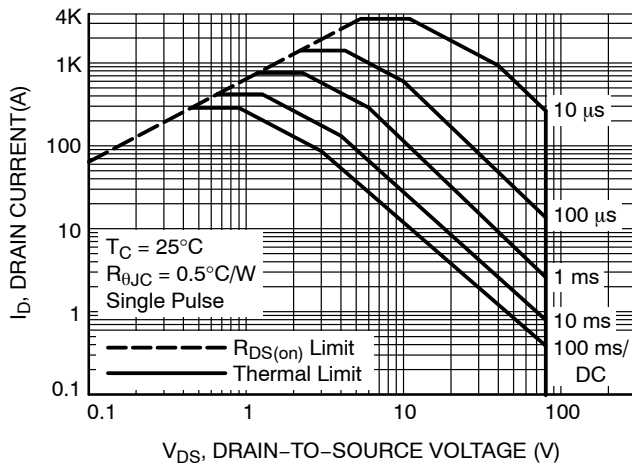


Figure 11. Forward Biased Safe Operating Area

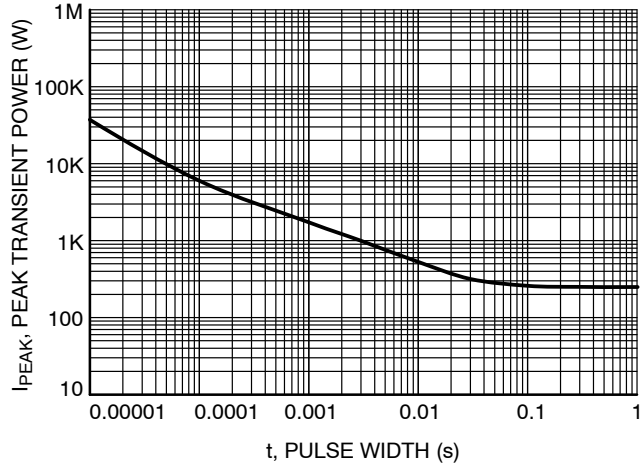


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS

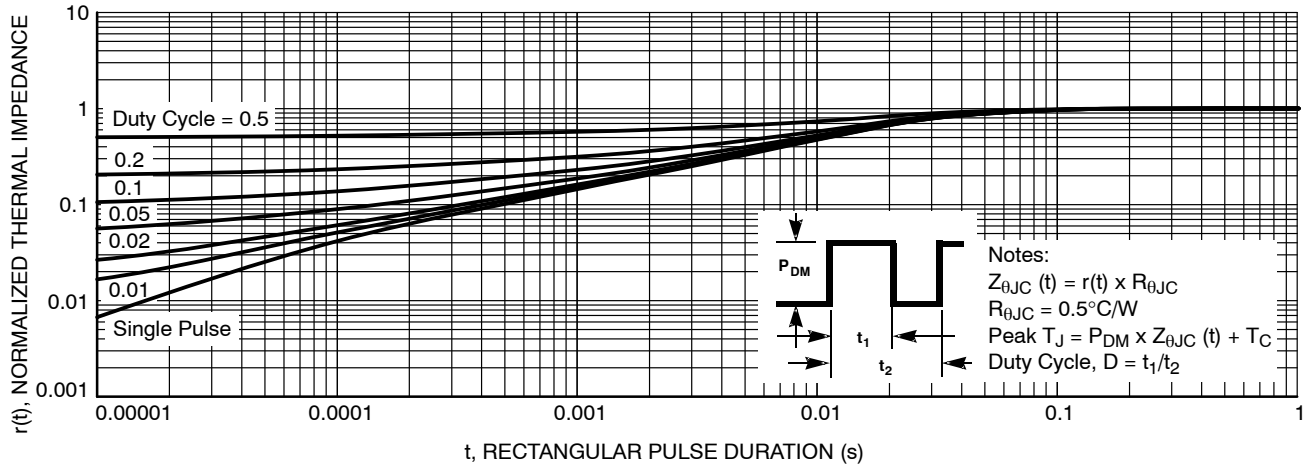
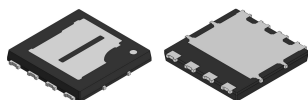


Figure 13. Transient Thermal Impedance

DEVICE ORDERING INFORMATION

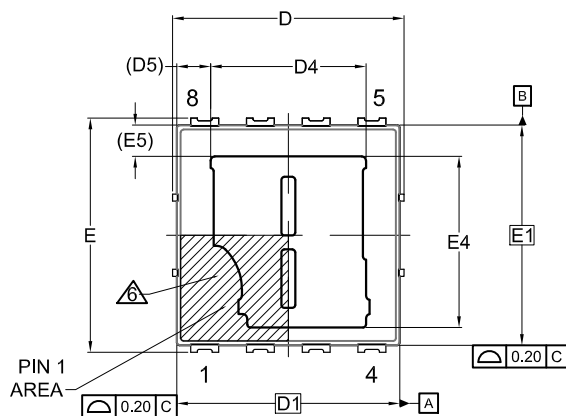
Device	Marking	Package	Shipping [†]
NTMTSC1D5N08MC	N1D5N08	DFNW8 DUAL COOL (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



TDFNW8 8.30x8.40x0.92, 2.00P
CASE 507AS
ISSUE C

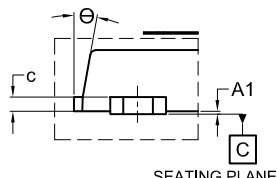
DATE 28 MAY 2024



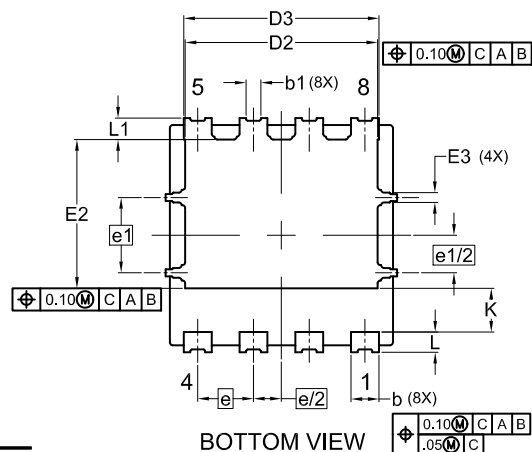
TOP VIEW



SEE DETAIL A FRONT VIEW



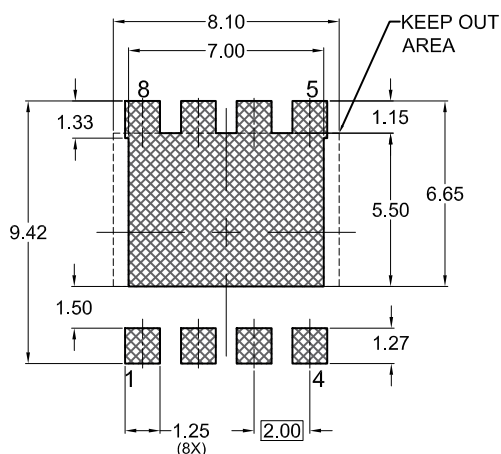
DETAIL A
(SCALE: 2X)



BOTTOM VIEW

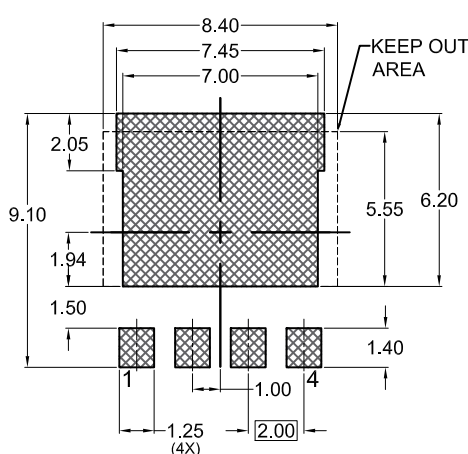
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS.
"A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. SLOT PARTITION IS OPTIONAL.



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL. SOLDERRM/D.



UNIVERSAL LAND PATTERN*

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.82	0.92	1.02
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	8.00 BSC		
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
D4	5.52	5.67	5.82
D5	1.16 REF		
E	8.30	8.40	8.50
E1	7.90 BSC		
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
E4	6.08	6.23	6.38
E5	1.13 REF		
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	—	12°

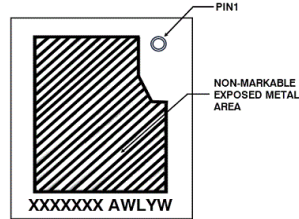
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TDFNW8 8.30x8.40x0.92, 2.00P
CASE 507AS
ISSUE C

DATE 28 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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