

NRVBD1035CTL

Switch-mode Schottky Power Rectifier

DPAK Power Surface Mount Package

The NRVBD1035CTL employs the Schottky Barrier principle in a large area metal-to-silicon power diode. State of the art geometry features epitaxial construction with oxide passivation and metal overlay contact. Ideally suited for low voltage, high frequency switching power supplies, free wheeling diode and polarity protection diodes.

Features

- Highly Stable Oxide Passivated Junction
- Guardring for Stress Protection
- Matched Dual Die Construction –
May be Paralleled for High Current Output
- High dv/dt Capability
- Short Heat Sink Tap Manufactured – Not Sheared
- Very Low Forward Voltage Drop
- Epoxy Meets UL 94 V-0 @ 0.125 in
- This is a Pb-Free Device

Mechanical Characteristics:

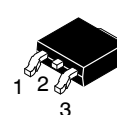
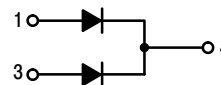
- Case: Epoxy, Molded
- Weight: 0.4 Gram (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead and Mounting Surface Temperature for Soldering Purposes: 260°C Max. for 10 Seconds



ON Semiconductor®

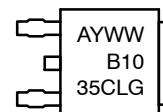
www.onsemi.com

SCHOTTKY BARRIER RECTIFIER 10 AMPERES 35 VOLTS



**DPAK
CASE 369C**

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
B1035CL	= Device Code
G	= Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NRVBD1035CTL

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	35	V
Average Rectified Forward Current (At Rated V_R , $T_C = 115^\circ\text{C}$)	I_O	5.0 10	A
Peak Repetitive Forward Current (At Rated V_R , Square Wave, 20 kHz, $T_C = 115^\circ\text{C}$)	I_{FRM}	10	A
Non-Repetitive Peak Surge Current (Surge applied at rated load conditions, halfwave, single phase, 60 Hz)	I_{FSM}	50	A
Storage / Operating Case Temperature	T_{stg}, T_c	-55 to +150	$^\circ\text{C}$
Operating Junction Temperature (Note 1)	T_J	-55 to +150	$^\circ\text{C}$
Voltage Rate of Change (Rated V_R , $T_J = 25^\circ\text{C}$)	dv/dt	10,000	V/ μs

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The heat generated must be less than the thermal conductivity from Junction-to-Ambient: $dP_D/dT_J < 1/R_{\theta JA}$.

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	Per Leg	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient (Note 2)	Per Leg	$R_{\theta JA}$	137	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS

Maximum Instantaneous Forward Voltage (Note 3) (See Figure 2) $I_F = 5$ Amps, $T_J = 25^\circ\text{C}$ $I_F = 5$ Amps, $T_J = 100^\circ\text{C}$ $I_F = 10$ Amps, $T_J = 25^\circ\text{C}$ $I_F = 10$ Amps, $T_J = 100^\circ\text{C}$	Per Leg	V_F	0.47 0.41 0.56 0.55	V
Maximum Instantaneous Reverse Current (Note 3) (See Figure 4) $(V_R = 35\text{ V}, T_J = 25^\circ\text{C})$ $(V_R = 35\text{ V}, T_J = 100^\circ\text{C})$ $(V_R = 17.5\text{ V}, T_J = 25^\circ\text{C})$ $(V_R = 17.5\text{ V}, T_J = 100^\circ\text{C})$	Per Leg	I_R	2.0 30 0.20 5.0	mA

2. Rating applies when using minimum pad size, FR4 PC Board

3. Pulse Test: Pulse Width $\leq 250\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

ORDERING INFORMATION

Device	Package	Shipping [†]
NRVBD1035CTLT4G	DPAK (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

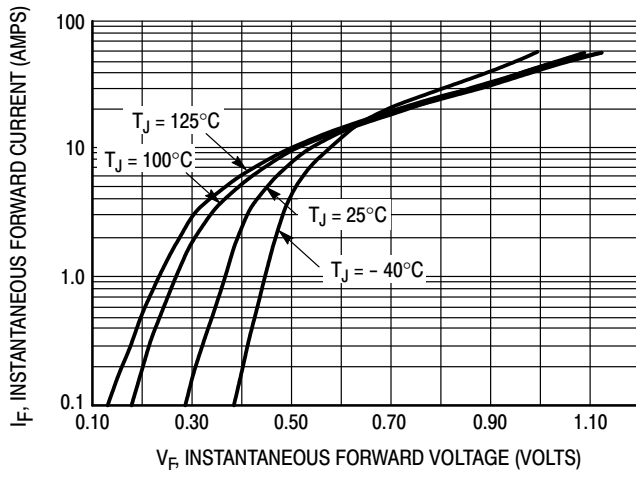


Figure 1. Typical Forward Voltage Per Leg

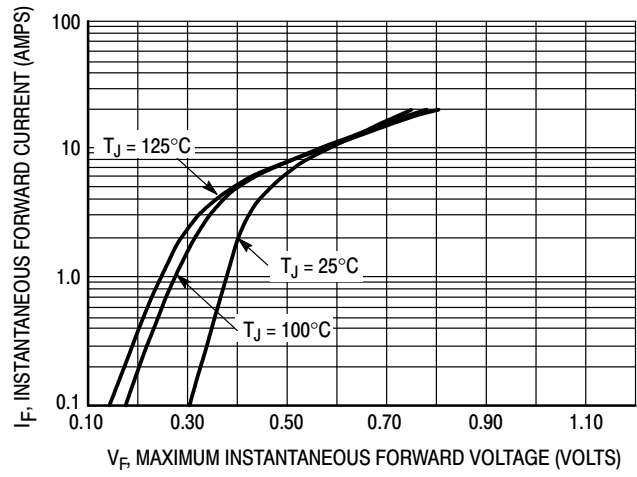


Figure 2. Maximum Forward Voltage Per Leg

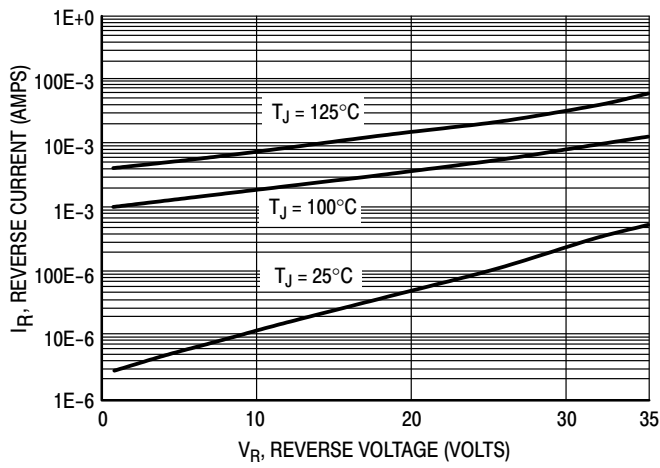


Figure 3. Typical Reverse Current Per Leg

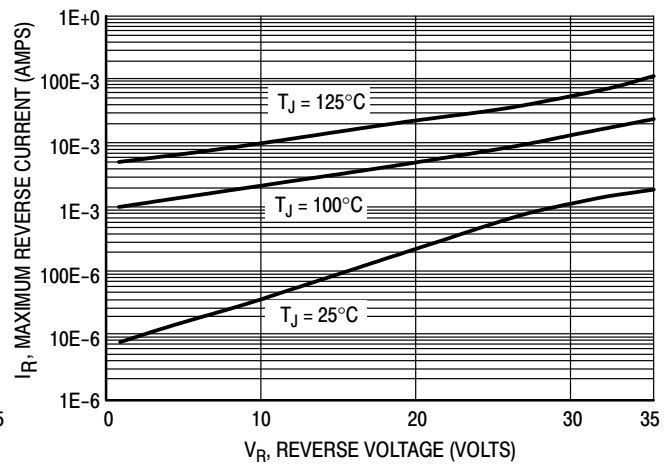


Figure 4. Maximum Reverse Current Per Leg

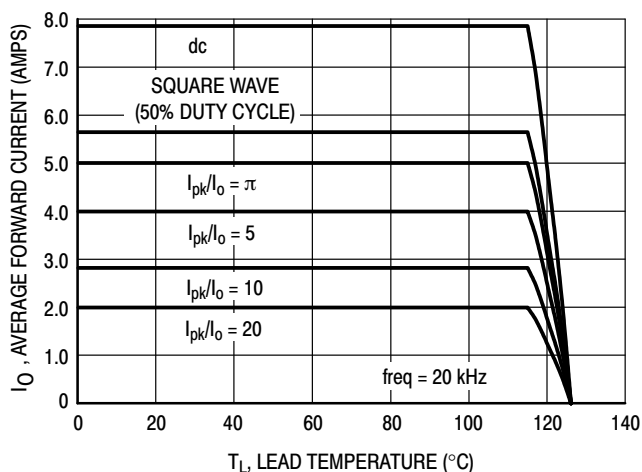


Figure 5. Current Derating Per Leg

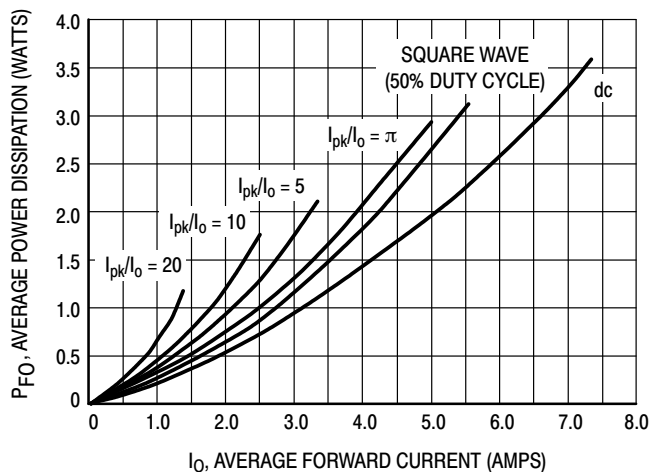


Figure 6. Forward Power Dissipation Per Leg

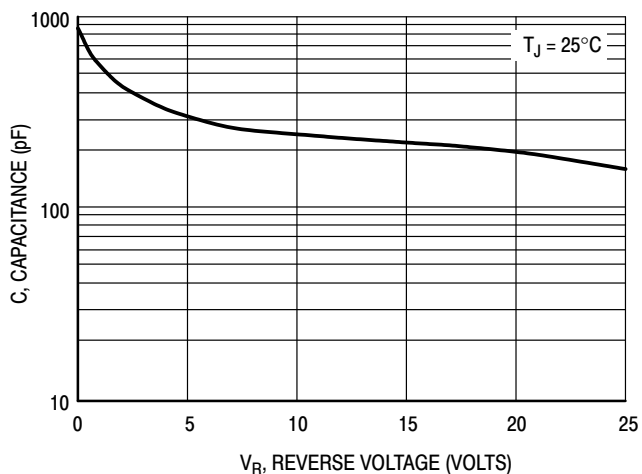


Figure 7. Capacitance Per Leg

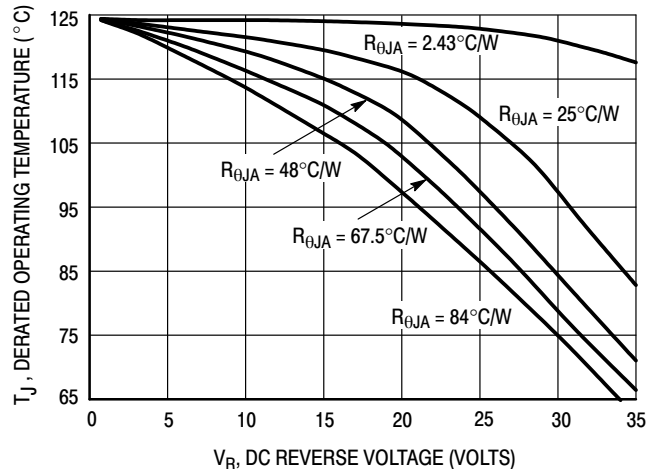


Figure 8. Typical Operating Temperature Derating Per Leg *

* Reverse power dissipation and the possibility of thermal runaway must be considered when operating this device under any reverse voltage conditions. Calculations of T_J therefore must include forward and reverse power effects. The allowable operating T_J may be calculated from the equation:

$$T_J = T_{Jmax} - r(t)(P_f + P_r) \text{ where}$$

$r(t)$ = thermal impedance under given conditions,
 P_f = forward power dissipation, and
 P_r = reverse power dissipation

This graph displays the derated allowable T_J due to reverse bias under DC conditions only and is calculated as $T_J = T_{Jmax} - r(t)P_r$, where $r(t) = R_{\theta JA}$. For other power applications further calculations must be performed.

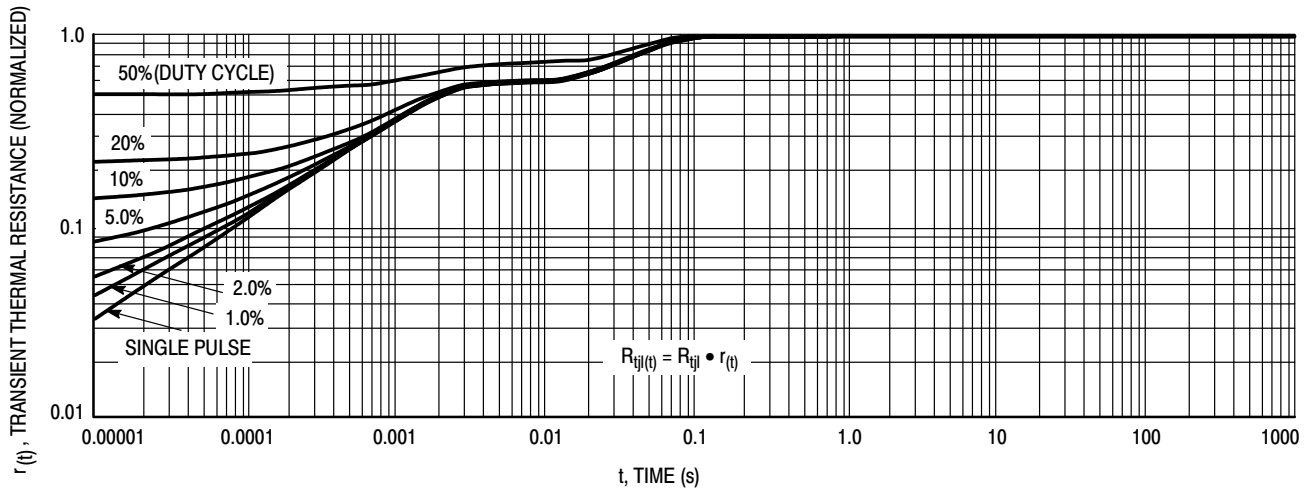


Figure 9. Thermal Response Junction to Case (Per Leg)

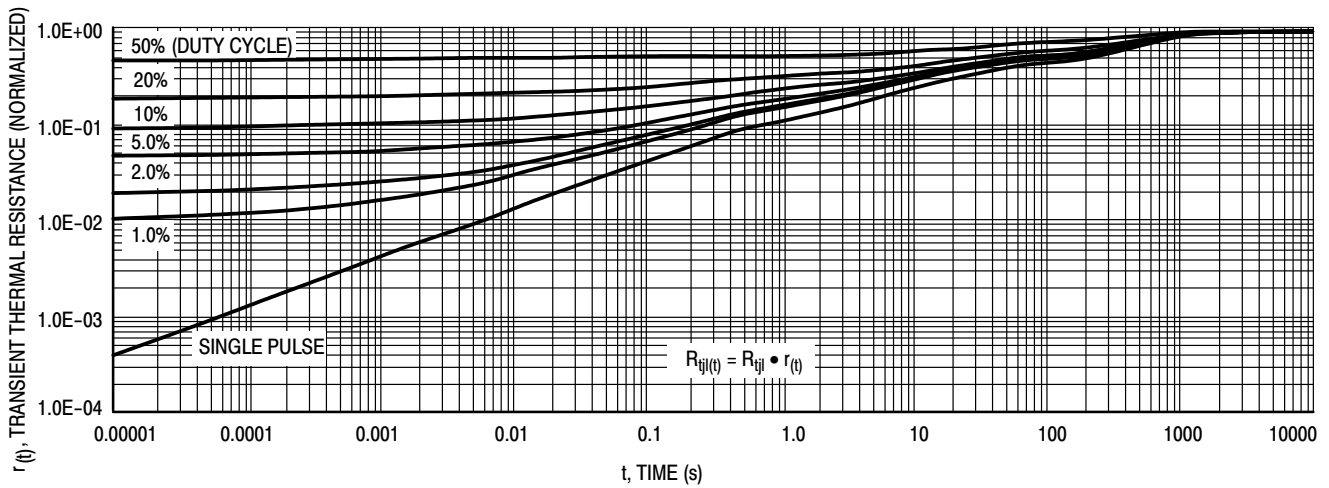
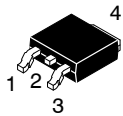


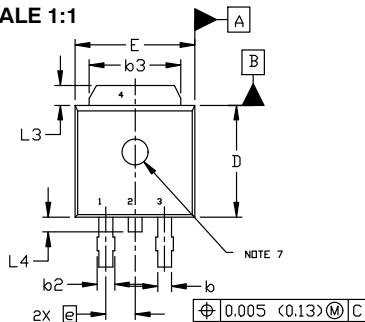
Figure 10. Thermal Response Junction to Ambient (Per Leg)



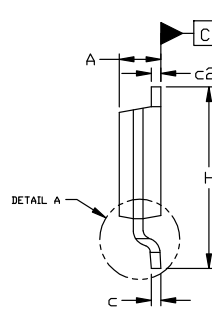
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

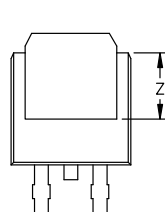
SCALE 1:1



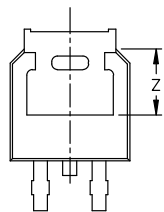
TOP VIEW



SIDE VIEW

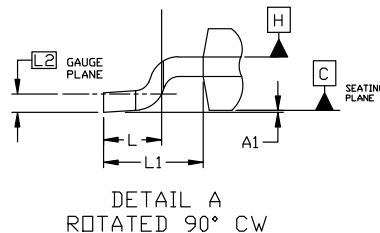
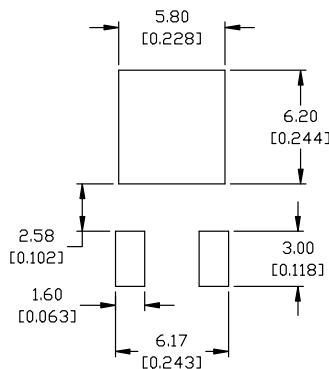


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE
CONSTRUCTIONS



DETAIL A
ROTATED 90° CW

NOTES:

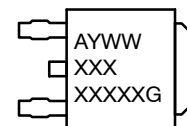
1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---

GENERIC
MARKING DIAGRAM*



IC



Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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