

1.Description

This N-channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

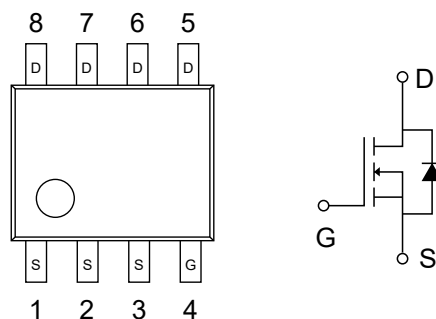
2.Features

- $V_{DS(V)}=30V$
- $I_D=8.5A$
- $R_{DS(ON)}<23m\Omega(V_{GS}=10V)$
- $R_{DS(ON)}<30m\Omega(V_{GS}=4.5V)$
- Low gate charge

2.Pinning information

Pin	Symbol	Description
4	G	GATE
1,2,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



3.Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Rating	Units
Drain to Source Voltage	V_{DS}	30	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current Continuous	I_D	8.5	A
Pulsed (Note 1a)		40	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	32	mJ
Power dissipation	P_D	2.5	W
Derate above $25^{\circ}C$		20	$^{\circ}C/W$
Storage Temperature	T_J, T_{STG}	-55 to 150	$^{\circ}C$



4.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient (Note 1a)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JA}$	25	°C/W



5. Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

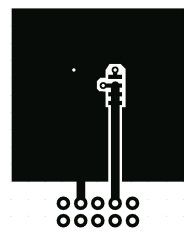
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	$I_D=250\mu\text{A}$ Referenced to 25°C		23		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$			1	μA
		$T_J=125^\circ\text{C}$			250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20\text{V}$			± 100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.2	1.7	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	$I_D=250\mu\text{A}$ Referenced to 25°C		-4.9		mV/ $^\circ\text{C}$
Drain to Source On Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=8.5\text{A}$		19	23	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=7.5\text{A}$		23	30	m Ω
		$V_{GS}=10\text{V}$, $I_D=8.5\text{A}$, $T_J=125^\circ\text{C}$		26	32	m Ω
Input Capacitance	C_{iss}	$V_{DS}=15\text{V}$		475	635	pF
Output Capacitance	C_{oss}	$V_{GS}=0\text{V}$		100	135	pF
Reverse Transfer Capacitance	C_{rss}	$f=1\text{MHz}$		65	100	pF
Gate Resistance	R_G	$f=1\text{MHz}$		0.9	1.6	Ω
Turn-On DelayTime	$t_{D(on)}$	$V_{DD}=15\text{V}$, $I_D=8.5\text{A}$ $V_{GS}=10\text{V}$, $R_{GS}=33\Omega$		5	10	ns
Rise Time	t_r			9	18	ns
Turn-Off DelayTime	$t_{D(off)}$			42	68	ns
Fall Time	t_f			21	34	ns
Total Gate Charge	Q_g	$V_{DS}=15\text{V}$, $I_D=8.5\text{A}$, $V_{GS}=10\text{V}$		9.2	13	nC
Total Gate Charge	Q_g	$V_{DS}=15\text{V}$, $I_D=8.5\text{A}$ $V_{GS}=5\text{V}$		5	7	nC
Gate to Source Gate Charge	Q_{gs}			1.5		nC
Gate to Drain Charge	Q_{gd}			2		nC
Source to Drain Diode Voltage	V_{SD}	$I_{SD}=8.5\text{A}$		0.9	1.25	V
		$I_{SD}=2.1\text{A}$		0.8	1	V



Reverse Recovery Time	t_{rr}	$I_F=8.5A, d_{IF}/d_t=100A/\mu s$			33	nS
Reverse Recovery Charge	Q_{rr}				20	nC

Notes:

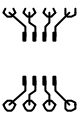
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1in² pad of 2 oz copper



b) 105° C/W when mounted on a 0.4 in² pad of 2 oz. copper.



c) 125° C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2: Starting $T_J=25^{\circ}C$, $L=1mH$, $I_{AS}=8A$, $V_{DD}=27V$, $V_{GS}=10V$.

3: Pulse Test:Pulse Width <300μs, Duty Cycle <2%.



6.1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

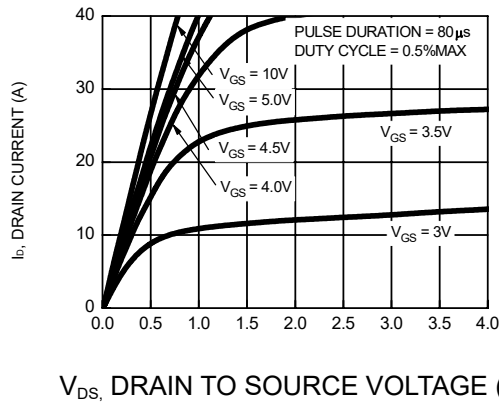


Figure 1: On-Region Characteristics.

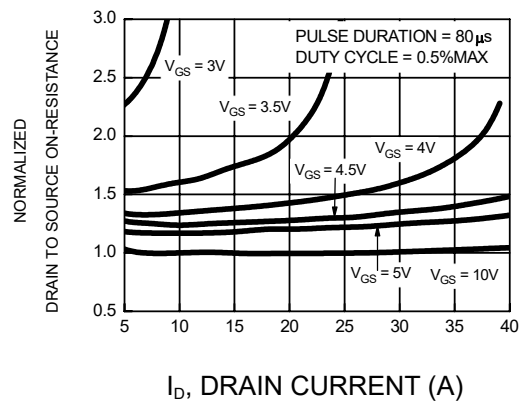


Figure 2: On-Resistance Variation with Drain Current and Gate Voltage.

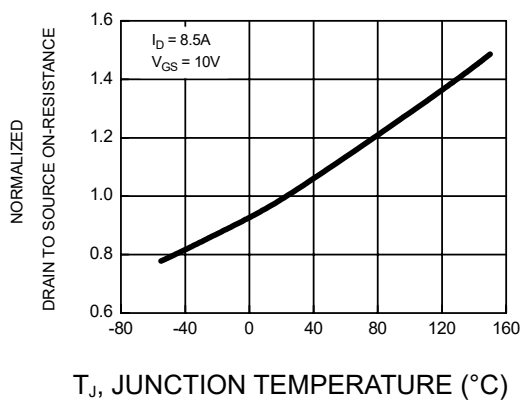


Figure 3: On-Resistance Variation with Temperature.

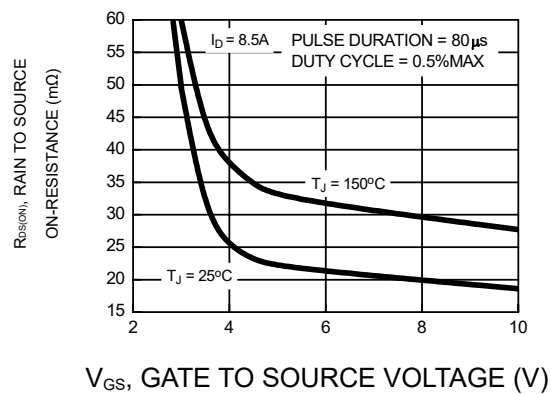


Figure 4: On-Resistance Variation with Gate-to-Source Voltage.

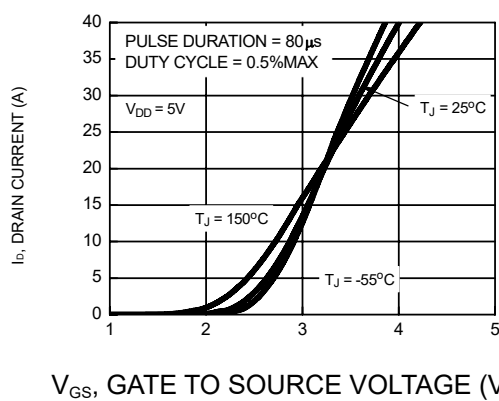


Figure 5: Transfer Characteristics.

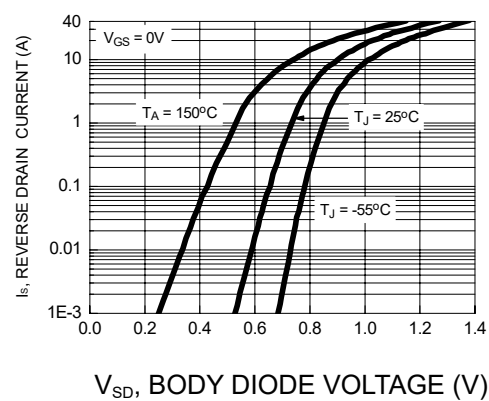


Figure 6: Source to Drain Diode Forward Voltage vs Source Current.



6.2 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

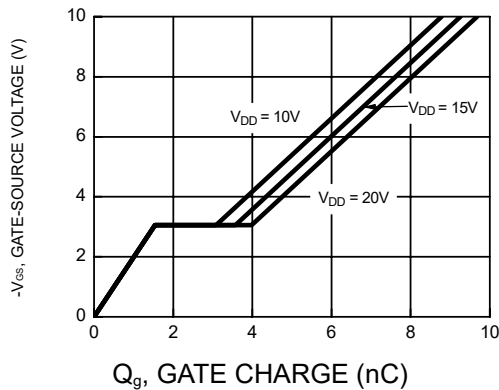


Figure 7: Gate-Charge Characteristics.

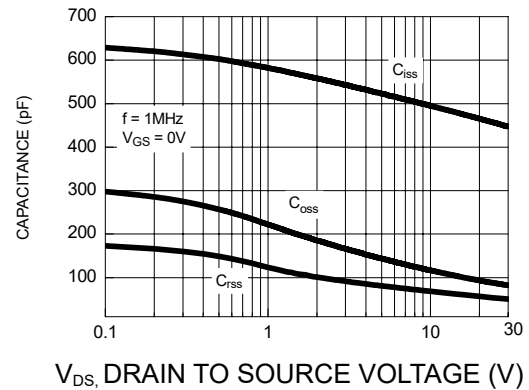


Figure 8: Capacitance vs Drain to Source Voltage.

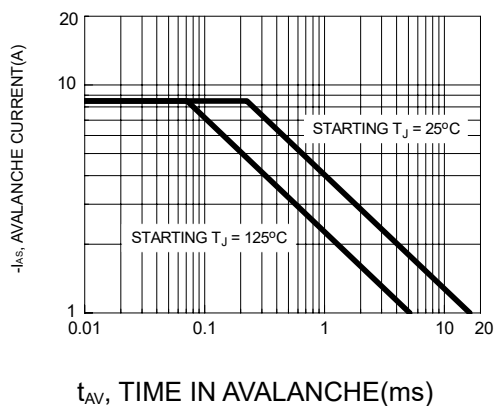


Figure 9: Unclamped Inductive Switching Capability.

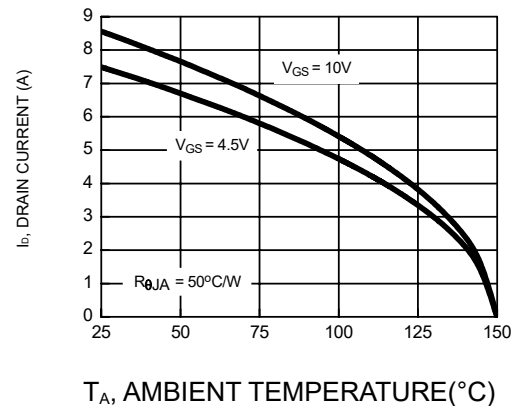


Figure 10: Maximum Continuous Drain Current vs Ambient Temperature.

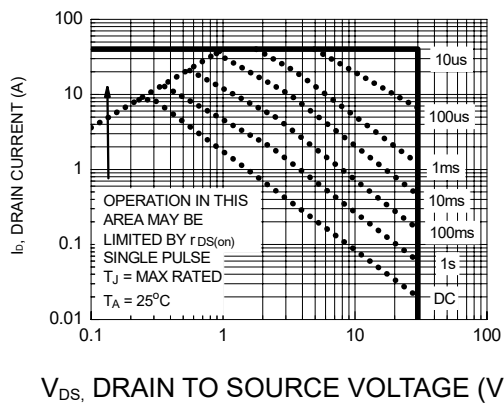


Figure 11: Forward Bias Safe Operating Area.

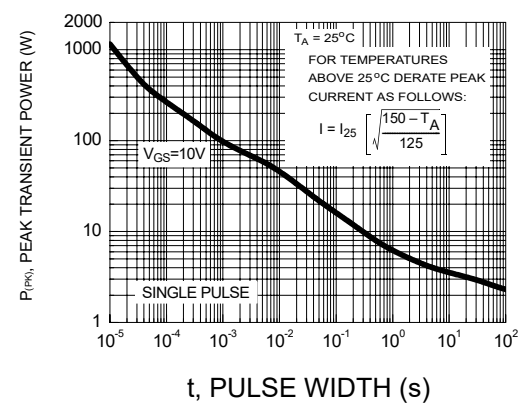
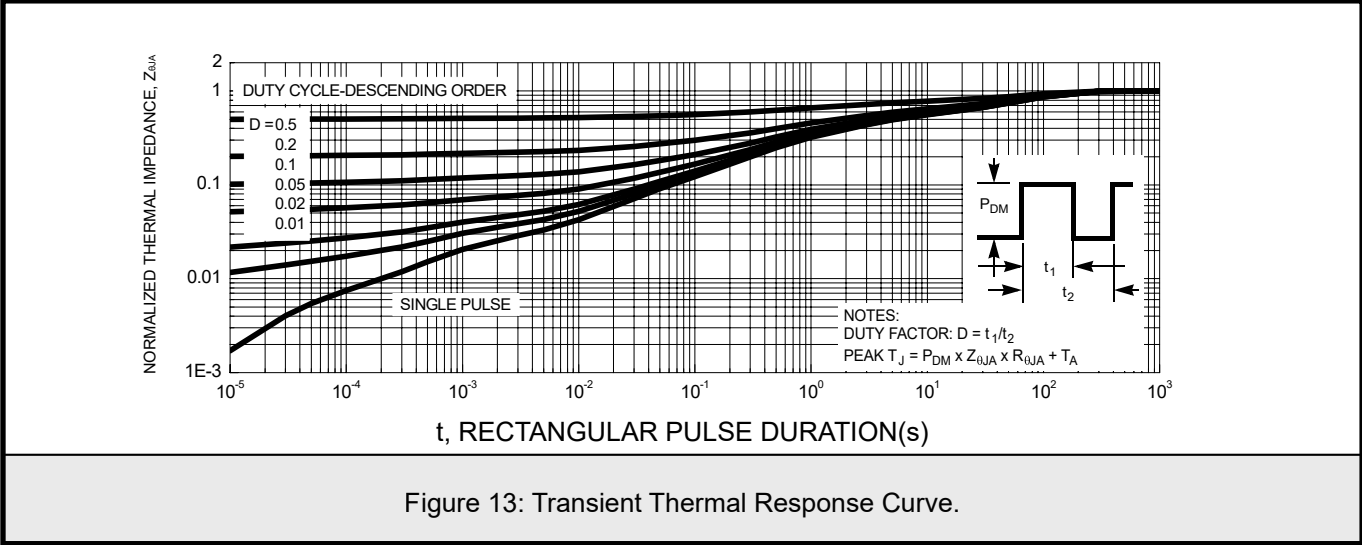


Figure 12: Single Pulse Maximum Power Dissipation.

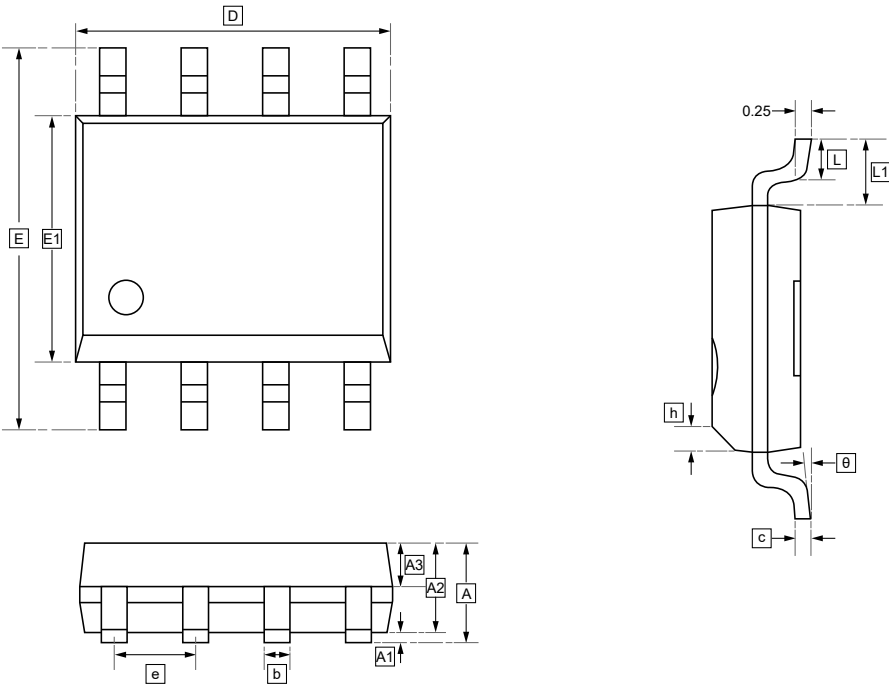


6.3Typical Characterisitics





7.SOP-8 Package Outline Dimensions



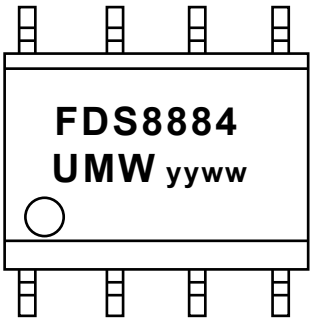
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°



8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDS8884	SOP-8	3000	Tape and reel



9.Disclaimer

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