



PBL6003D

60 V, 1 A PNP loadswitch double transistor

12 August 2026

Product data sheet

1. General description

PNP low V_{CEsat} transistor and NPN Resistor-Equipped Transistor (RET) in a SOT457 (SC-74) small Surface Mounted Device (SMD) plastic package.

2. Features and benefits

- Low V_{CEsat} transistor and resistor-equipped transistor in one package
- Low threshold voltage (< 1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

3. Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

4. Quick reference data

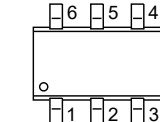
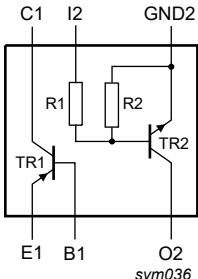
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	-60	V
I_C	collector current		[1]	-	-	-1	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -1$ A; $I_B = -100$ mA; $T_{amb} = 25$ °C; pulsed; $t_p \leq 300$ μ s; $\delta_{factor} \leq 0.02$		-	255	340	m Ω
TR2; NPN resistor-equipped transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	50	V
I_O	output current			-	-	100	mA
R1	bias resistor 1 (input)			7	10	13	k Ω
R2/R1	bias resistor ratio			0.8	1	1.2	

[1] Device mounted on a ceramic Printed-Circuit Board (PCB), Al_2O_3 , standard footprint.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 TSOP6 (SOT457)	 sym036
2	B1	base TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	C1	collector TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBLS6003D	TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PBLS6003D	F3

8. Limiting values

Table 5. Limiting values

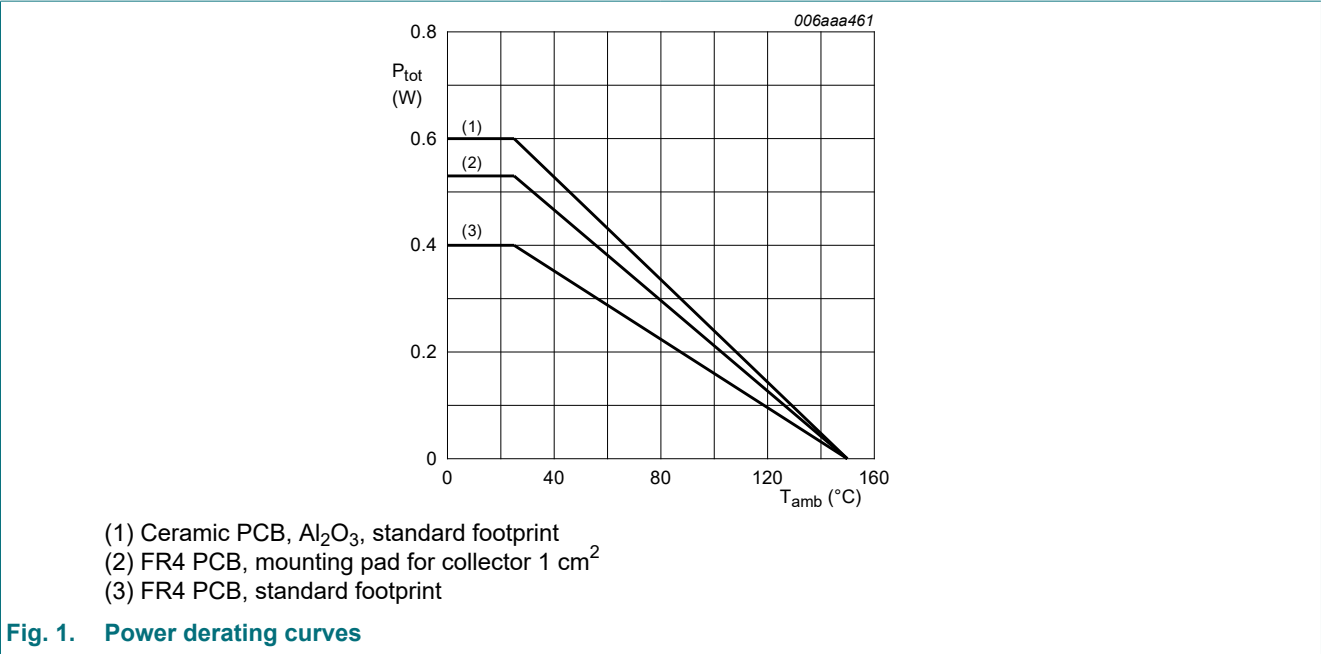
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR1; PNP low V _{CEsat} transistor						
V _{CBO}	collector-base voltage	open emitter		-	-80	V
V _{CEO}	collector-emitter voltage	open base		-	-60	V
V _{EBO}	emitter-base voltage	open collector		-	-5	V
I _C	collector current		[1]	-	-700	mA
			[2]	-	-850	mA
			[3]	-	-1	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms		-	-2	A
I _B	base current			-	-300	mA
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms		-	-1	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	250	mW
			[2]	-	350	mW
			[3]	-	400	mW
TR2; NPN resistor-equipped transistor						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
V _I	input voltage			-10	40	V
I _O	output current			-	100	mA
I _{CM}	peak collector current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
			[2]	-	200	mW
			[3]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	400	mW
			[2]	-	530	mW
			[3]	-	600	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

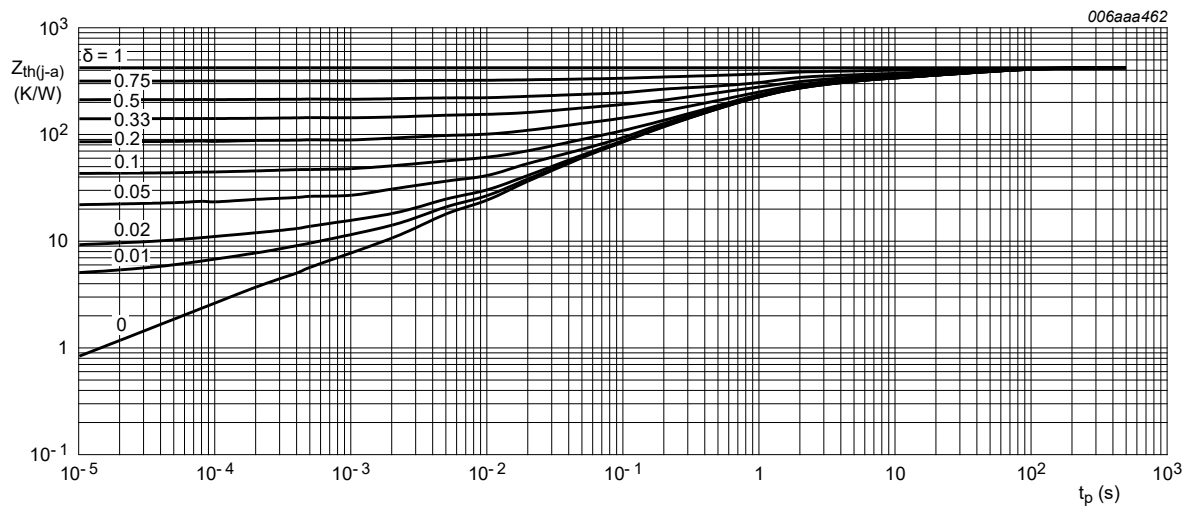


9. Thermal characteristics

Table 6. Thermal characteristics

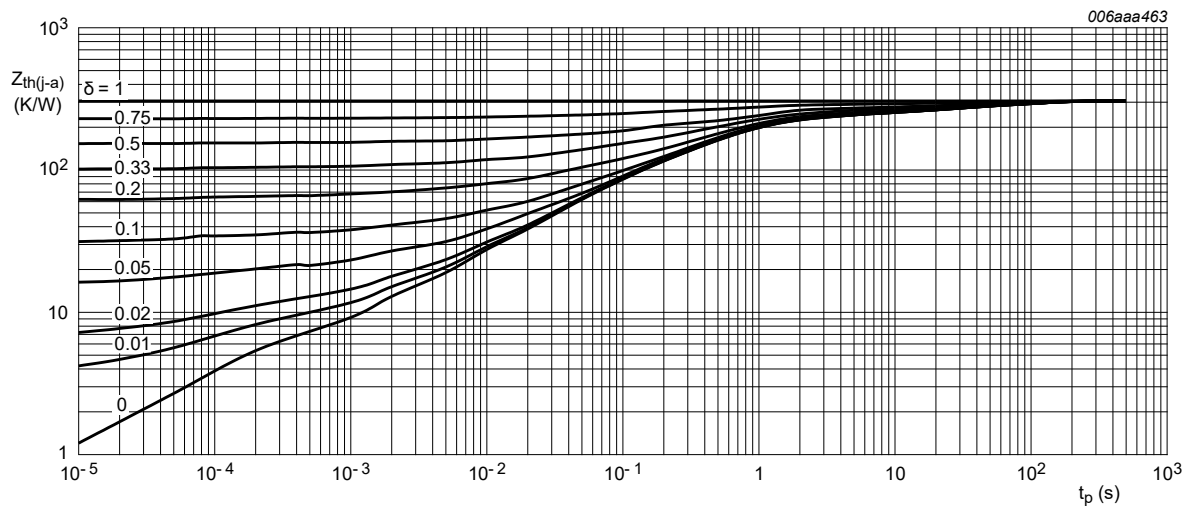
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	312	K/W
			[2]	-	-	236	K/W
			[3]	-	-	208	K/W
TR1; PNP low V _{CEsat} transistor							
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	105	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



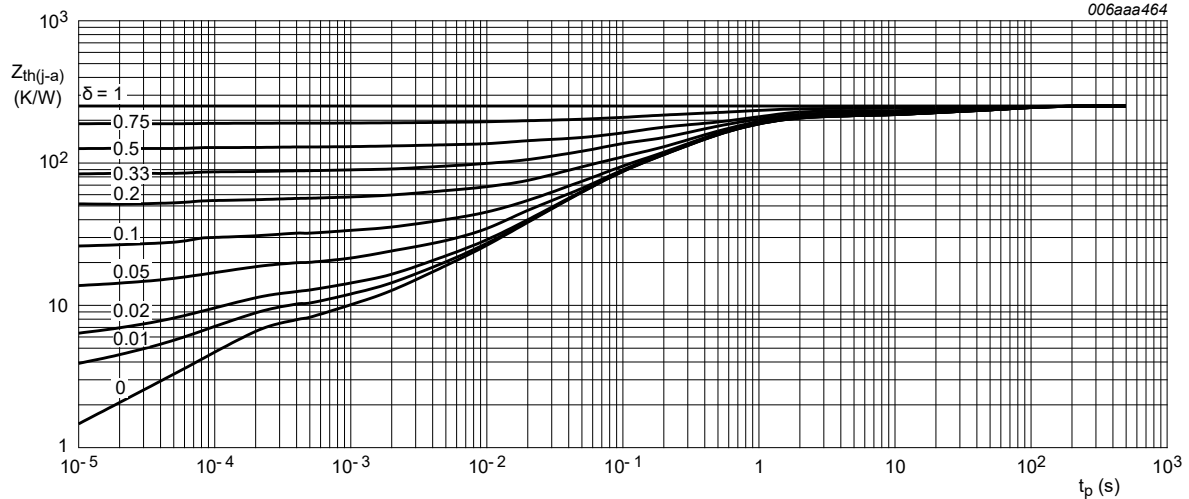
FR4 PCB, standard footprint

Fig. 2. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm²

Fig. 3. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al₂O₃, standard footprint

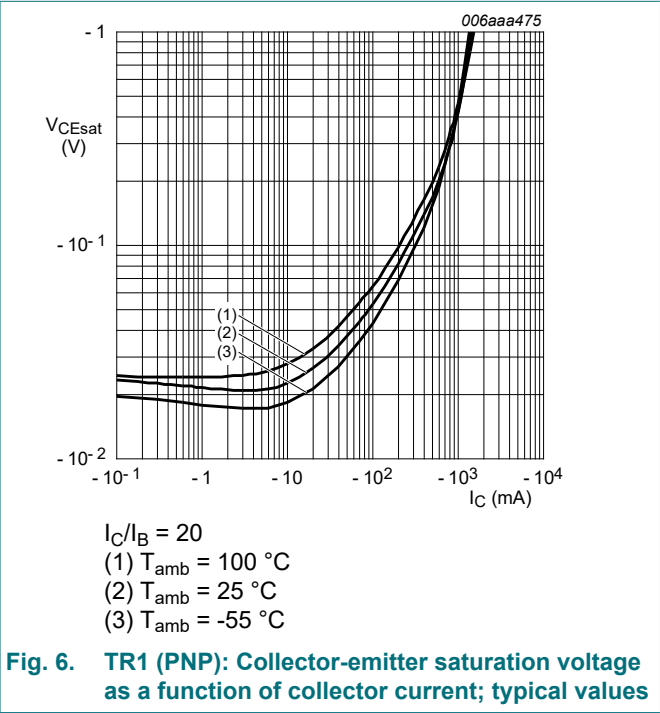
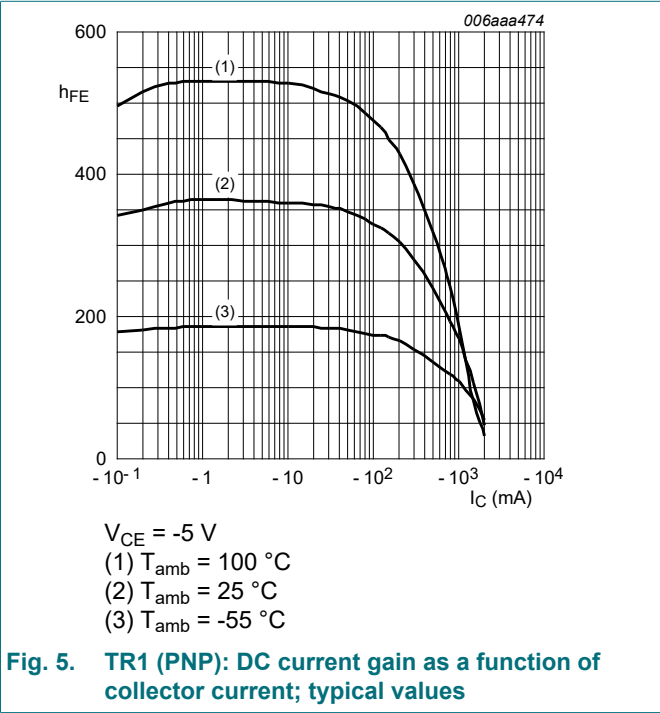
Fig. 4. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = -60\text{ V}$; $I_E = 0\text{ A}$; $T_{amb} = 25\text{ °C}$	-	-	-100	nA
		$V_{CB} = -60\text{ V}$; $I_E = 0\text{ A}$; $T_j = 150\text{ °C}$	-	-	-50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = -60\text{ V}$; $V_{BE} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$	-	-	-100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}$; $I_C = 0\text{ A}$; $T_{amb} = 25\text{ °C}$	-	-	-100	nA
h_{FE}	DC current gain	$V_{CE} = -5\text{ V}$; $I_C = -1\text{ mA}$; $T_{amb} = 25\text{ °C}$	200	350	-	
		$V_{CE} = -5\text{ V}$; $I_C = -500\text{ mA}$; pulsed; $t_p \leq 300\text{ μs}$; $\delta \leq 0.02$; $T_{amb} = 25\text{ °C}$	150	230	-	
		$V_{CE} = -5\text{ V}$; $I_C = -1\text{ A}$; pulsed; $t_p \leq 300\text{ μs}$; $\delta \leq 0.02$; TR1; PNP low V_{CEsat} transistor; $T_{amb} = 25\text{ °C}$	100	160	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -100\text{ mA}$; $I_B = -1\text{ mA}$; $T_{amb} = 25\text{ °C}$	-	-110	-175	mV
		$I_C = -500\text{ mA}$; $I_B = -50\text{ mA}$; pulsed; $t_p \leq 300\text{ μs}$; $\delta \leq 0.02$; $T_{amb} = 25\text{ °C}$	-	-135	-180	mV
		$I_C = -1\text{ A}$; $I_B = -100\text{ mA}$; pulsed; $t_p \leq 300\text{ μs}$; $\delta \leq 0.02$; $T_{amb} = 25\text{ °C}$	-	-255	-340	mV
R_{CEsat}	collector-emitter saturation resistance	$I_C = -1\text{ A}$; $I_B = -100\text{ mA}$; $T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 300\text{ μs}$; $\delta_{factor} \leq 0.02$	-	255	340	mΩ
V_{BEsat}	base-emitter saturation voltage	$I_C = -1\text{ A}$; $I_B = -50\text{ mA}$; $T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 300\text{ μs}$; $\delta_{factor} \leq 0.02$	-	-0.95	-1.1	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -5\text{ V}$; $I_C = -1\text{ A}$; $T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 300\text{ μs}$; $\delta_{factor} \leq 0.02$	-	-0.82	-0.9	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_d	delay time	$I_C = -0.5\text{ A}$; $I_{B\text{on}} = -25\text{ mA}$; $I_{B\text{off}} = 25\text{ mA}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	-	11	-	ns
t_r	rise time		-	30	-	ns
t_{on}	turn-on time		-	41	-	ns
t_s	storage time		-	205	-	ns
t_f	fall time		-	55	-	ns
t_{off}	turn-off time		-	260	-	ns
C_c	collector capacitance	$V_{CB} = -10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	-	9	15	pF
f_T	transition frequency	$V_{CE} = -10\text{ V}$; $I_C = -50\text{ mA}$; $f = 100\text{ MHz}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	150	185	-	MHz
TR2; NPN resistor-equipped transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}$; $I_E = 0\text{ A}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	-	-	1	μA
		$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}$; $I_C = 0\text{ A}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	-	-	400	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}$; $I_C = 5\text{ mA}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	30	-	-	
$V_{CE\text{sat}}$	collector-emitter saturation voltage	$I_C = 10\text{ mA}$; $I_B = 0.5\text{ mA}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	-	-	150	mV
$V_{I(\text{off})}$	off-state input voltage	$V_{CE} = 5\text{ V}$; $I_C = 100\text{ }\mu\text{A}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	-	1.1	0.8	V
$V_{I(\text{on})}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$; $I_C = 10\text{ mA}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	2.5	1.8	-	V
R1	bias resistor 1 (input)		7	10	13	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	-	-	2.5	pF



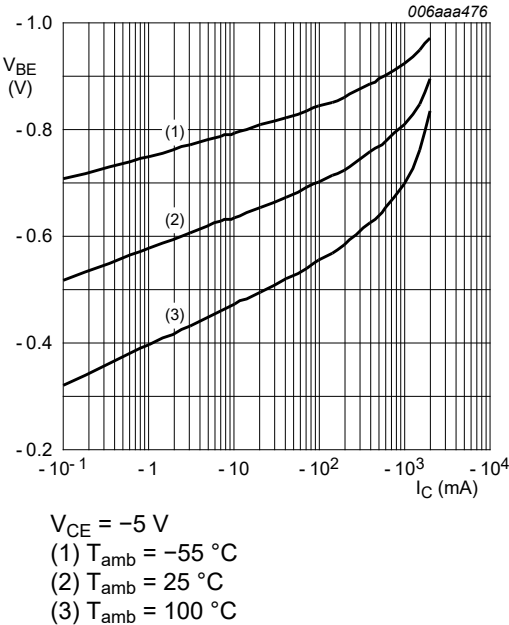


Fig. 7. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values

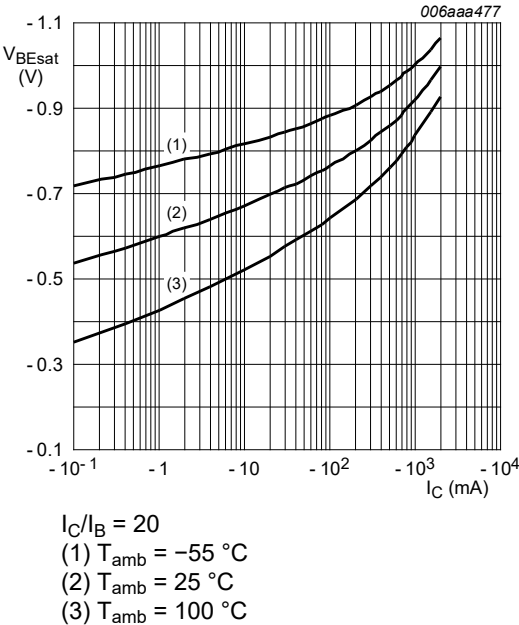


Fig. 8. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values

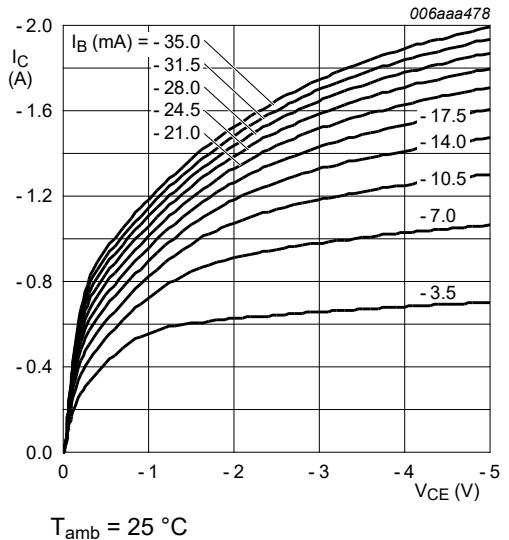


Fig. 9. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values

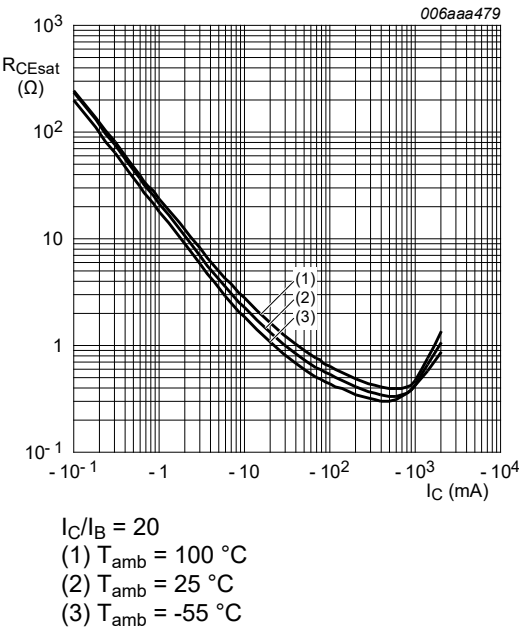


Fig. 10. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

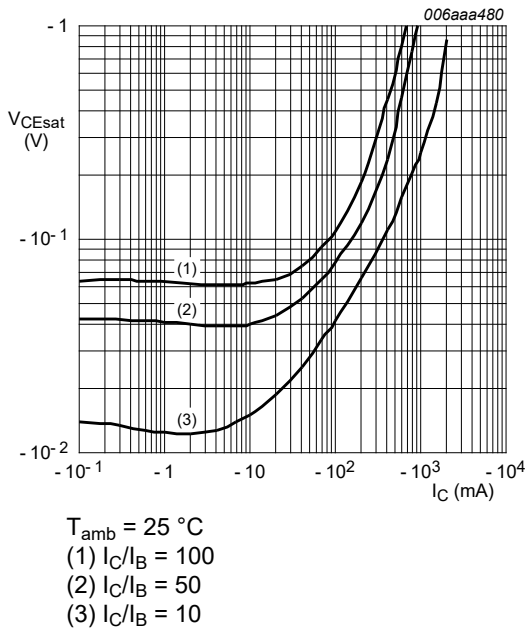


Fig. 11. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

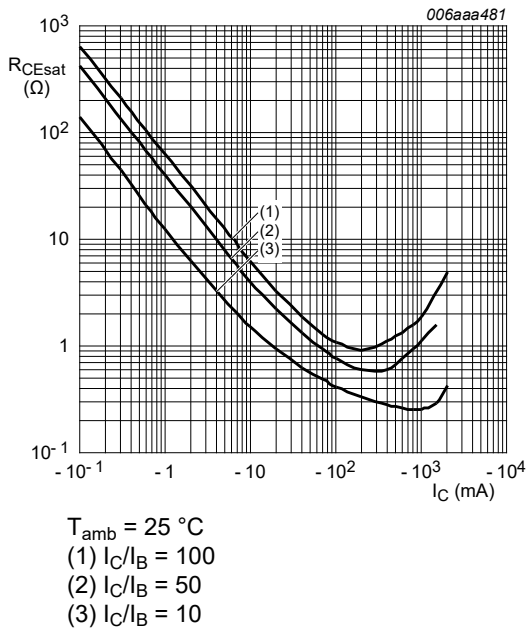


Fig. 12. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

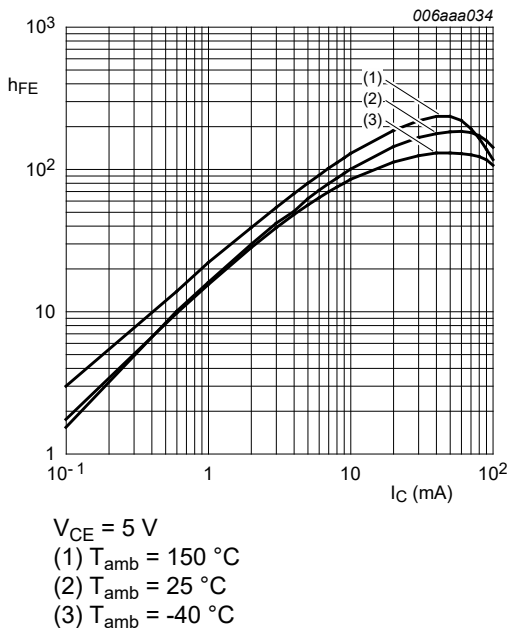


Fig. 13. TR2 (NPN): DC current gain as a function of collector current; typical values

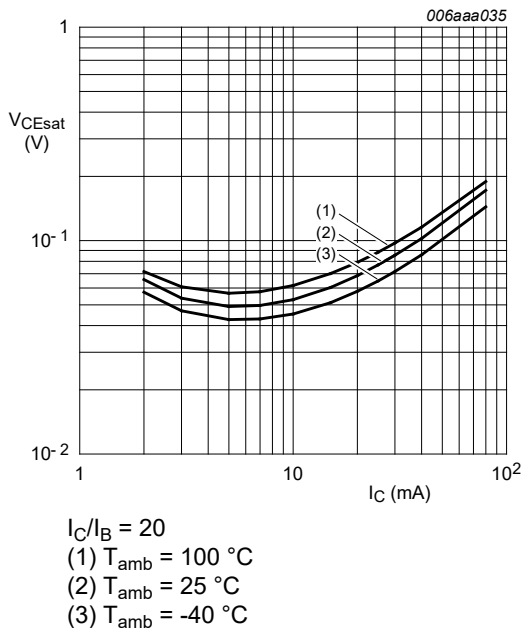


Fig. 14. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

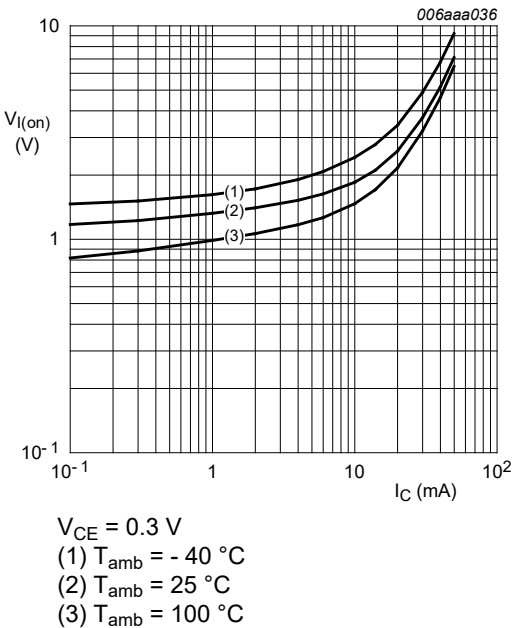


Fig. 15. TR2 (NPN): On-state input voltage as a function of collector current; typical values

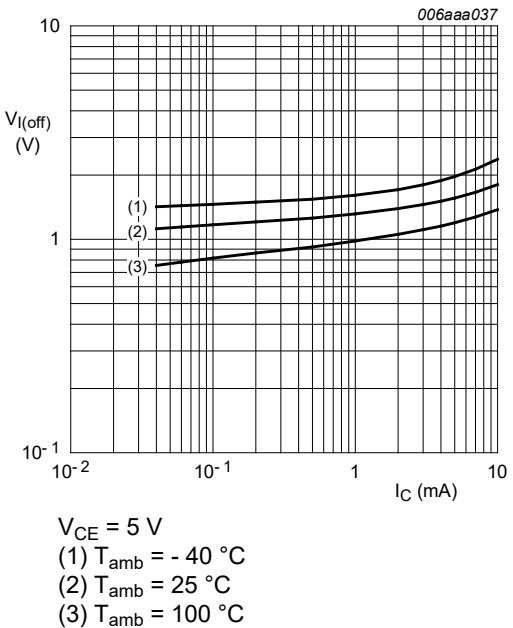


Fig. 16. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

11. Test information

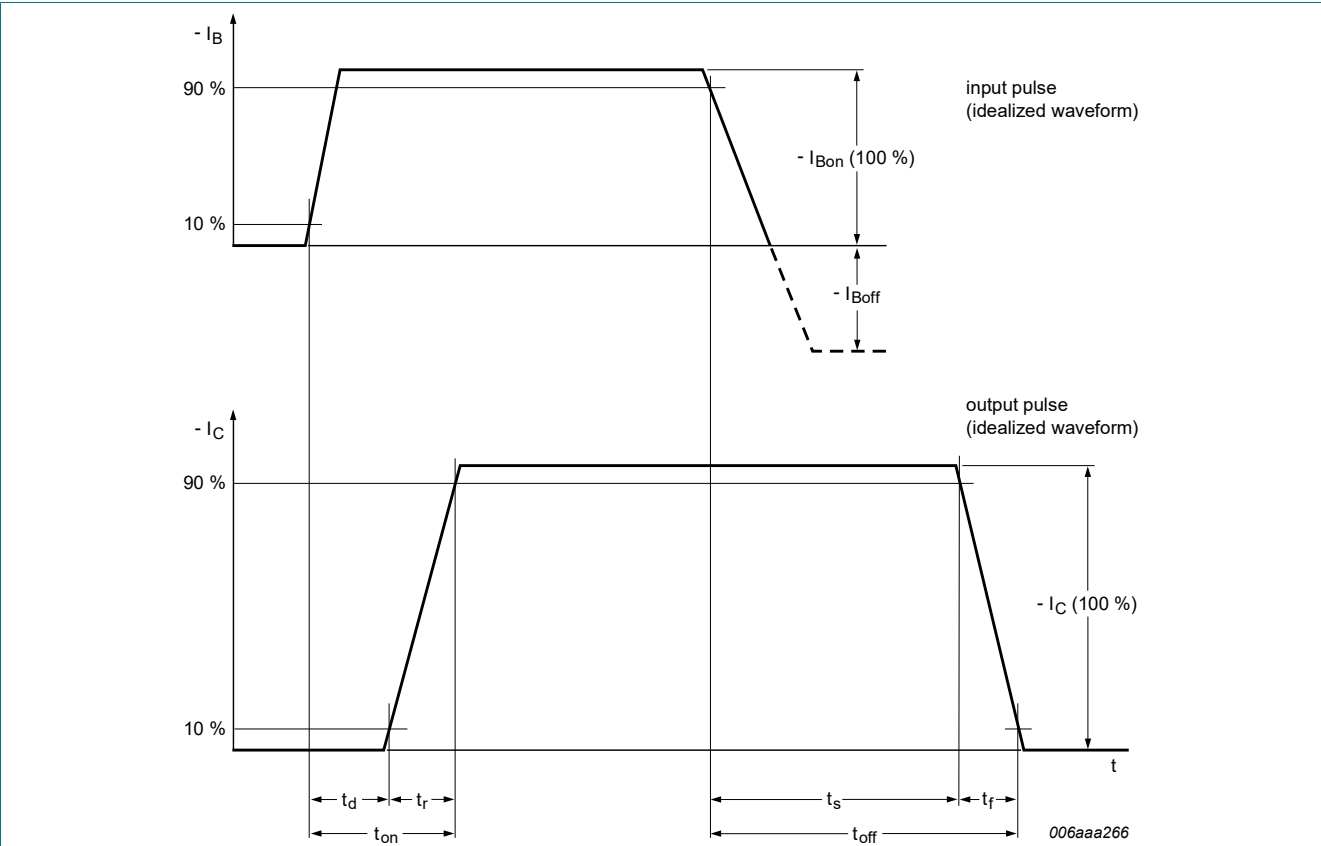
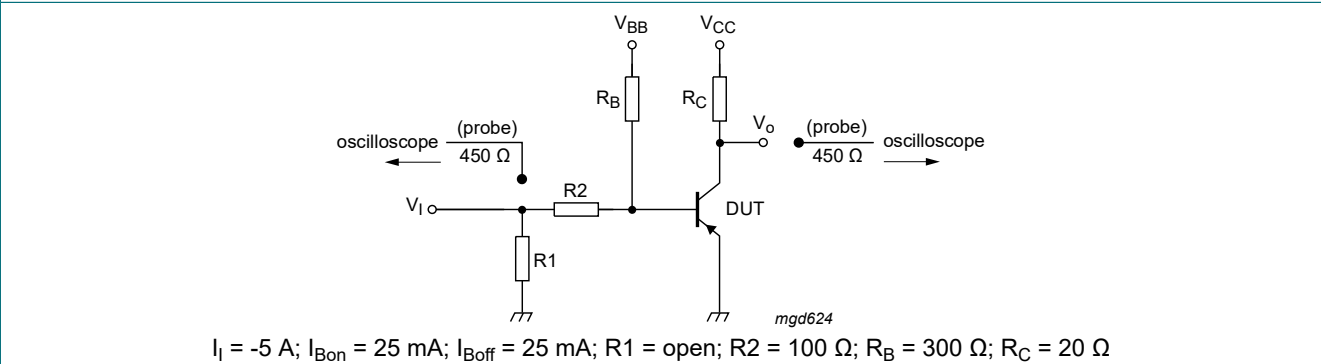


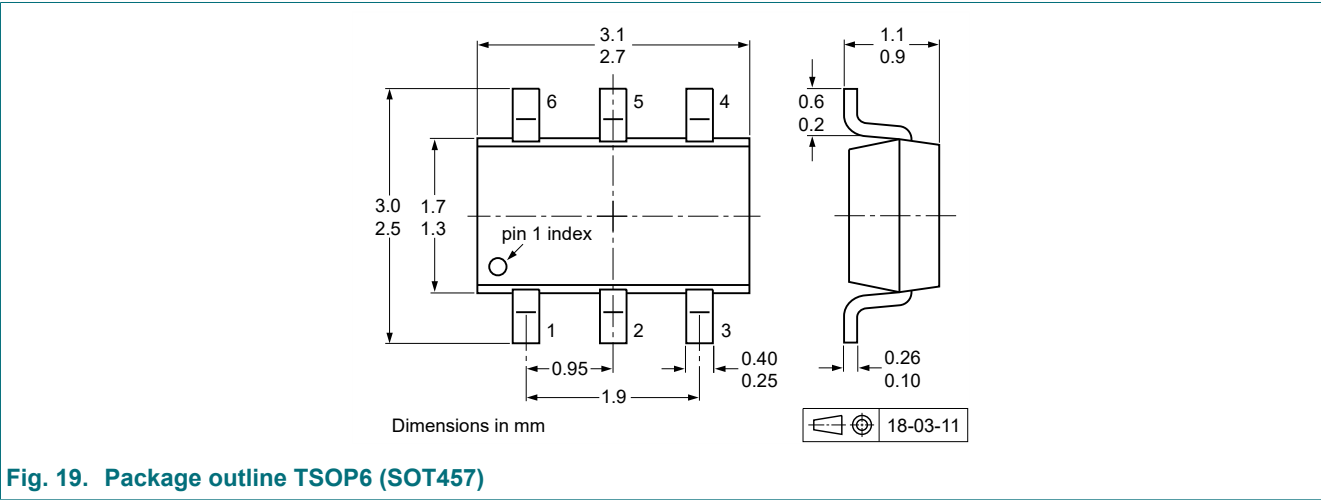
Fig. 17. Transistor switching time definition



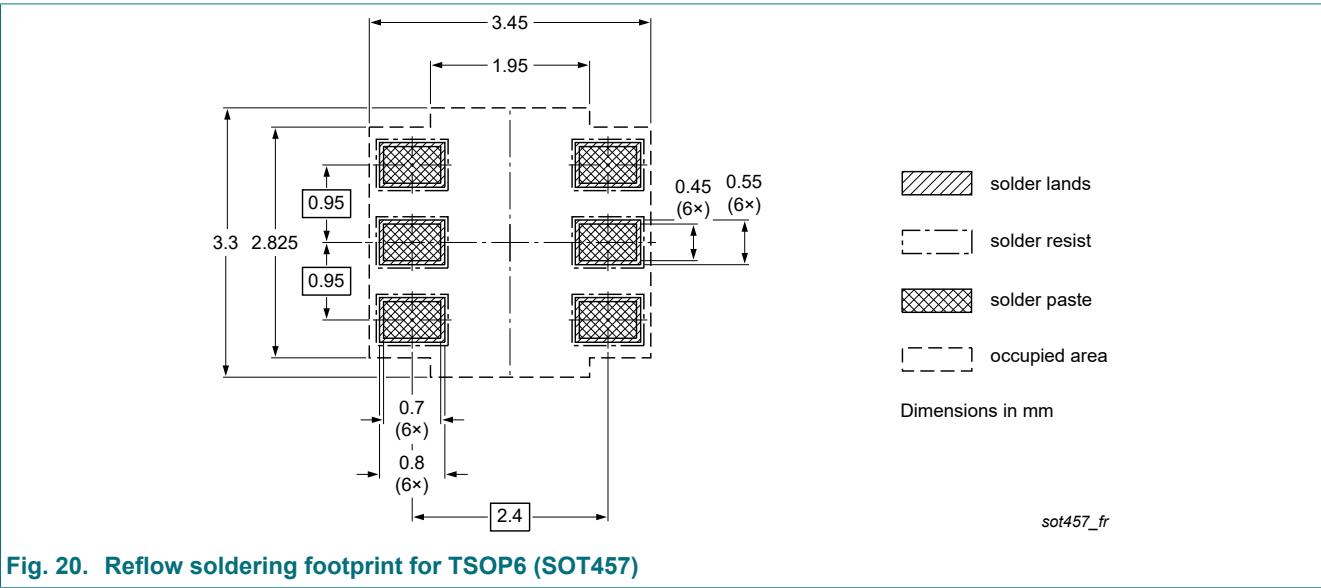
$I_I = -5\text{ A}$; $I_{B\text{on}} = 25\text{ mA}$; $I_{B\text{off}} = 25\text{ mA}$; $R_1 = \text{open}$; $R_2 = 100\text{ }\Omega$; $R_B = 300\text{ }\Omega$; $R_C = 20\text{ }\Omega$

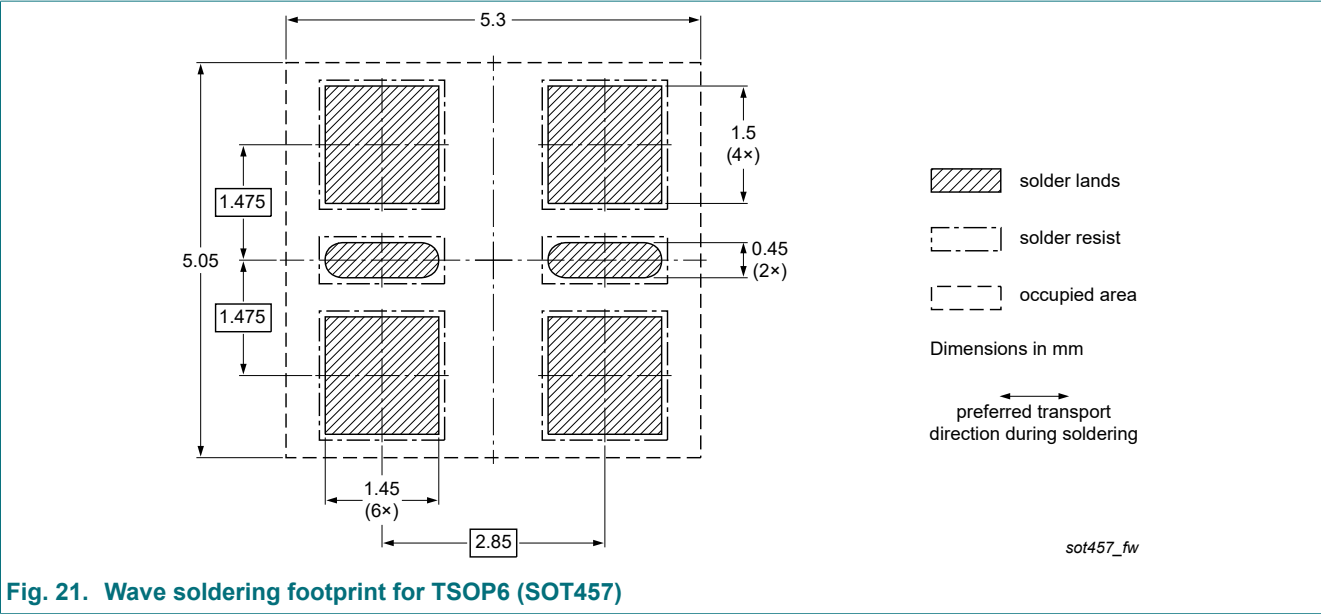
Fig. 18. Test circuit for switching times

12. Package outline



13. Soldering





14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBLS6003D v.4	20260812	Product data sheet	-	PBLS6003D v.3
Modifications:	Product(s) changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s).			
PBLS6003D v.3	20230830	Product data sheet	-	PBLS6003D_2
PBLS6003D_2	20090907	Product data sheet	-	PBLS6003D_1
PBLS6003D_1	20050628	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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