

Document Title**256Kx16 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	June 28, 1996	Advance
0.1	Revise - Die name change ; A to B	September 19, 1996	Preliminary
1.0	Finalize	December 17, 1996	Final
2.0	Revise - Operating current update and release. Icc(Read/Write) = 20/40 → 10/45mA Icc1(Read/Write) = 20/40 → 10/45mA Icc2 = 90 → 70mA	February 17, 1997	Final
3.0	Revise - Change datasheet format - Erase 70ns part from KM616V4000BI, KM616U4000B and KM616U4000BI Family - Power dissipation improved 0.7 to 1.0W - V _{IL} (MAX) improved 0.4 to 0.6V. - Icc2 decreased 70 to 60mA. - Erase 100ns from KM616V4000B commercial product	January 14, 1998	Final
3.01	Error correction	August 7, 1998	

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256Kx16 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 256K x16
- Power Supply Voltage
KM68V4000B Family: 3.0~3.6V
KM68U4000B Family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2-400F/R

GENERAL DESCRIPTION

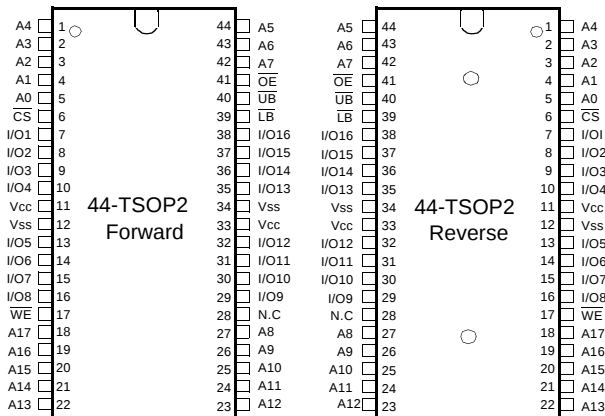
The K6T4016V3B and K6T4016U3B families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature range and have small package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
K6T4016V3B-B	Commercial(0~70°C)	3.0~3.6V	70 ¹ /85 ¹ ns	15μA	60mA	44-TSOP2-F/R
K6T4016U3B-B		2.7~3.3V	85 ¹ /100ns			
K6T4016V3B-F	Industrial(-40~85°C)	3.0~3.6V	85 ¹ /100ns	20μA		
K6T4016U3B-F		2.7~3.3V				

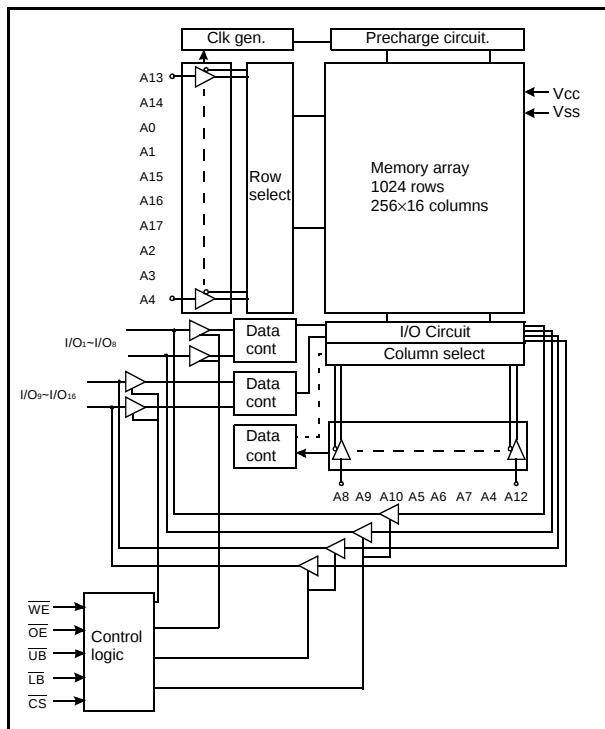
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	$\overline{LB}$	Lower Byte (I/O1~8)
$\overline{OE}$	Output Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
$\overline{WE}$	Write Enable Input	Vcc	Power
A0~A17	Address Inputs	Vss	Ground
I/O1~I/O16	Data Inputs/Outputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

PRODUCT LIST

Commercial Temperature Product(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6T4016V3B-TB70	44-TSOP2-F, 70ns, 3.3V,LL	K6T4016V3B-TF85	44-TSOP2-F, 85ns, 3.3V,LL
K6T4016V3B-TB85	44-TSOP2-F, 85ns, 3.3V,LL	K6T4016V3B-TF10	44-TSOP2-F, 100ns, 3.3V,LL
K6T4016V3B-RB70	44-TSOP2-R, 70ns, 3.3V,LL	K6T4016V3B-RF85	44-TSOP2-R, 85ns, 3.3V,LL
K6T4016V3B-RB85	44-TSOP2-R, 85ns, 3.3V,LL	K6T4016V3B-RF10	44-TSOP2-R, 100ns, 3.3V,LL
K6T4016U3B-TB85	44-TSOP2-F, 85ns, 3.0V,LL	K6T4016U3B-TF85	44-TSOP2-F, 85ns, 3.0V,LL
K6T4016U3B-TB10	44-TSOP2-F, 100ns, 3.0V,LL	K6T4016U3B-TF10	44-TSOP2-F, 100ns, 3.0V,LL
K6T4016U3B-RB85	44-TSOP2-R, 85ns, 3.0V,LL	K6T4016U3B-RF85	44-TSOP2-R, 85ns, 3.0V,LL
K6T4016U3B-RB10	44-TSOP2-R, 100ns, 3.0V,LL	K6T4016U3B-RF10	44-TSOP2-R, 100ns, 3.0V,LL

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
L	H	H	X ¹⁾	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	Commercial
		-40 to 85	°C	Industrial
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	K6T4016V3B Family K6T4016U3B Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	K6T4016V3B, K6T4016U3B Family	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	K6T4016V3B, K6T4016U3B Family	-0.3 ³⁾	-	0.6	V

Note:

1. Commercial Product : T_A=0 to 70°C, otherwise specified
Industrial Product : T_A=-40 to 85°C, otherwise specified
2. Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns
3. Undershoot : -3.0V in case of pulse width ≤ 30ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IL} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IL} or V _{IH} , Read	-	-	10	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA $\overline{CS} \leq 0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	Read	-	-	10
			Write	-	-	45
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL}	-	-	60	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.2	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}=V_{IH}$, Other inputs=V _{IL} or V _{IH}	-	-	0.5	mA
Standby Current(CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Others inputs = 0~V _{CC}	-	-	15 ¹⁾	μA

1. Industrial product = 20μA

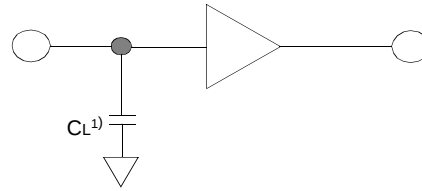
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V

Input rising and falling time : 5ns

Input and output reference voltage :1.5V

Output load(see right) : $C_L=100\text{pF}+1\text{TTL}$ $C_L=30\text{pF}+1\text{TTL}$ 

1.Including scope and jig capacitance

AC CHARACTERISTICS (K6T4016V3B Family: $V_{CC}=3.0\sim 3.6\text{V}$, K6T4016U3B Family: $V_{CC}=2.7\sim 3.3\text{V}$,
Commercial product : $T_A=0$ to 70°C , Industrial product : $T_A=-40$ to 85°C)

Parameter List		Symbol	Speed Bins						Units
			70ns ¹⁾		85ns ¹⁾		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	70	-	85	-	100	-	ns
	Address access time	t _{AA}	-	70	-	85	-	100	ns
	Chip select to output	t _{CO}	-	70	-	85	-	100	ns
	Output enable to valid output	t _{OE}	-	35	-	40	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	5	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ enable to low-Z output	t _{BLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	25	0	30	ns
	$\overline{\text{OE}}$ disable to high-Z output	t _{OHZ}	0	25	0	25	0	30	ns
	Output hold from address change	t _{OH}	10	-	10	-	15	-	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ valid to data output	t _{BA}	-	35	-	40	-	50	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ disable to high-Z output	t _{BHZ}	0	25	0	25	0	30	ns
Write	Write cycle time	t _{WC}	70	-	85	-	100	-	ns
	Chip select to end of write	t _{CW}	60	-	70	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t _{AW}	60	-	70	-	80	-	ns
	Write pulse width	t _{WP}	55	-	55	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	25	0	30	ns
	Data to write time overlap	t _{DW}	30	-	35	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	5	-	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ valid to end of write	t _{BW}	60	-	70	-	80	-	ns

1. The parameter is measured with 30pF test load.

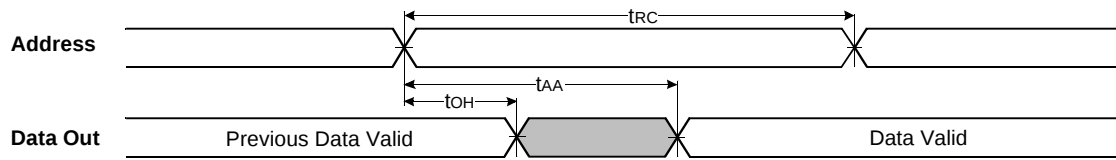
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$	2.0	-	3.6	V
Data retention current	I _{DR}	$V_{CC}=3.0\text{V}$, $\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$	-	0.5	15 ¹⁾	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

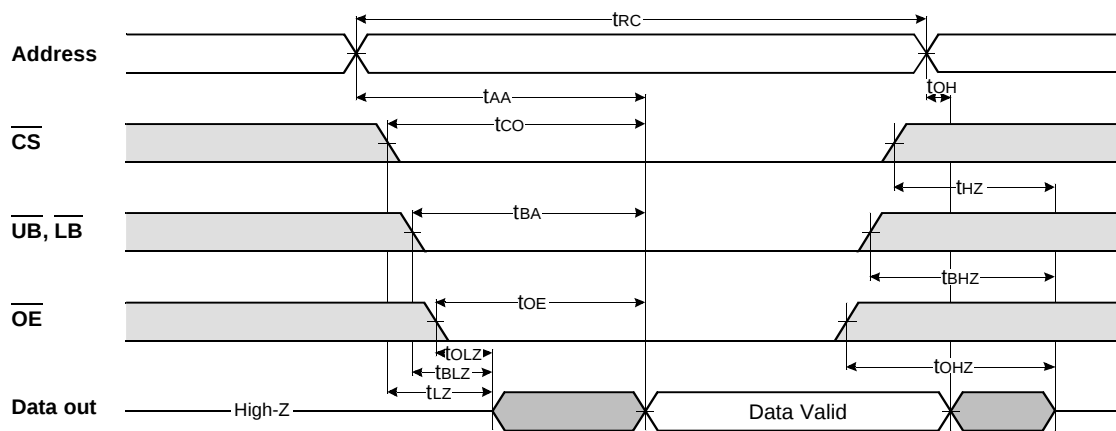
1. Industrial product = 20 μA

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, $\overline{UB}$ or/and $\overline{LB}=V_{IL}$)

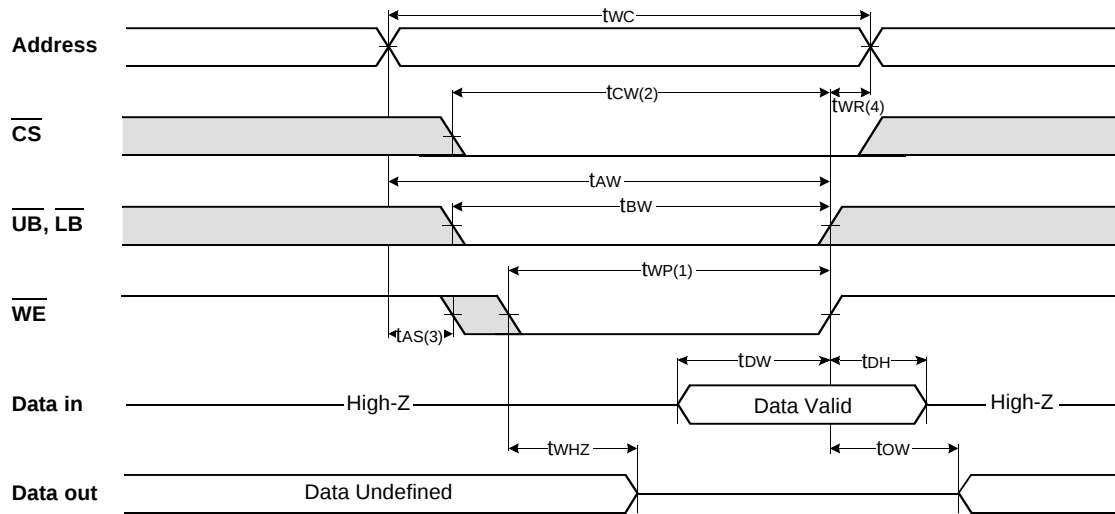
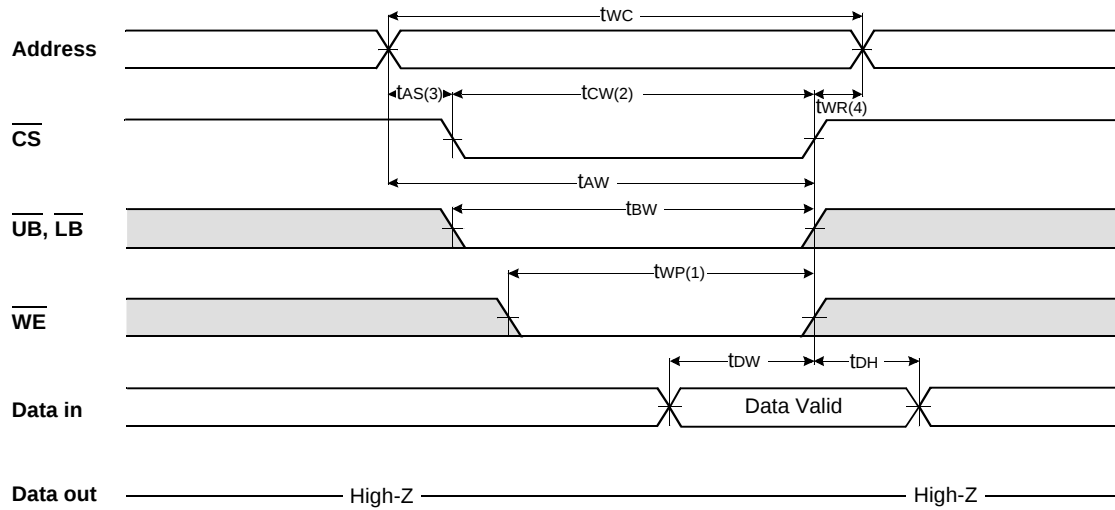


TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

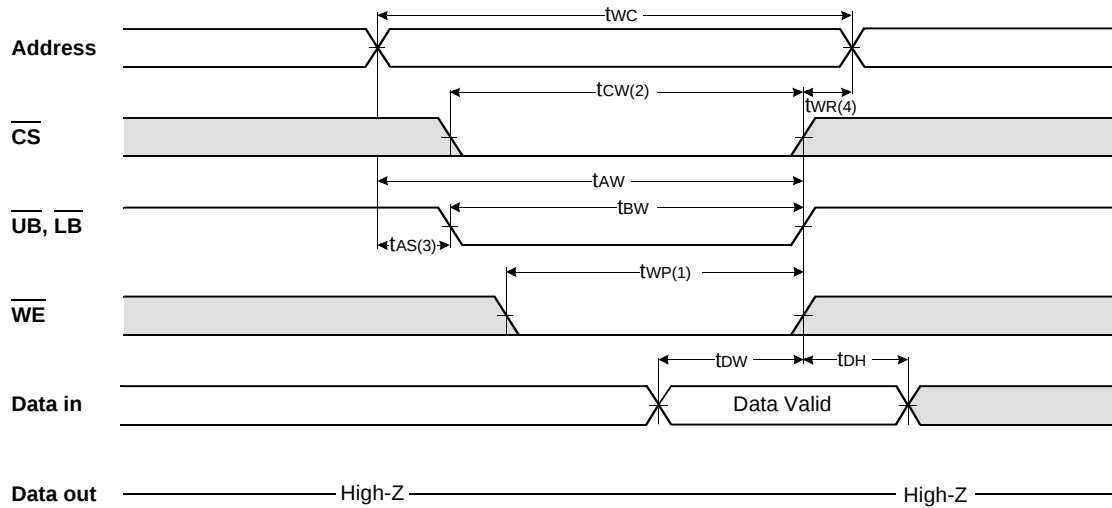


NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

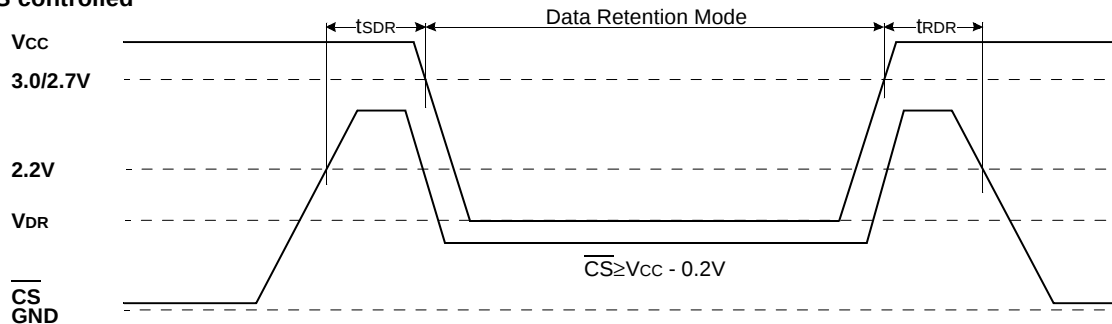


NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

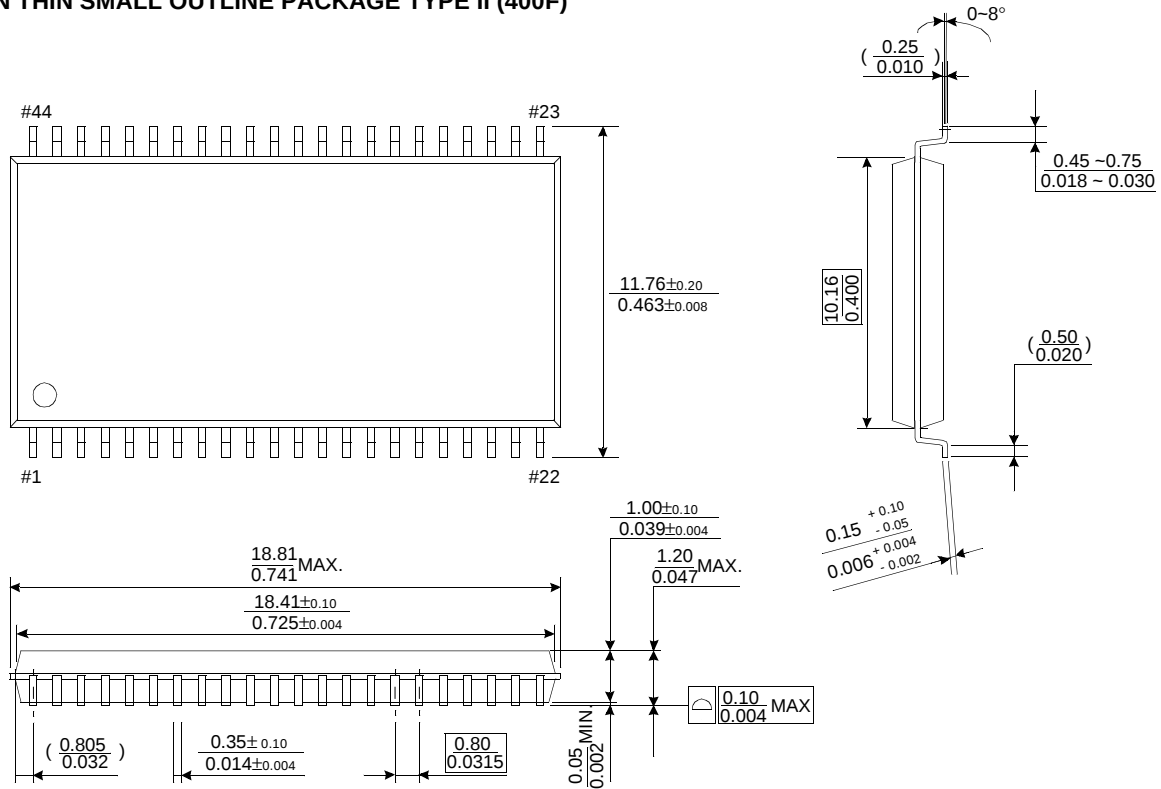
$\overline{CS}$ controlled



PACKAGE DIMENSIONS

Unit: millimeters(inches)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

