TEXAS INSTRUMENTS

SN65EPT21D Differential PECL or LVDS to TTL Translator

General Description:

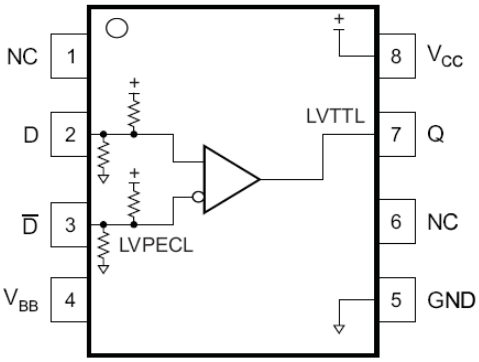
The SN65EPT21 is a differential PECL-to-TTL translator. It operates on +3.3 V supply and ground only. The device includes circuitry to maintain inputs at Vcc/2 when left open.

The V_{BB} pin is a reference voltage output for the device. When the device is used in single-ended mode, the unused input should be tied to VBB. This reference voltage can also be used to bias the input when it is ac coupled. When it is used, place a 0.01µF decoupling capacitor between VCC and VBB. Also limit the sink/source current to < 0.5 mA to VBB. Leave VBB open when it is not used.

The SN65EPT21 is housed in an industry standard SOIC-8 package and is also available in an optional TSSOP-8 package.

Key Features:

- 1 ns Propagation Delay
- Fmax > 300MHz
- Operating Range: VCC = 3.0 V to 3.6 V with GND = 0 V
- 24-mA TTL Output
- Built-In Temperature Compensation
- Drop-In Compatible to the MC10EPT21, MC100EPT21



Applications:

- Data and Clock Transmission Over Backplane
- Signalling Level Conversion for Clock or Data

Related Products Information:

Mfr Part #	Farnell #	Newark #	Description
SN65EPT21D	1783858	55R1352	Differential PECL/LVDS to TTL Translator

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