

# RAD-TOLERANT CLASS V, HIGH-SPEED PWM CONTROLLER

Check for Samples: [UC1825-SP](#)

## FEATURES

- QML-V Qualified, SMD 5962-87681
- Rad-Tolerant: 30 kRad (Si) TID <sup>(1)</sup>
- Compatible With Voltage- or Current-Mode Topologies
- Practical Operation Switching Frequencies to 1 MHz
- 50-ns Propagation Delay-to-Output
- High-Current Dual Totem Pole Outputs (1.5 A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic With Double-Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Maximum Duty-Cycle Control
- Undervoltage Lockout With Hysteresis
- Low Start-Up Current (1.1 mA)

(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/sec. Radiation Lot Acceptance Testing is available - contact factory for details.

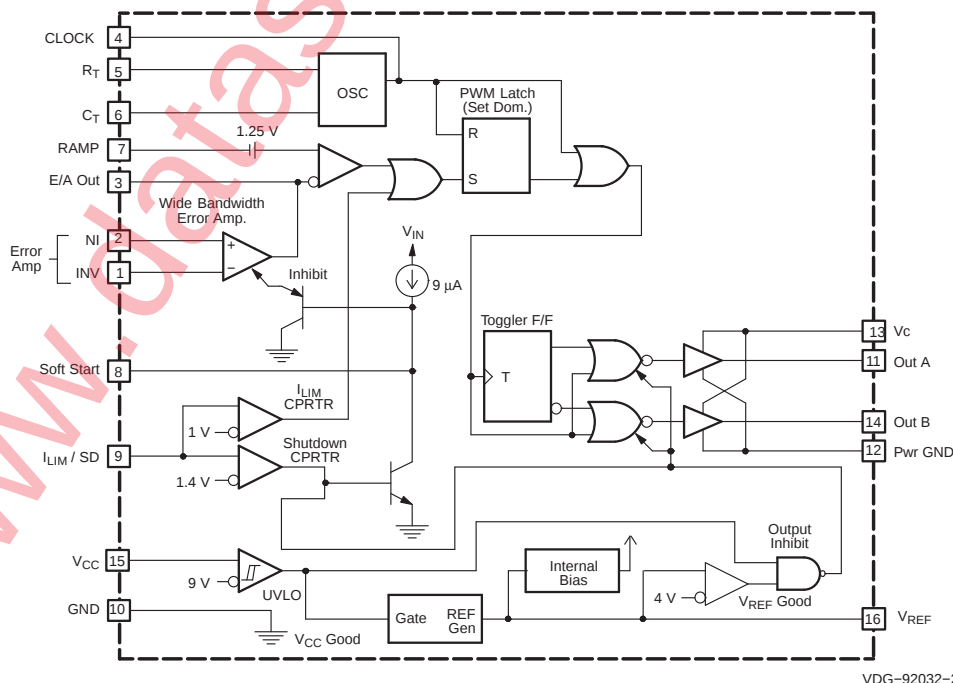
## DESCRIPTION

The UC1825 PWM control device is optimized for high-frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1-V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty-cycle clamp. The logic is fully latched to provide jitter-free operation and prohibit multiple pulses at an output. An undervoltage lockout section with 800 mV of hysteresis assures low start up current. During undervoltage lockout, the outputs are high impedance.

This device features totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

Figure 1. BLOCK DIAGRAM



VDG-92032-2



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

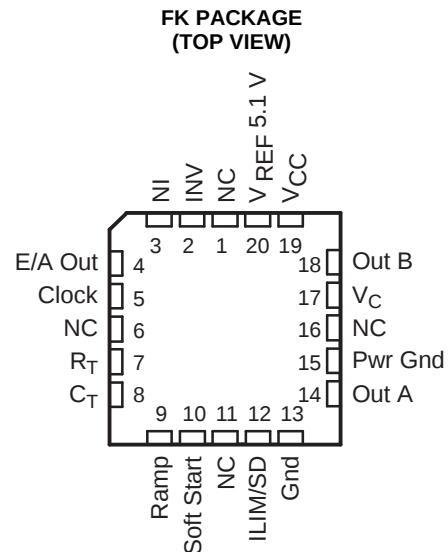
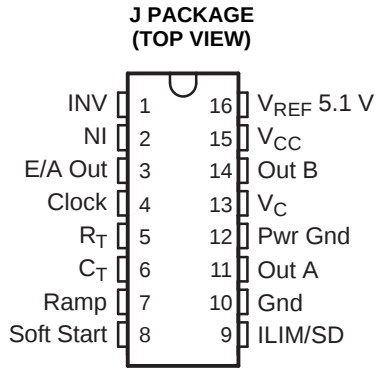
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

| <b>T<sub>A</sub></b> | <b>PACKAGE<sup>(2)</sup></b> | <b>ORDERABLE PART NUMBER</b> | <b>TOP-SIDE MARKING</b> |
|----------------------|------------------------------|------------------------------|-------------------------|
| –55°C to 125°C       | CDIP – J                     | 5962-8768104VEA              | UC1825J-SP              |
|                      | LCCC – FK                    | 5962-8768104V2A              | UC1825FK-SP             |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



### TERMINAL FUNCTIONS

| NAME                   | NO. |              | I/O | DESCRIPTION                                                                                                                                                                                                                                                      |
|------------------------|-----|--------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                        | J   | FK           |     |                                                                                                                                                                                                                                                                  |
| Clock                  | 4   | 5            | O   | Output of the internal oscillator                                                                                                                                                                                                                                |
| C <sub>T</sub>         | 6   | 8            | I   | Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.                                                                                                  |
| E/A Out                | 3   | 4            | O   | Output of the error amplifier for compensation                                                                                                                                                                                                                   |
| Gnd                    | 10  | 13           | -   | Analog ground return pin                                                                                                                                                                                                                                         |
| ILIM/SD                | 9   | 12           | I   | Input to the current limit comparator and the shutdown comparator                                                                                                                                                                                                |
| INV                    | 1   | 2            | I   | Inverting input to the error amplifier                                                                                                                                                                                                                           |
| NC                     |     | 1, 6, 11, 16 | -   | No connection                                                                                                                                                                                                                                                    |
| NI                     | 2   | 3            | I   | Non-inverting input to the error amplifier                                                                                                                                                                                                                       |
| Out A                  | 11  | 14           | O   | High-current totem pole output A of the on-chip drive stage                                                                                                                                                                                                      |
| Out B                  | 14  | 18           | O   | High-current totem pole output B of the on-chip drive stage                                                                                                                                                                                                      |
| Pwr Gnd                | 12  | 15           | -   | Ground return pin for the output driver stage                                                                                                                                                                                                                    |
| Ramp                   | 7   | 9            | I   | Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input. |
| R <sub>T</sub>         | 5   | 7            | I   | Timing resistor connection pin for oscillator frequency programming                                                                                                                                                                                              |
| Soft Start             | 8   | 10           | I   | Soft-start input pin which also doubles as the maximum duty cycle clamp                                                                                                                                                                                          |
| V <sub>C</sub>         | 13  | 17           | -   | Power supply pin for the output stage. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths.                                                                                                                |
| V <sub>CC</sub>        | 15  | 19           | -   | Power supply pin for the device. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths.                                                                                                                      |
| V <sub>REF</sub> 5.1 V | 16  | 20           | O   | 5.1-V reference. For stability, the reference should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.                                                                                                |

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

|                                              |                     |            | UNIT |
|----------------------------------------------|---------------------|------------|------|
| Supply voltage                               | $V_C, V_{CC}$       | 30         | V    |
| Output current, source or sink, Out A, Out B | DC                  | 0.5        | A    |
|                                              | Pulse (0.5 $\mu$ s) | 2.0        |      |
| Analog inputs                                | INV, NI, Ramp       | –0.3 to 7  | V    |
|                                              | Soft Start, ILIM/SD | –0.3 to 6  |      |
| Clock output current                         | Clock               | –5         | mA   |
| Error amplifier output current               | E/A Out             | 5          |      |
| Soft-start sink current                      | Soft Start          | 20         |      |
| Oscillator charging current                  | $R_T$               | –5         |      |
| Power dissipation                            |                     | 1          | W    |
| Storage temperature range                    |                     | –65 to 150 | °C   |
| Lead temperature (soldering, 10 seconds)     |                     | 300        |      |

(1) All voltages are with respect to GND; all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.

**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range ( $T_A = T_J = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ), unless otherwise noted.

|                                                         | MIN | MAX | UNIT |
|---------------------------------------------------------|-----|-----|------|
| $V_{CC}$ Supply voltage                                 | 10  | 30  | V    |
| Sink/source output current (continuous or time average) | 0   | 100 | mA   |
| Reference load current                                  | 0   | 10  | mA   |

**THERMAL RATINGS TABLE**

| PACKAGE     | $\theta_{JA}$<br>(°C/W) | $\theta_{JC}$<br>(°C/W) |
|-------------|-------------------------|-------------------------|
| DIL-16 (J)  | 80–120                  | 28 <sup>(1)</sup>       |
| LCC-20 (FK) | 70–80                   | 20 <sup>(1)</sup>       |

(1)  $\theta_{JC}$  data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that the baseline values shown are worst case (mean + 2s) for a 60 × 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack 10°C/W; pin grid array, 10°C/W.

## ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for  $R_T = 3.65 \text{ k}\Omega$ ,  $C_T = 1 \text{ nF}$ ,  $V_{CC} = 15 \text{ V}$ ,  $-55^\circ\text{C} < T_A < 125^\circ\text{C}$ ,  $T_A = T_J$

| PARAMETERS                            | TEST CONDITIONS                                 | MIN  | TYP  | MAX  | UNIT             |
|---------------------------------------|-------------------------------------------------|------|------|------|------------------|
| <b>REFERENCE</b>                      |                                                 |      |      |      |                  |
| Output voltage                        | $T_J = 25^\circ\text{C}$ , $I_O = 1 \text{ mA}$ | 5.05 | 5.10 | 5.15 | V                |
| Line regulation                       | $10 \text{ V} < V_{CC} < 30 \text{ V}$          |      | 2    | 20   | mV               |
| Load regulation                       | $1 \text{ mA} < I_O < 10 \text{ mA}$            |      | 5    | 20   | mV               |
| Total output variation                | Line, load, temperature                         | 5.0  |      | 5.2  | V                |
| Output noise voltage                  | $10 \text{ Hz} < f < 10 \text{ kHz}$            |      | 50   |      | $\mu\text{V}$    |
| Short-circuit current                 | $V_{REF} = 0 \text{ V}$                         | -15  | -50  | -100 | mA               |
| <b>OSCILLATOR SECTION</b>             |                                                 |      |      |      |                  |
| Initial accuracy                      | $T_J = 25^\circ\text{C}$                        | 360  | 400  | 440  | kHz              |
| Voltage stability                     | $10 \text{ V} < V_{CC} < 30 \text{ V}$          |      | 0.2% | 2%   |                  |
| Temperature stability                 | $T_{MIN} < T_A < T_{MAX}$                       |      | 5%   | 16%  |                  |
| Total variation                       | Line, Temperature                               | 340  |      | 460  | kHz              |
| Clock out high                        |                                                 | 3.9  | 4.5  |      | V                |
| Clock out low                         |                                                 |      | 2.3  | 2.9  | V                |
| Ramp peak <sup>(1)</sup>              |                                                 | 2.6  | 2.8  | 3.0  | V                |
| Ramp valley <sup>(1)</sup>            |                                                 | 0.7  | 1.0  | 1.25 | V                |
| Ramp valley to peak <sup>(1)</sup>    |                                                 | 1.6  | 1.8  | 2.1  | V                |
| <b>ERROR AMPLIFIER</b>                |                                                 |      |      |      |                  |
| Input offset voltage                  |                                                 |      |      | 10   | mV               |
| Input bias current                    |                                                 |      | 0.6  | 3    | $\mu\text{A}$    |
| Input offset current                  |                                                 |      | 0.1  | 1    | $\mu\text{A}$    |
| Open-loop gain                        | $1 \text{ V} < V_O < 4 \text{ V}$               | 60   | 95   |      | dB               |
| CMRR                                  | $1.5 \text{ V} < V_{CM} < 5.5 \text{ V}$        | 75   | 95   |      | dB               |
| PSRR                                  | $10 \text{ V} < V_{CC} < 30 \text{ V}$          | 85   | 110  |      | dB               |
| Output sink current                   | $V_{E/AOut} = 1 \text{ V}$                      | 1    | 2.5  |      | mA               |
| Output source current                 | $V_{E/AOut} = 4 \text{ V}$                      | -0.5 | -1.3 |      | mA               |
| Output high voltage                   | $I_{E/AOut} = -0.5 \text{ mA}$                  | 4.0  | 4.7  | 5.0  | V                |
| Output low voltage                    | $I_{E/AOut} = 1 \text{ mA}$                     | 0    | 0.5  | 1.0  | V                |
| Gain bandwidth product <sup>(1)</sup> | $f = 200 \text{ kHz}$                           | 5    | 10.5 |      | MHz              |
| Slew rate <sup>(1)</sup>              |                                                 | 4    | 9    |      | V/ $\mu\text{s}$ |
| <b>PWM COMPARATOR</b>                 |                                                 |      |      |      |                  |
| Ramp bias current                     | $V_{Ramp} = 0 \text{ V}$                        |      | -1   | -5   | $\mu\text{A}$    |
| Duty cycle range                      |                                                 | 0%   |      | 80%  |                  |
| E/A out zero dc threshold             | $V_{Ramp} = 0 \text{ V}$                        | 1.1  | 1.25 |      | V                |
| Delay to output <sup>(1)</sup>        |                                                 |      | 50   | 80   | ns               |
| <b>SOFT-START</b>                     |                                                 |      |      |      |                  |
| Charge current                        | $V_{Soft Start} = 0.5 \text{ V}$                | 3    | 9    | 20   | $\mu\text{A}$    |
| Discharge current                     | $V_{Soft Start} = 1 \text{ V}$                  | 1    |      |      | mA               |
| <b>CURRENT LIMIT/SHUTDOWN</b>         |                                                 |      |      |      |                  |
| Current limit/shutdown bias current   | $0 < V_{ILIM/SD} < 4 \text{ V}$                 |      |      | 15   | $\mu\text{A}$    |
| Current limit threshold               |                                                 | 0.9  | 1.0  | 1.1  | V                |
| Shutdown threshold                    |                                                 | 1.25 | 1.40 | 1.55 | V                |
| Delay to output <sup>(1)</sup>        |                                                 |      | 50   | 80   | ns               |

(1) Parameters ensured by design and/or characterization, if not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**

Unless otherwise stated, these specifications apply for  $R_T = 3.65 \text{ k}\Omega$ ,  $C_T = 1 \text{ nF}$ ,  $V_{CC} = 15 \text{ V}$ ,  $-55^\circ\text{C} < T_A < 125^\circ\text{C}$ ,  $T_A = T_J$

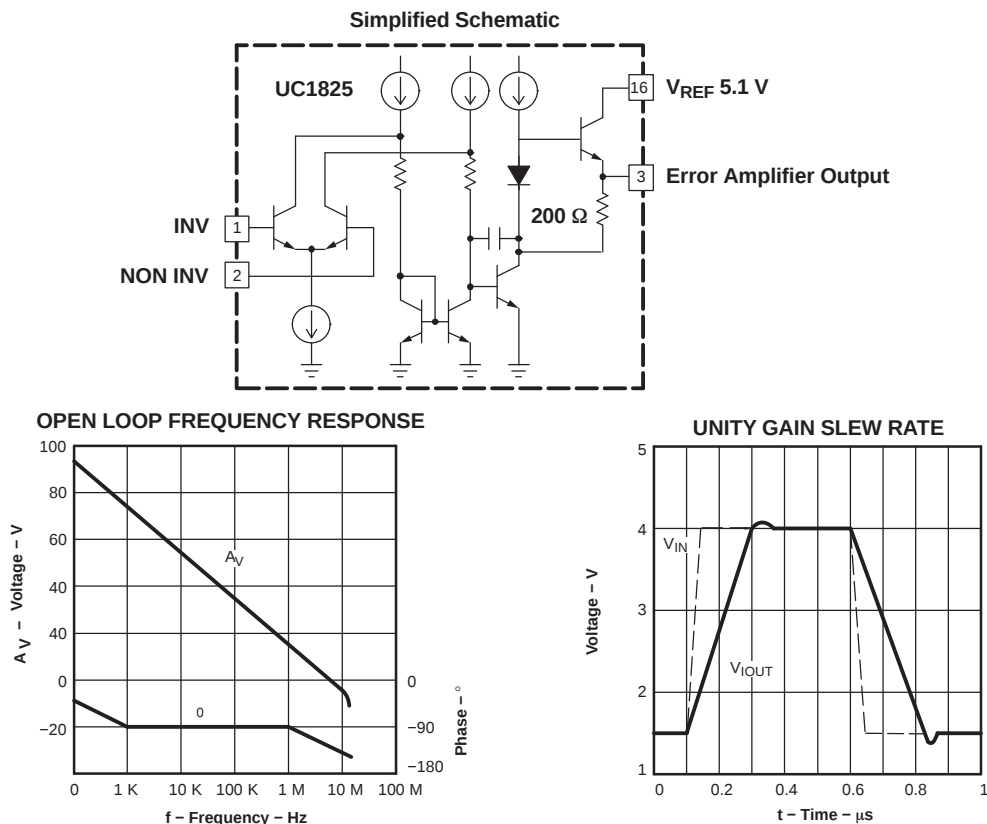
| PARAMETERS                    | TEST CONDITIONS                                                           | MIN  | TYP  | MAX  | UNIT          |
|-------------------------------|---------------------------------------------------------------------------|------|------|------|---------------|
| <b>OUTPUT</b>                 |                                                                           |      |      |      |               |
| Low-level output voltage      | $I_{OUT} = 20 \text{ mA}$                                                 |      | 0.25 | 0.40 | V             |
|                               | $I_{OUT} = 200 \text{ mA}$                                                |      | 1.2  | 2.2  | V             |
| High-level output voltage     | $I_{OUT} = -20 \text{ mA}$                                                | 13.0 | 13.5 |      | V             |
|                               | $I_{OUT} = -200 \text{ mA}$                                               | 12.0 | 13.0 |      | V             |
| Collector leakage             | $V_C = 30 \text{ V}$                                                      |      | 10   | 500  | $\mu\text{A}$ |
| Rise/fall time <sup>(2)</sup> | $C_L = 1 \text{ nF}$                                                      |      | 30   | 75   | ns            |
| <b>UNDER-VOLTAGE LOCKOUT</b>  |                                                                           |      |      |      |               |
| Start threshold               |                                                                           | 8.8  | 9.2  | 9.6  | V             |
| UVLO hysteresis               |                                                                           | 0.4  | 0.8  | 1.2  | V             |
| <b>SUPPLY CURRENT SECTION</b> |                                                                           |      |      |      |               |
| Startup current               | $V_{CC} = 8 \text{ V}$                                                    |      | 1.1  | 2.5  | mA            |
| $I_{CC}$                      | $V_{INV} = V_{Ramp} = V_{ILIM/SD} = 0 \text{ V}$ , $V_{NI} = 1 \text{ V}$ |      | 22   | 33   | mA            |

(2) Parameters ensured by design and/or characterization, if not production tested.

## PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

High speed circuits demand careful attention to layout and component placement. To ensure proper performance of the UC1825 follow these rules:

1. Use a ground plane.
2. Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1-A Schottky diode at the output pin serves this purpose.
3. Bypass  $V_{CC}$ ,  $V_C$ , and  $V_{REF}$ . Use 0.1- $\mu$ F monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1-cm of total lead length for each capacitor between the bypassed pin and the ground plane.
4. Treat the timing capacitor,  $C_T$ , like a bypass capacitor.



**Figure 2. Error Amplifier**

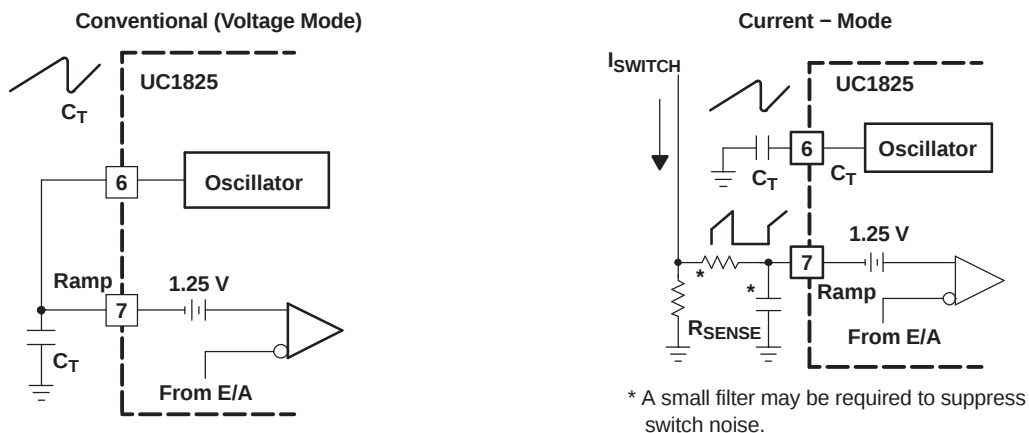


Figure 3. PWM Applications

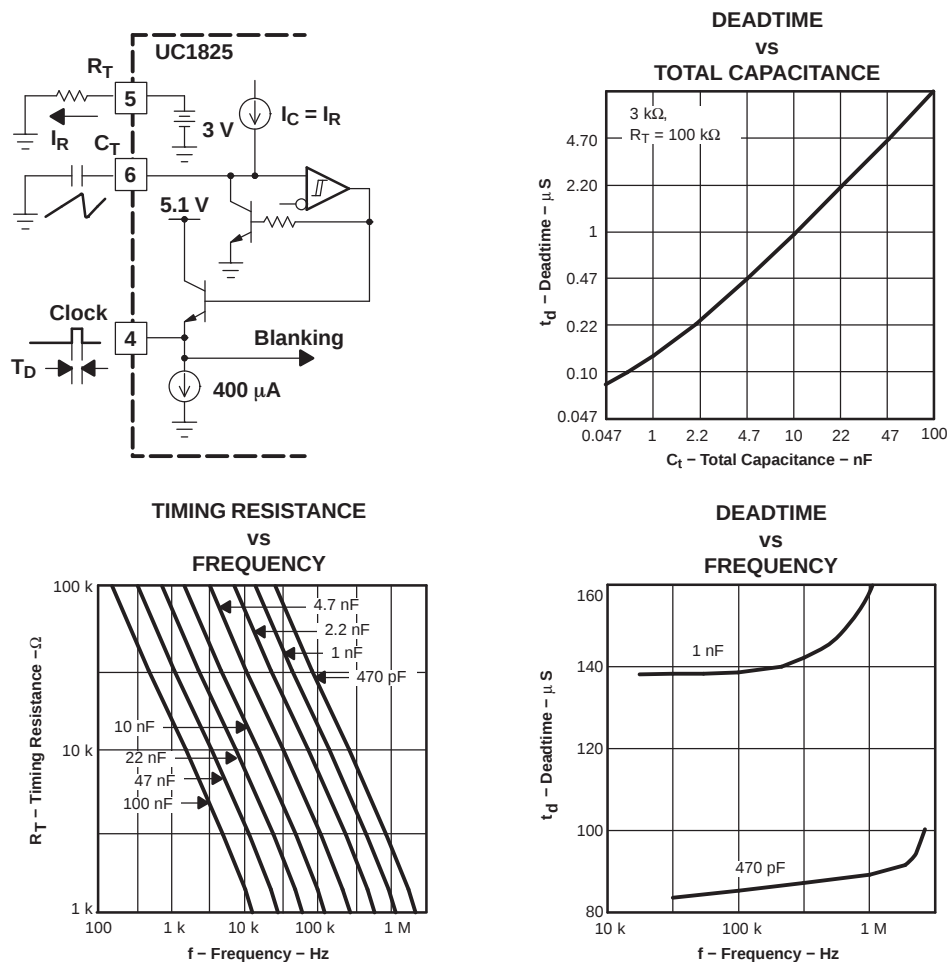


Figure 4. Oscillator Circuit

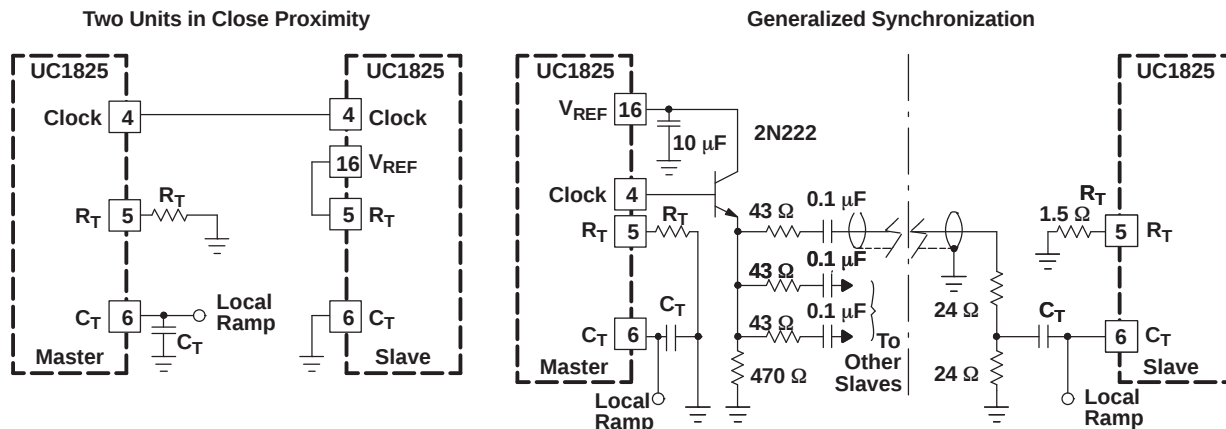


Figure 5. Synchronized Operation

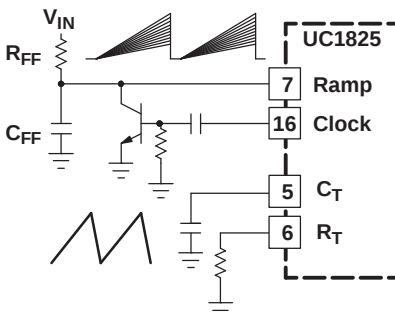


Figure 6. Forward Technique for Off-Line Voltage Mode Application

The circuit shown in Figure 6 will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components,  $R_T$  and  $C_T$  are chosen so that the ramp at the ILIM/SD pin crosses the 1-V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

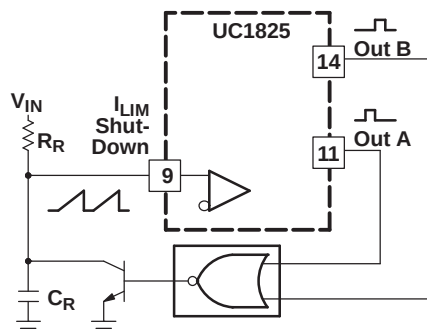


Figure 7. Constant Volt-Second Clamp Circuit

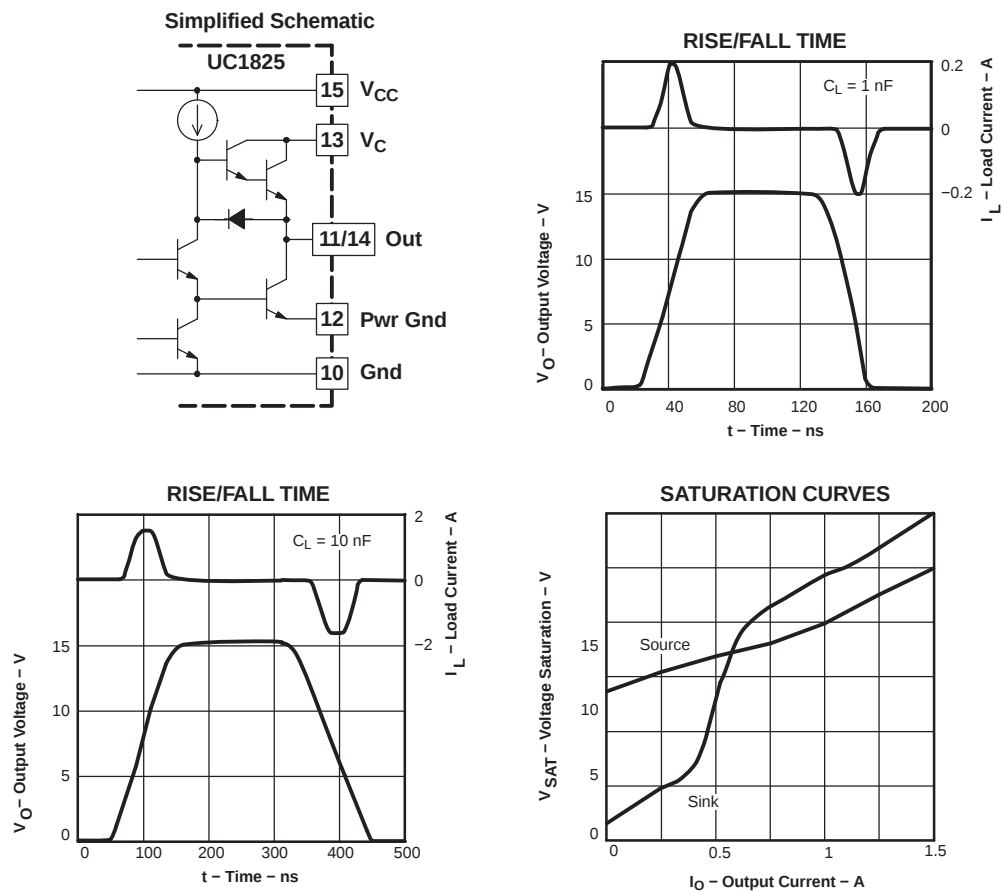
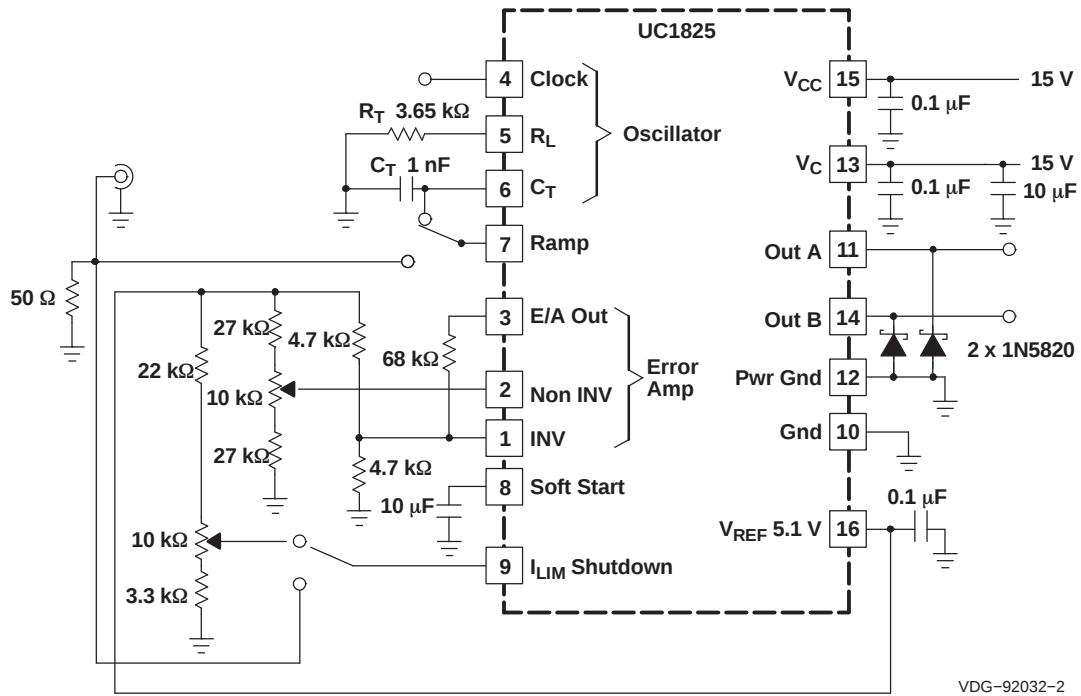
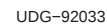


Figure 8. Output Section

The circuit in [Figure 8](#) is useful for exercising many of the UC1825 functions and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.



**Figure 9. Open-Loop Laboratory Test Fixture**



**Figure 10. Design Example: 50 W, 48-V to 5-V DC-to-DC Converter – 1.5-MHz Clock Frequency**

## REVISION HISTORY

### Changes from Original (January, 2009) to Revision A

### Page

- Added MAX spec of 16% to temperature stability parameter ..... [5](#)

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| 5962-8768101V2A  | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE           | N / A for Pkg Type           |                             |
| 5962-8768101VEA  | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42                  | N / A for Pkg Type           |                             |
| 5962-8768104V2A  | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE           | N / A for Pkg Type           |                             |
| 5962-8768104VEA  | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42                  | N / A for Pkg Type           |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UC1825-SP :**

- Catalog: [UC1825](#)

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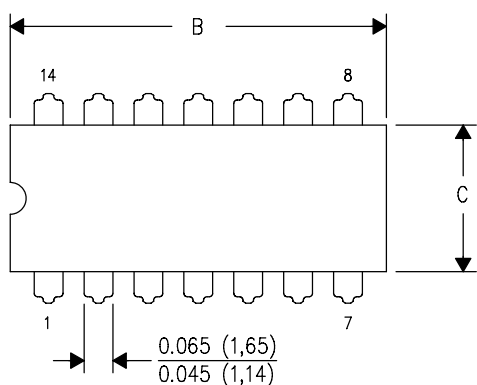
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

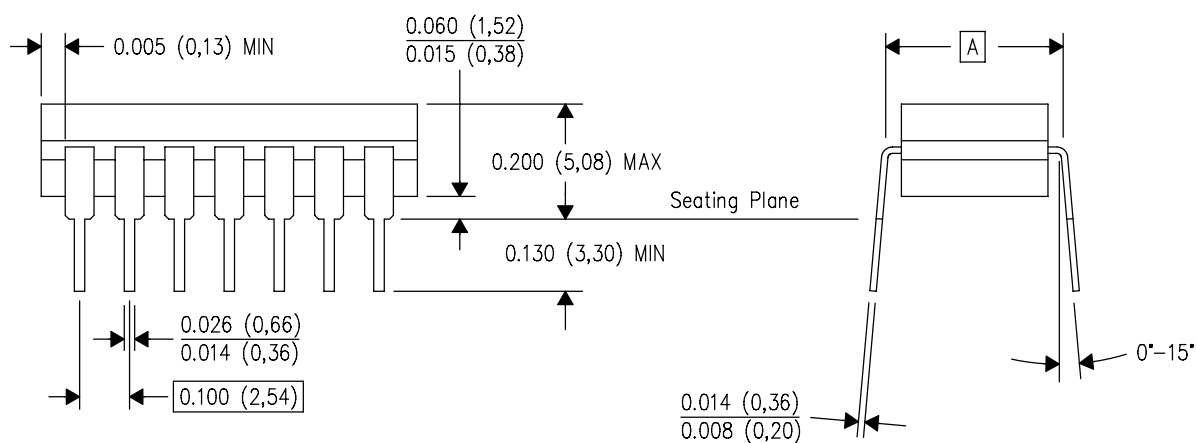
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



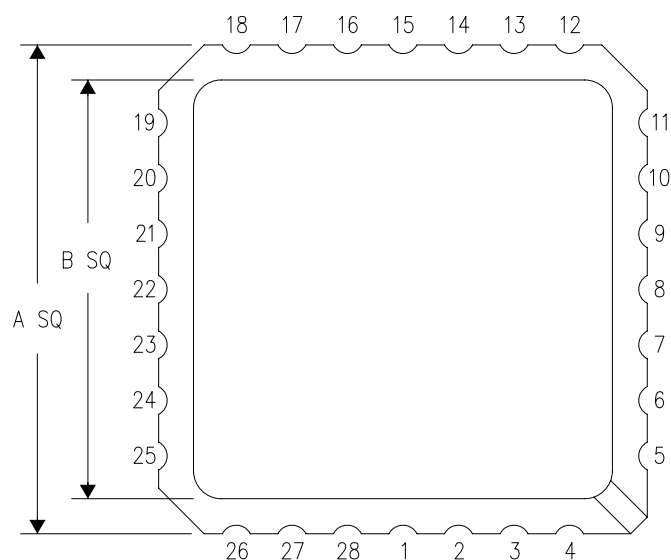
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

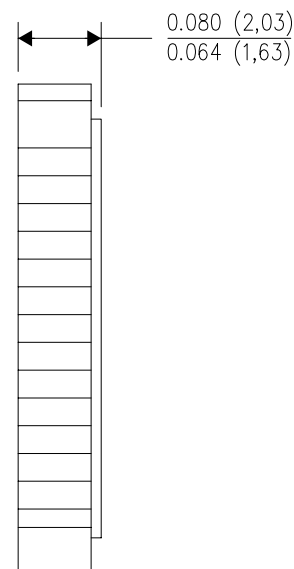
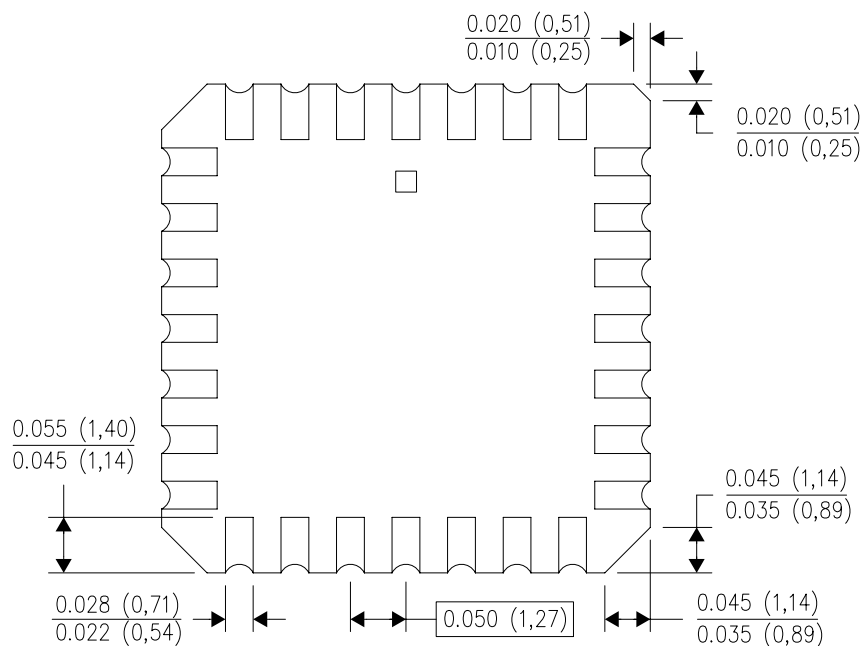
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

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| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
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### Applications

|                               |                                                                                          |
|-------------------------------|------------------------------------------------------------------------------------------|
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| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
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