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FUJITSU

DATA SHEET

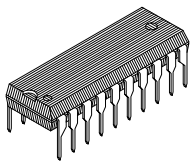
MB1514

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

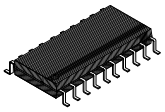
DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 400MHz PRESCALER

The Fujitsu MB1514 is a dual serial input PLL (phase locked loop) frequency synthesizer designed for cordless telephone applications.
The MB1514 has two PLL circuits on a single chip; one for transmission (PLL-1) and the other for reception (PLL-2). Separate power supply pins are provided for each PLL circuit. Transmission PLL contains a low sensitivity charge pump for modulation, and reception PLL contains a high sensitivity charge pump for fast lock-up time. 400MHz dual modulus prescalers are provided and enables a pulse swallow function.

MB1514 operates at 3.0 V typ. power supply voltage and dissipates 8mA typ. of current realized through the use of Bi-CMOS technology.



PLASTIC PACKAGE
DIP–20P–M02

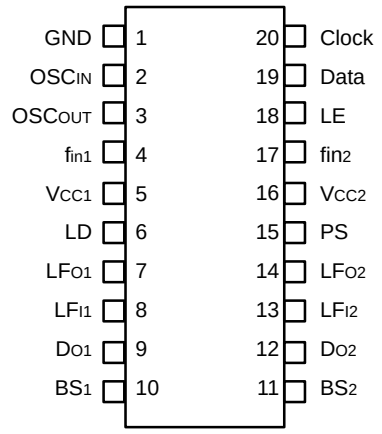


PLASTIC PACKAGE
FPT–20P–M01

FEATURES

- Low voltage operation : Vcc = 2.2V to 4.2V
- High operating frequency : fin = 400MHz (Pin = –10dBm, Vcc = 3.0V)
- Low current consumption : Icc = 8mA typ. (Vcc = 3V)
- Power saving function
- Two charge pumps
  Low sensitivity charge pump for transmission (PLL-1)
  High sensitivity charge pump for reception (PLL-2)
- Plastic 20-pin DIP package (Suffix: -P)
  Plastic 20-pin SOP package (Suffix: -PF)

PIN ASSIGNMENT



DIP–20P–M02/
FPT–20P–M01

ABSOLUTE MAXIMUM RATINGS

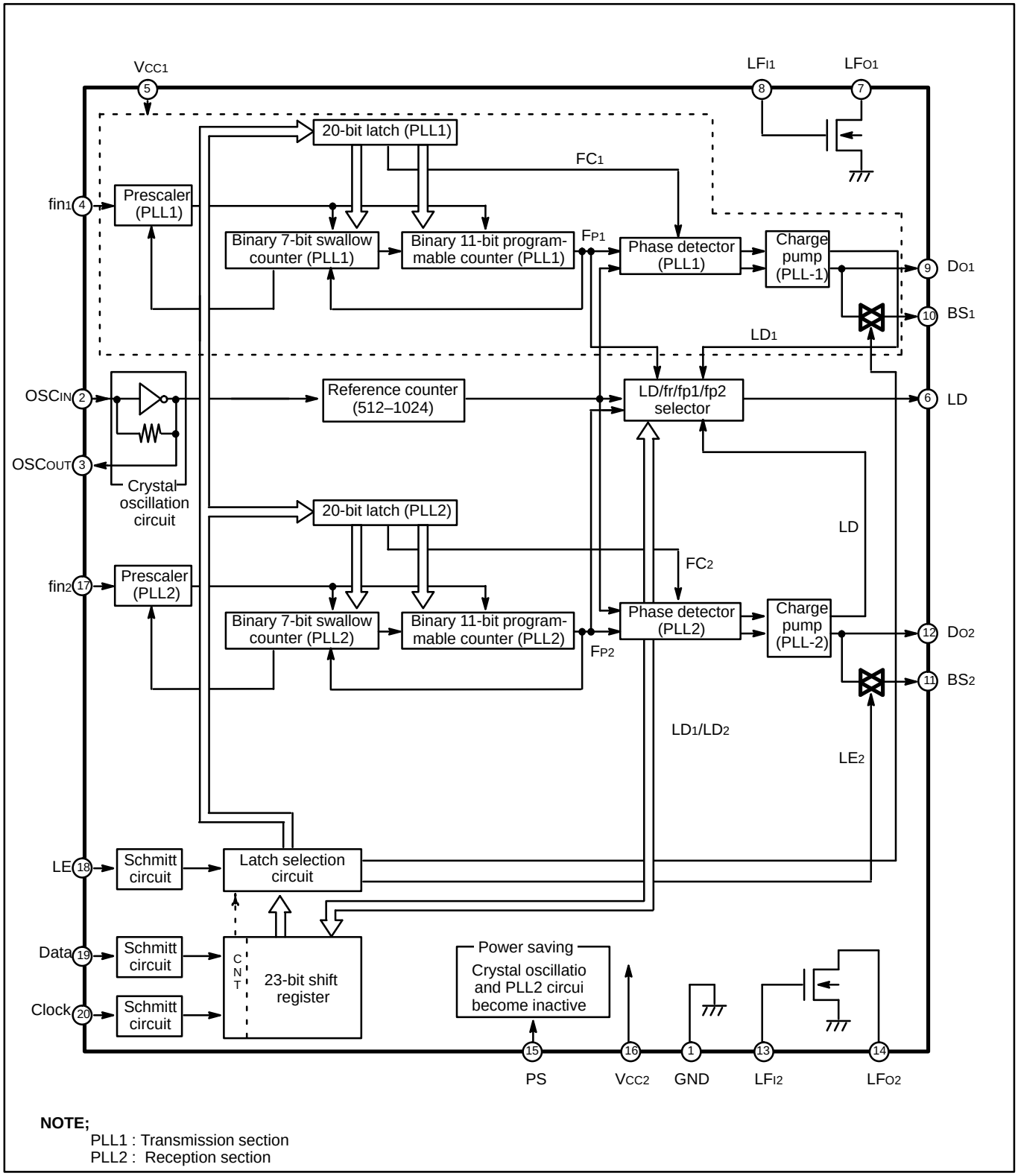
Ratings		Symbol	Value	Unit
Supply Voltage		V_{CC}	–0.5 to +6.0	V
Output Voltage	OSC_{OUT}, D_O, BS	V_{O1}	–0.5 to V_{CC}+0.5	V
	LD, LF_O	V_{O2}	–0.5 to +6.0	V
Output Current		I_O	±10	mA
Storage Temperature		T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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BLOCK DIAGRAM



NOTE;

PLL1 : Transmission section
PLL2 : Reception section

BLOCK DESCRIPTIONS

TRANSMISSION/RECEPTION BLOCK

- 20-bit latch
- Programmable divider;
  Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
  The programmable dividers for transmission and reception are able to be controlled independently.
- Phase detectors with phase polarity change function
- 400MHz dual modulus prescalers (Divide ratio: 64/65)
- Charge pumps
- Transistors for LPFs
- Analog swithes

COMMON BLOCK

- 23-bit shift register
- Reference divider;
  Reference counter (Divide ratio: 1700)
  (Divide frequency = 12.5 kHz (Crystal oscillator frequency = 12.8 kHz))
- Crystal oscillation circuit
- Latch selector
- Shmitt circuits
- LD/fr/fp output selector

PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Pin Descriptions
1	GND	–	Ground.
2 3	OSC_{IN} OSC_{OUT}	I O	Input and output of a reference divider and a crystal is externally connected between these pins.
4	fin_1	I	Input of a prescaler of PLL-1 (Transmission section). Connection with a VCO should be AC (capacitor) coupling.
5	V_{CC1}	–	Power supply for PLL-1 block. When power is cut off, PLL-1 block's latched data is cancelled.
6	LD	O	Output of lock detectors, a reference divider, and programmable dividers. Output data is selected by data setting of LD bits in the serial data. This is open-drain output.
7	LF_{O1}	O	Output of the transistor, used for transmission LPF.
8	LF_{I1}	I	Input of the transistor, used for transmission LPF.
9	D_{O1}	O	Output of the charge pump(PLL-1). Phase polarity is inverted by FC bit setting in the serial data.
10	BS_1	O	Output of the analog switch(PLL-1). Usually this pin is high-impedance state. When LE is set to high, the state of the internal charge pump is output.
11	BS_2	O	Output of the analog switch(PLL-2: reception section). Usually this pin is high-impedance state. When LE is set to high, the state of the internal charge pump is output.
12	D_{O2}	O	Output of the charge pump(PLL-2). Phase polarity is inverted by FC bit setting in the serial data.
13	LF_{I2}	I	Input of the transistor which is used for reception LPF.
14	LF_{O2}	O	Output of the transistor which is used for reception LPF.
15	PS	I	Power saving control for PLL-2 circuits.

PS	State
H	Active state
L	Power saving state (Crystal oscillation circuit and PLL2 circuits are inactive)

PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Pin Descriptions
16	V_{CC2}	–	Power supply for PLL-2 circuits, a reference counter, a shift register, and a crystal oscillation circuit. When power is cut off, PLL-2 block's and reference counter's latched data are cancelled.
17	f_{in2}	I	Input of a prescaler of PLL-2. Connection with a VCO should be AC (capacitor) coupling.
18	LE	I	Load enable signal input. This pin involves a schmitt trigger circuit. When this pin is high (LE="H"), the data stored in a shift register is transferred into the latch according to the control bit in the serial data. And at the moment, internal analog switch is closed(ON), then each charge pump output signal is output through the BS pin.
19	Data	I	Serial data input. This pin involves a schmitt trigger circuit. The stored data in the shift register is transferred to either transmission or reception sections depending upon the control bit as follows.
20	Clock	I	Clock input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. Each rising edge of the clock shifts one bit of data into the shift register.

Control bit data	The destination of data
H	Latch of PLL-1 (transmission)
L	Latch of PLL-2 (reception)

FUNCTIONAL DESCRIPTIONS

Divide ratio can be set using the following equation:

$f_{VCO} = \{ (M \times N) + A \} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of an external voltage controlled oscillator (VCO)
M: Preset divide ratio of an internal dual modulus prescaler (64)
N: Preset divide ratio of binary 12-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 5-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of reference counter (1700)

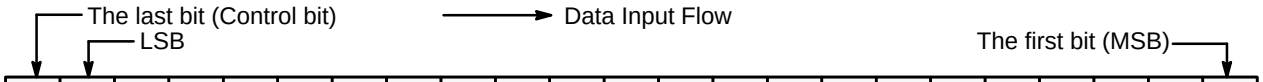
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is input using three pins; Data, Clock, and LE pins. Programmable dividers of PLL-1 and PLL-2 are controlled individually.
Serial data of binary data is input to the Data pin.
On rising edge of the clock shifts one bit of the data into the shift register.
When the load enable (LE) is high, the data stored in the shift register is transferred to either the latch of the transmission or the reception sections, depending upon the control bit setting.

Control bit data	The destination of data
H	Latch of PLL-1 (transmission)
L	Latch of PLL-2 (reception)

SHIFT REGISTER COSTITUTION



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CNT	LD1	LD2	DMY	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio of the programmable counter setting bit (16 to 2047)
A1 to A7 : Divide ratio of the swallow counter setting bit (0 to 127)
FC : Phase control bit of the phase detector
DMY : Dummy bit (set to ”L” as a rule)
LD2 : Select bit of LD output (LD, fr, fp1, fp2)
LD1 : Select bit of LD output (LD, fr, fp1, fp2)
CNT : Control bit

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

11-bit programmable counter divide ratio (N1 to N11)

Divide ratio	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2047	1	1	1	1	1	1	1	1	1	1	1

NOTE: Divide ratio less than 16 is prohibited.

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

7-bit swallow counter divide ratio (A1 to A7)

Divide ratio A	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
127	1	1	1	1	1	1	1

LD1, LD2 : LD OUTPUT SELECT

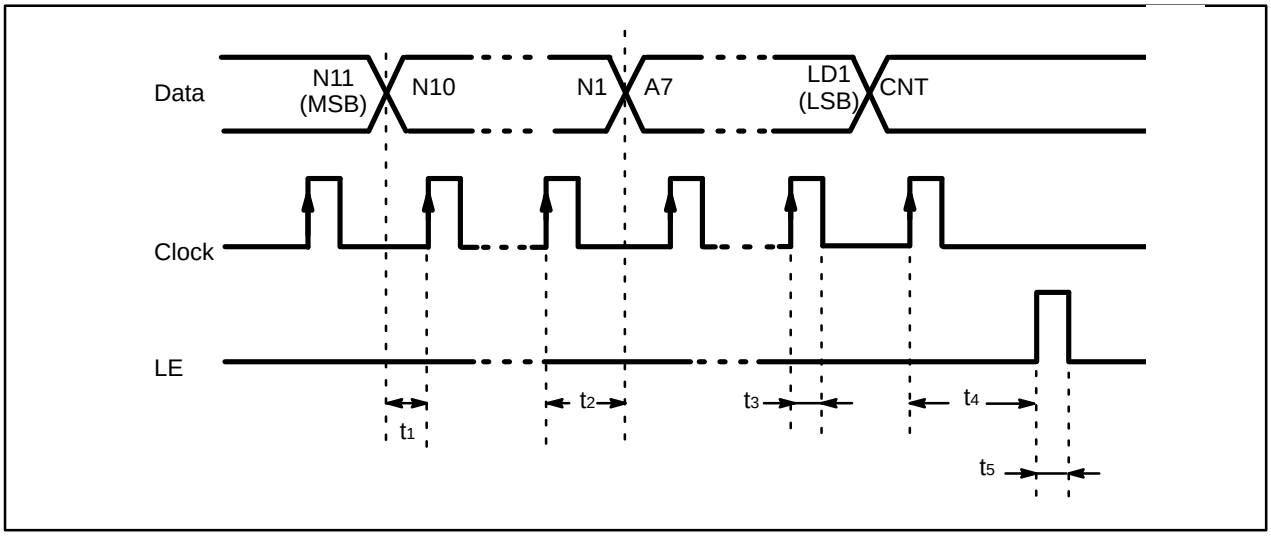
LD1	LD2	LD Output
1	1	Reference frequency (fr)
1	0	PLL-1 programmable frequency (fp1)
0	1	PLL-2 programmable frequency (fp2)
0	0	Lock detector output

DMY: DUMMY BIT

Set to ”L” as a rule

SERIAL DATA INPUT TIMING

t_1 (≥ 1 µs) : Data setup time t_2 (≥ 1 µs) : Data hold time t_3 (≥ 1 µs) : Clock pulse width
t_4 (≥ 1 µs) : LE setup time to the rising edge of the last clock t_5 (≥ 1 µs) : LE pulse width



NOTE: On rising edge of the clock shifts one bit of the data into the shift register.
When LE is high, the data stored in the shift register is transferred into the latch.

PHASE DETECTOR CHARACTERISTICS

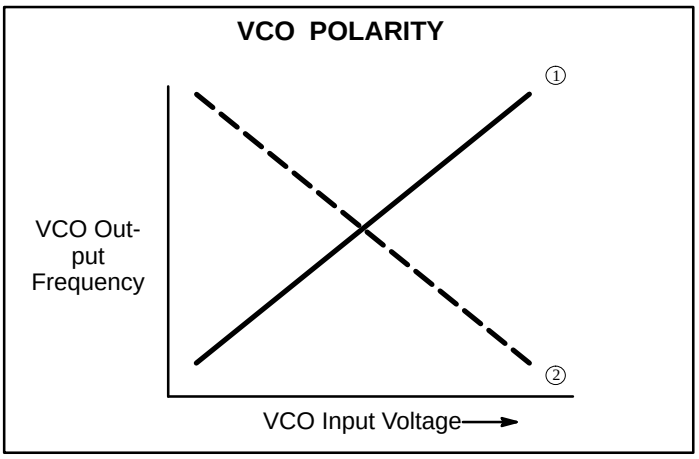
FC bit selects the phase of the phase detector. Phase characteristics (chage pump output) can be reversed depending upon the FC bit of the serial data. The phases of the charge pump outputs through LD pin are reversed depending upon the FC bit as well.

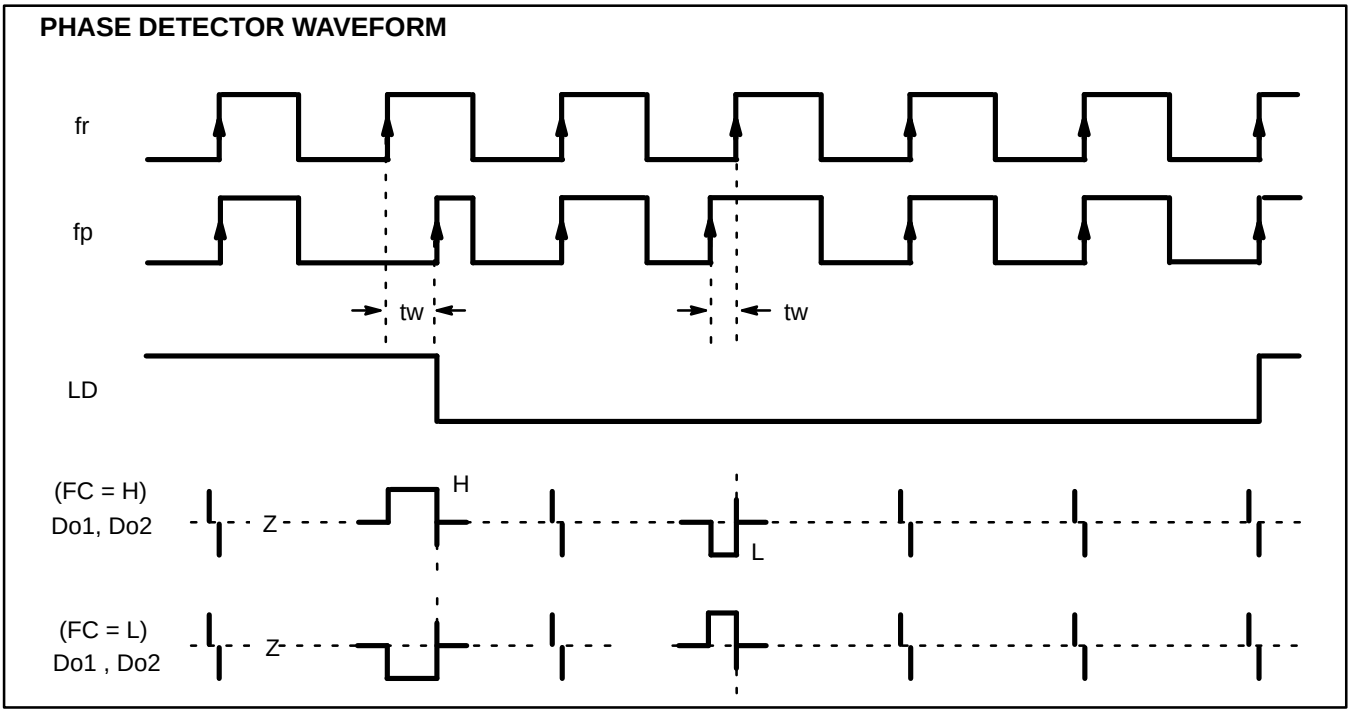
	FC = "H "	FC = "L"
	Do1, Do2, LD(fp1 & fp2) output	Do1, Do2, LD(fp1 & fp2) output
fr > fp	H	L
fr = fp	Z*	Z*
fr < fp	L	H

*Z: High-impedance

Depending upon the VCO polarity, FC pin should be set accordingly.

When VCO polarity is like① , the FC bit should be set at high.
When VCO polarity is like② , the FC bit should be set at low.





Note: Phase difference detection range : -2π to $+2\pi$
Spike shape depends on the charge pump characteristics. The spike is output to diminish the dead band.
LD output is "L" when the phase diference between the fr and fp is tw or more. When the phase difference is tw or less for three or more cycles, LD outputs "H". (When f_{osc}in is 21.25MHz, tw is 376ns to 753ns.)

STAND-BY MODE & LOCK DETECTOR (LD)

Setting the power saving control pin input level, the crystal oscillation circuit and PLL-2 circuits become inactive, then MB1514 enters lower current consumption state.

	PS pin	PLL-1	PLL-2	LD output
Transmit/Receive active mode	H	Lock	Lock	H
		Lock	Un-Lock	L
		Un-Lock	Lock	L
Receive active mode		Stand-by Vcc_1 = OFF	Lock	H
			Un-Lock	L
Stand-by mode	L*	Stand-by Vcc_1 = OFF	Stand-by	L

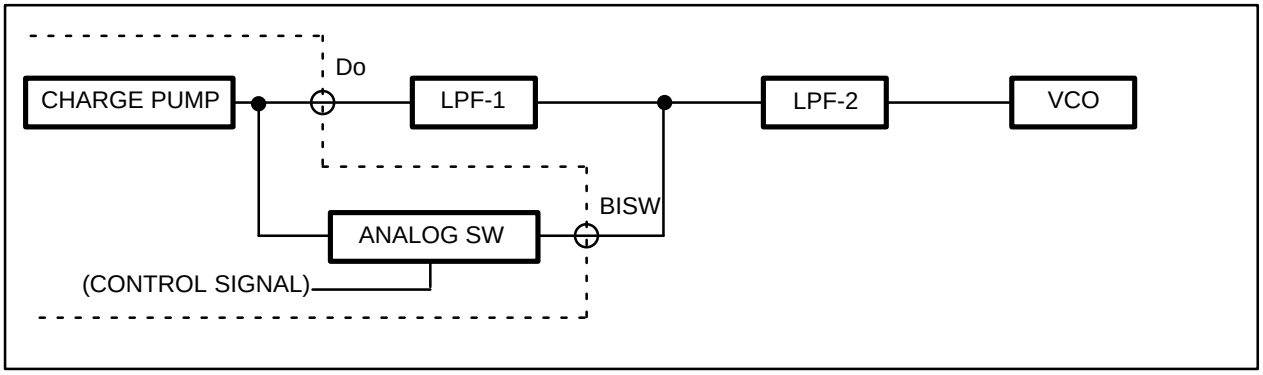
NOTE:When PS is ”L”, the charge pump (Do2) of the PLL-2 becomes high-impedance state.

ANALOG SWITCH

ON/OFF of the analog switch is controlled by the combination of the control data and LE signal. When the analog switch is ON, BS1, BS2 pins output the charge pump output (Do1, Do2). When the analog switch is OFF, BS pins are set to high-impedance state.

	Control data = H When the divide ratio of the PLL-1 is set.		**Control data = L When the divide ratio of the PLL-2 is set.**	
	LE = H	**LE = L**	**LE = H**	**LE = L**
Analog Switch of transmit section	ON	OFF	OFF	OFF
Analog Switch of receive section	OFF	OFF	ON	OFF

When an analog switch is inserted between LPF-1 and LPF-2, fast lock up is achieved by reducing LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	Vcc*	2.2	3.0	4.2	V
Input Voltage	V_{IN}	GND	–	V_{CC}	V
Ambient Temperature	Ta	–10		+70	°C

*: $V_{CC1} = V_{CC2}$

ELECTRICAL CHARACTERISTICS

($V_{CC1} = V_{CC2}$ = 2.2V to 4.2V, Ta = –10°C to + 70°C)

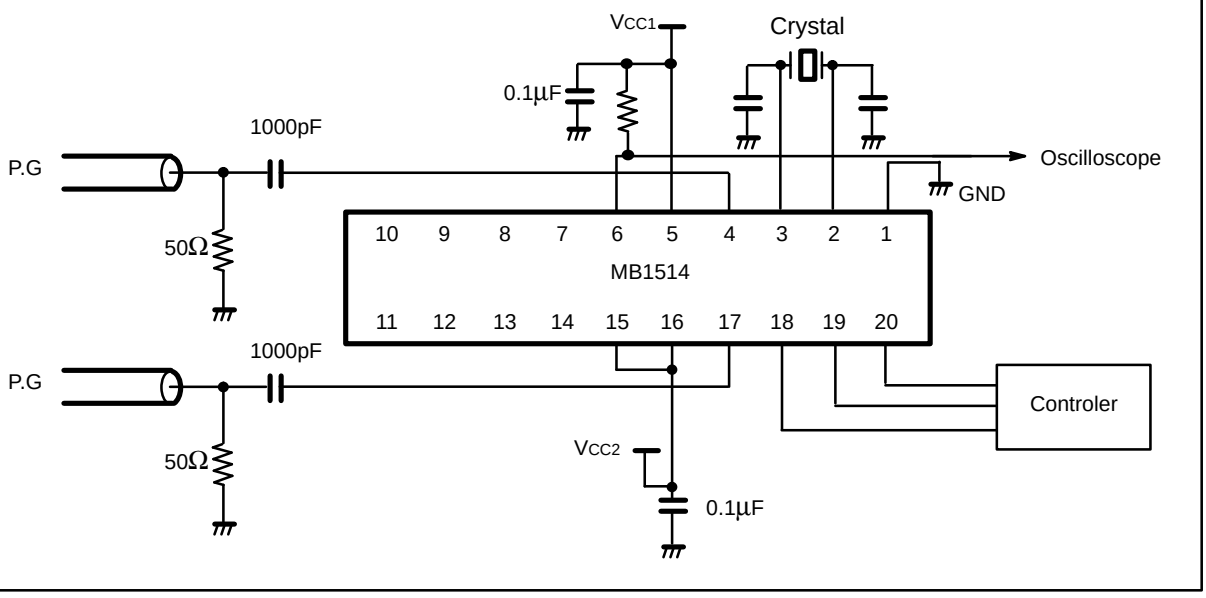
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC1}	PLL-2 Current	–	4.0	–	mA
		I_{CC2}	PLL-1 + PLL-2 Current	–	8.0	–	mA
Operating Frequency	fin	fin_1		10	–	400	MHz
	OSC_{IN}	f_{OSC}		–	21.25	–	
Input Sensitivity	fin	Pfin	50Ω system	–10	–	0	dBm
	OSC_{IN}	V_{OSC}		0.5	–	–	Vp-p
High–level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{CC}x0.7+0. 4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3–0.4	
High–level Input Current	Data, Clock, LE, PS	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	I_{OSC}			±50		
	LFi	I_{LF}				1.1	
High–level Output Voltage	Except D_O, OSC_{OUT}	V_{OSC}	V_{CC} = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OH}		–	–	0.4	
High–impedance Cutoff Current	D_O, LF_O	I_{OFF}		–	–	1.1	µA
	LD			–	–	10.0	
Output Current	Except D_O, OSC_{OUT}	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	

ELECTRICAL CHARACTERISTICS

(V_{CC1} = V_{CC2} = 2.2V to 4.2V, Ta = –10°C to + 70°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Output Current	D_{O1}	I_{OH}	V_{CC} = 3.0V	–	–0.5	–	mA
		I_{OL}	V_{CC} = 3.0V	–	12	–	mA
	D_{O2}	I_{OH}	V_{CC} = 3.0V	–	–1.5	–	mA
		I_{OL}	V_{CC} = 3.0V	–	6	–	mA
Analog Switch ON Resistance		Ron		–	50	–	Ω

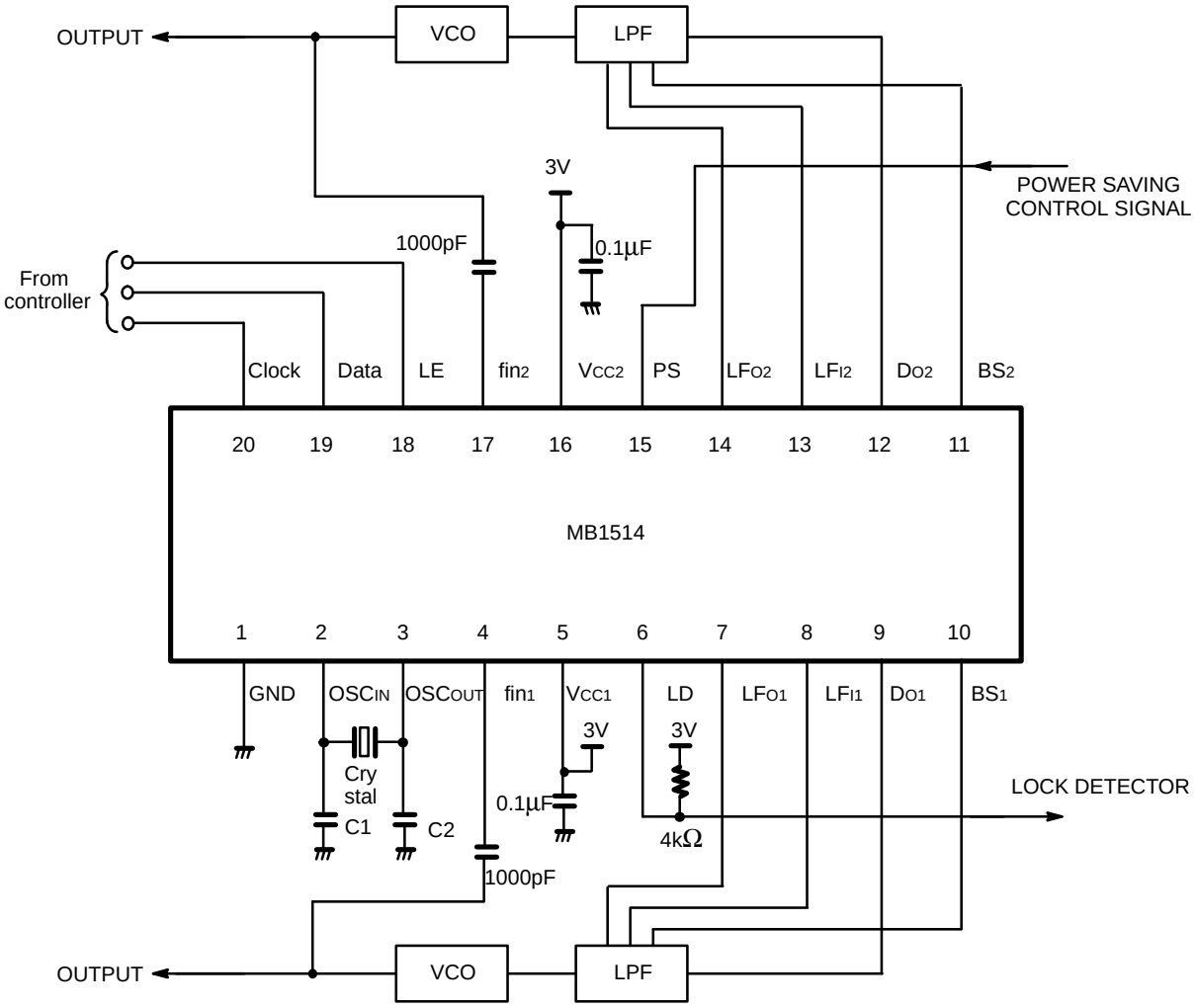
TEST CIRCUIT (FOR PRESCALER INPUT SENSITIVITY)



HANDLING PRECAUTION

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC bords with devices.

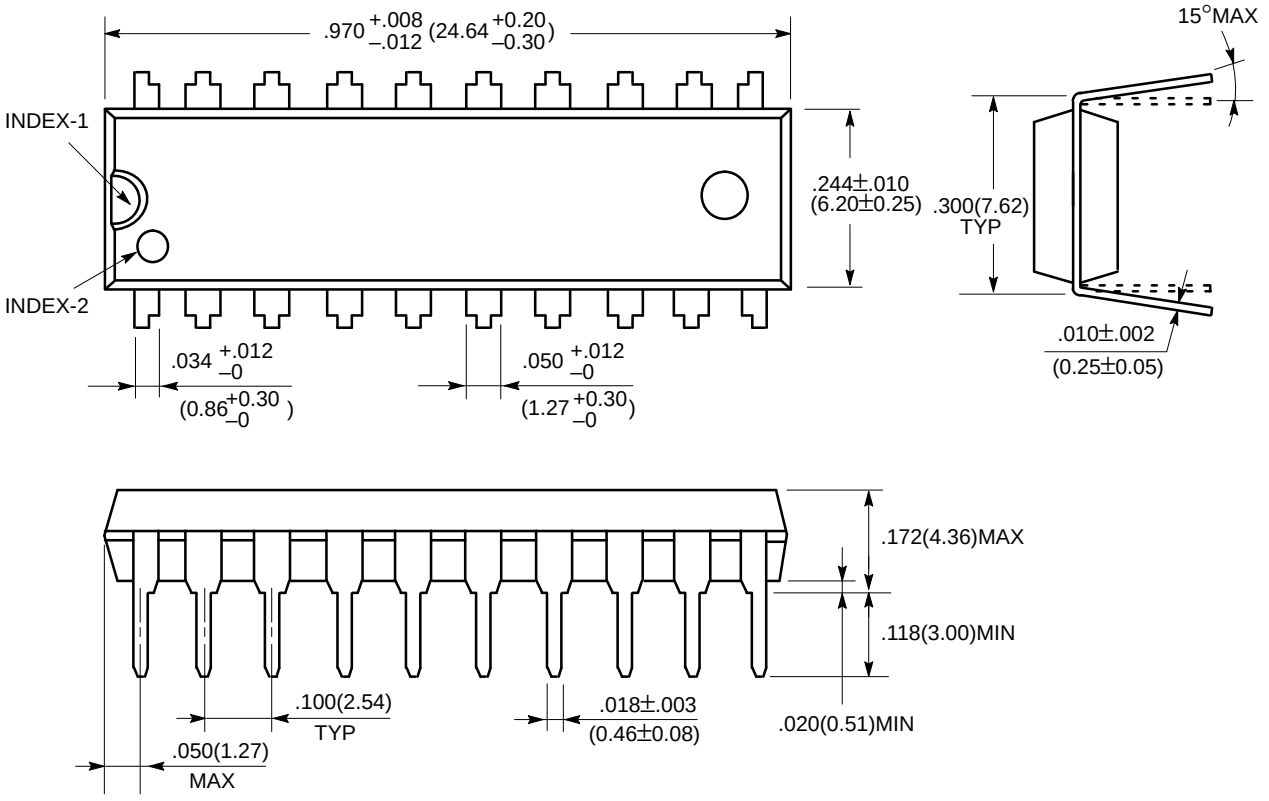
APPLICATION EXAMPLE



NOTE;
C1, C2 : depends on the crystal oscillator.
Clock, Data, LE : Using shmitt trigger circuits (When inputs are left open, pull-down or pull-up resistors are necessary to prevent oscillation.)
Crystal : 21.25MHz
LD : Open drain

PACKAGE DIMENTIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)

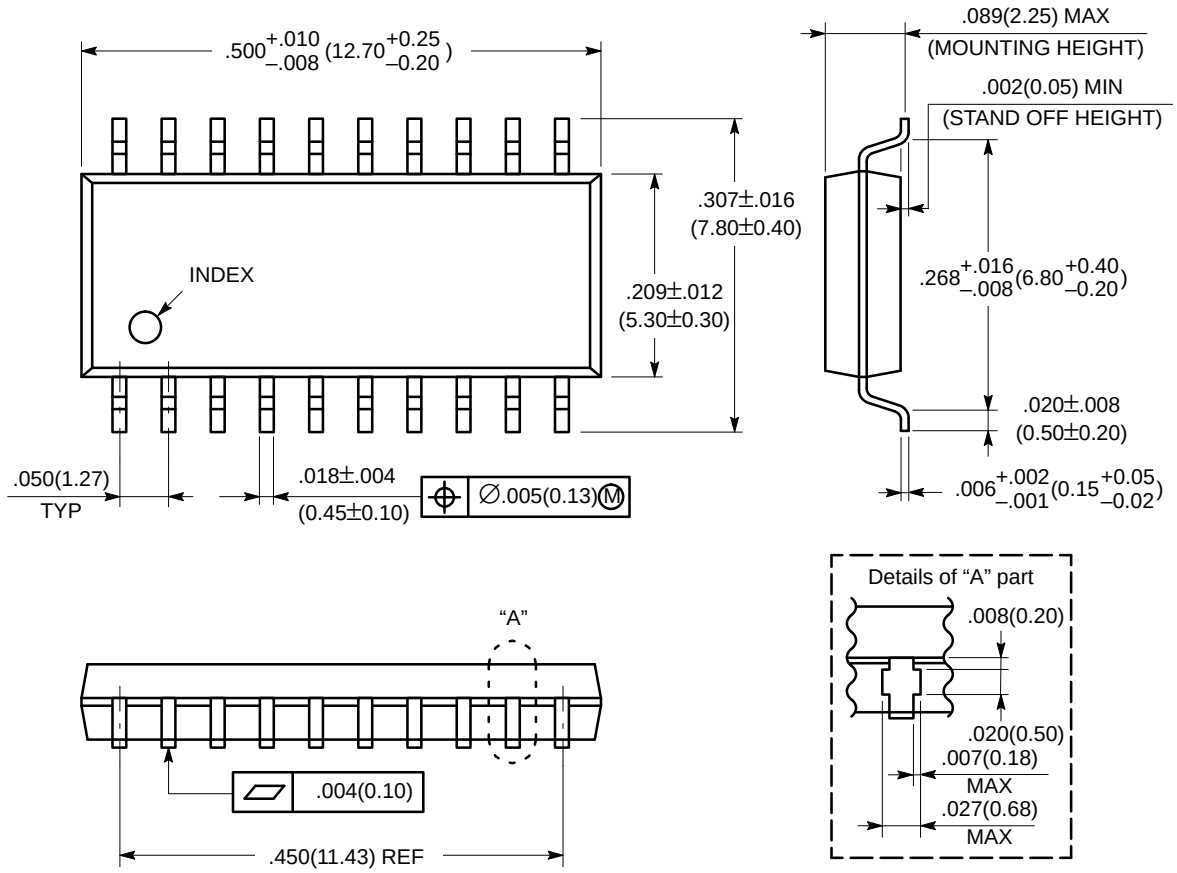


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Dimensions in
inches (millimeters)

PACKAGE DIMENTIONS (Continued)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



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