

HM674100H Series

1,048,576-word × 4-bit High Speed Static Random Access Memory

HITACHI

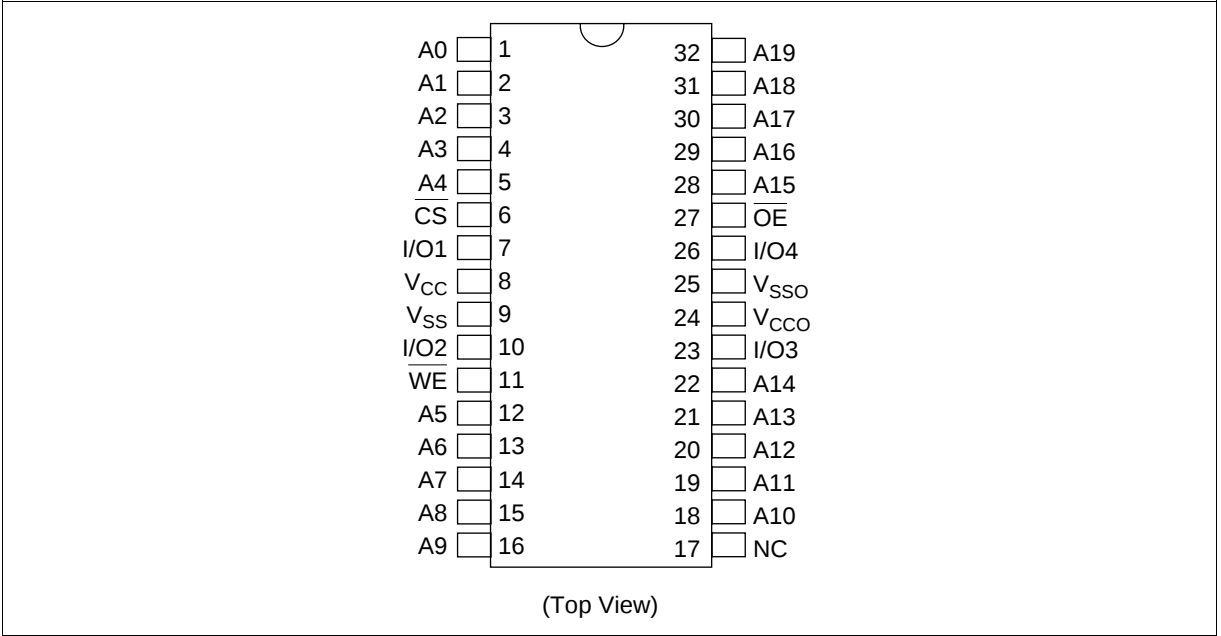
Features

- 1,048,576-word × 4-bit organization.
- Directly TTL compatible input and output.
- +5 V Single supply.
- Completely static memory.
- No clock or timing strobe required.
- Super fast access time: 15/20/25 ns (max).
- Revolutionary pin arrangement.

Ordering Information

Type No.	Access Time	Package
HM674100HJP-15	15 ns	400 mil 32 pin plastic SOJ (CP-32DB)
HM674100HJP-20	20 ns	
HM674100HJP-25	25 ns	

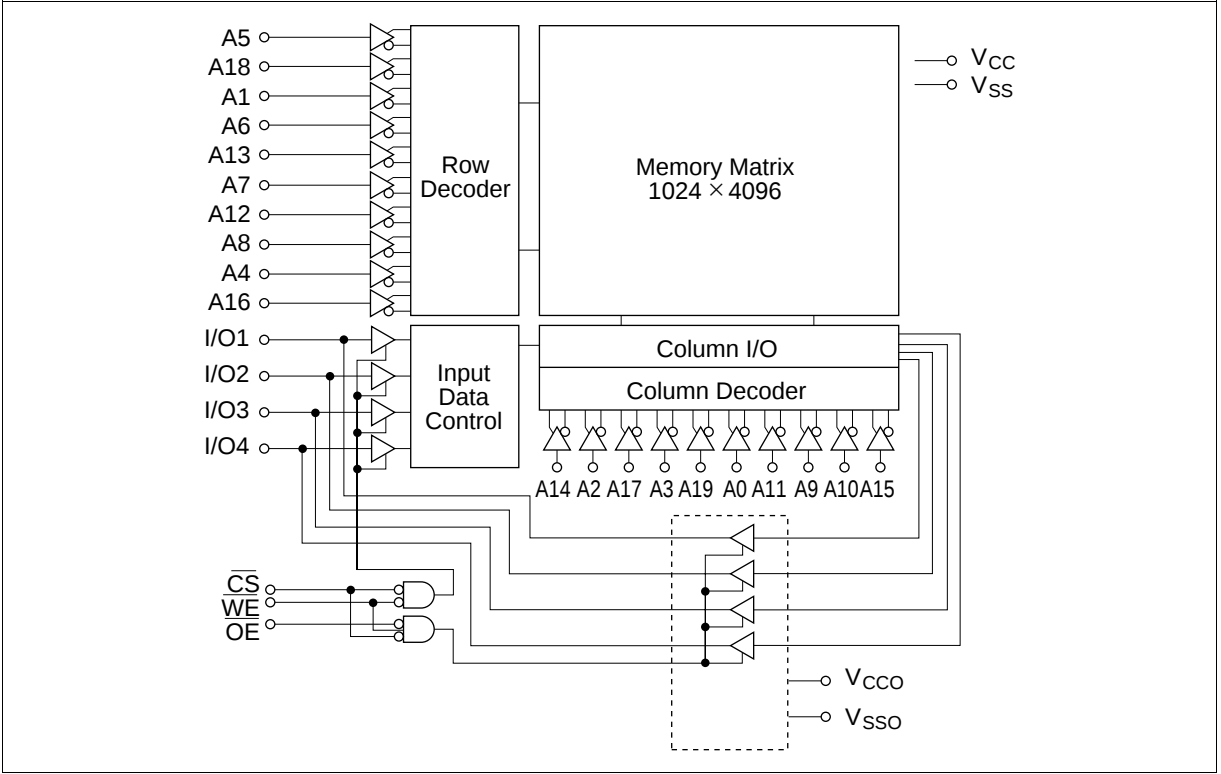
Pin Arrangement



Pin Description

Pin Name	Function
A0 to A19	Address input
I/O1 to I/O4	input/output
WE	Write enable
CS	Chip select
OE	Output enable
V _{CC}	+5 V Power supply
V _{CCO}	Output buffer power supply
V _{SSO}	Output buffer ground
V _{SS}	Ground
NC	Not connect

Block Diagram



Function Table

Input			Mode	I/O Pin	V _{CC} Current	Ref. Cycle
$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$				
H	X	X	Not selected	High-Z	$I_{\text{SB}}, I_{\text{SB1}}$	—
L	H	H	Output disabled	High-Z	$I_{\text{CC}}, I_{\text{CC1}}$	—
L	H	L	Read	Data Out	$I_{\text{CC}}, I_{\text{CC1}}$	Read Cycle (1), (2), (3)
L	L	H	Write	Data In	$I_{\text{CC}}, I_{\text{CC1}}$	Write Cycle (1), (2), (3), (4)
L	L	L	Write	Data In	$I_{\text{CC}}, I_{\text{CC1}}$	Write Cycle (5), (6)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ^{*1}	V _{CC}	−0.5 to +7.0	V
Voltage on any pin relative to V _{SS} ^{*1}	V _T	−0.5 to V _{CC} + 0.5	V
Power dissipation	P _T	1.0/1.5 ^{*2}	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (Bias)	−10 to +85	°C
Storage temperature range	Tstg	−55 to +125	°C

- Notes: 1 With respect to V_{SS} = V_{SSO}
- 2 P_T = 1.5 W is guaranteed under the minimum air flow exceeding 500 linear feet per minute. Under the DC and AC specifications shown in the Tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC} , V _{CCO}	4.5	5.0	5.5	V
	V _{SS} , V _{SSO}	0.0	0.0	0.0	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
Input low voltage	V _{IL}	−0.5	—	0.8	V

DC Characteristics (V_{CC} = V_{CCO} = 5.0 V ±10%, V_{SS} = V_{SSO} = 0 V, Ta = 0 to +70°C)

		HM674100H							
		-15		-20		-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Input leakage current	I _{LI}	—	2	—	2	—	2	μA	V _{CC} = 5.5 V, V _{IN} = 0 V to V _{CC}
Output leakage current	I _{LO}	—	10	—	10	—	10	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$, $\overline{WE} = V_{IL}$, V _{I/O} = 0 V to V _{CC}
Operating power supply current	I _{CC}	—	120	—	120	—	120	mA	$\overline{CS} = V_{IL}$, I _{I/O} = 0 mA
Average operating current	I _{CC1}	—	220	—	200	—	160	mA	min cycle, I _{I/O} = 0 mA
Standby power supply current	I _{SB}	—	100	—	80	—	60	mA	$\overline{CS} = V_{IH}$, V _{IN} = V _{IH} or V _{IL}
	I _{SB1}	—	10	—	10	—	10	mA	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$ V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V
Output low voltage	V _{OL}	—	0.4	—	0.4	—	0.4	V	I _{OL} = 8 mA
Output high voltage	V _{OH}	2.4	—	2.4	—	2.4	—	V	I _{OH} = -4 mA

Capacitance (Ta = 25°C, f = 1 MHz)

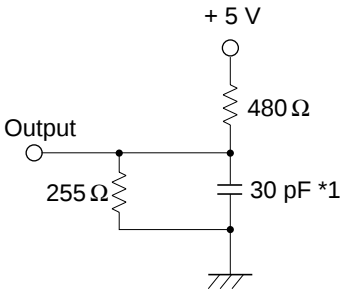
Parameter	Symbol	Max	Unit	Test Conditions
Input capacitance	C _{IN} ^{*1}	6	pF	V _{IN} = 0 V
Input/Output capacitance	C _{I/O} ^{*1}	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

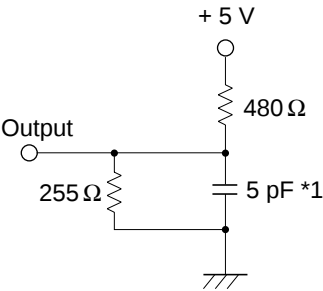
AC Characteristics ($V_{CC} = V_{CCO} = 5\text{ V} \pm 10\%$, $V_{SS} = V_{SSO} = 0\text{ V}$, $T_a = 0\text{ to } +70^\circ\text{C}$, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5V
- Input rise and fall time: 4 ns
- Output reference levels: 1.5 V
- Output Load: See figure



Output Load A



Output Load B

(for t_{HZ} , t_{LZ} , t_{OHZ} , t_{OLZ} , t_{WZ} , & t_{OW})

Note: including scope and jig capacitance

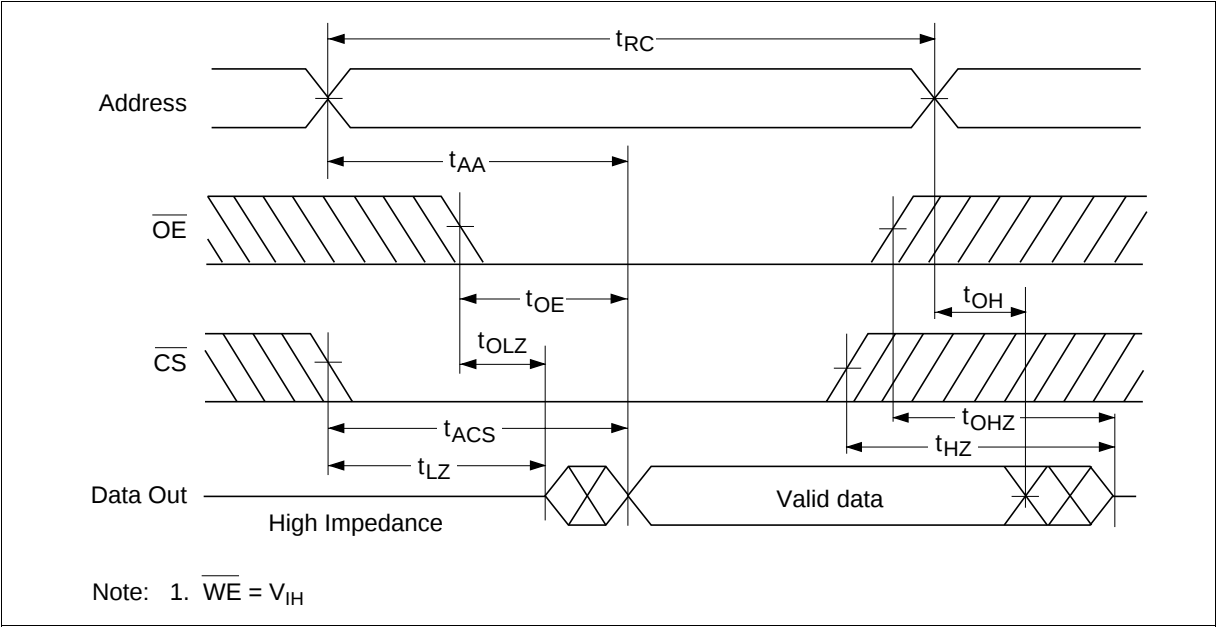
Read Cycle

		HM674100H						
		-15		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Read cycle time	t _{RC}	15	—	20	—	25	—	ns
Address access time	t _{AA}	—	15	—	20	—	25	ns
Chip select access time	t _{ACS}	—	15	—	20	—	25	ns
Chip selection to output in low-Z	t _{LZ} ^{*1,*2}	5	—	5	—	5	—	ns
Output enable to output Valid	t _{OE}	—	8	—	10	—	15	ns
Output enable to output in low-Z	t _{OLZ} ^{*1,*2}	2	—	2	—	2	—	ns
Chip deselection to output in high-Z	t _{HZ} ^{*1,*2}	0	7	0	8	0	15	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns

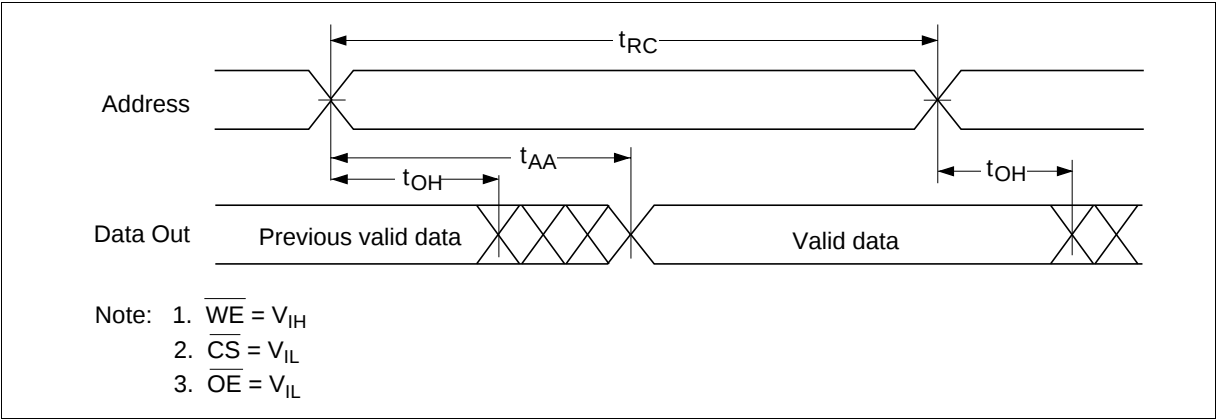
Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

Timing Waveforms

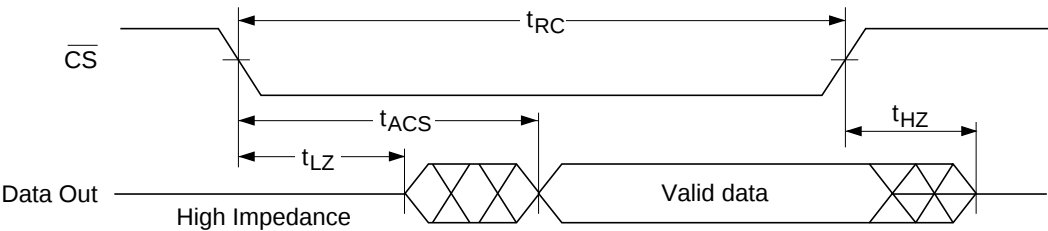
Read Cycle-1



Read Cycle-2



Read Cycle-3



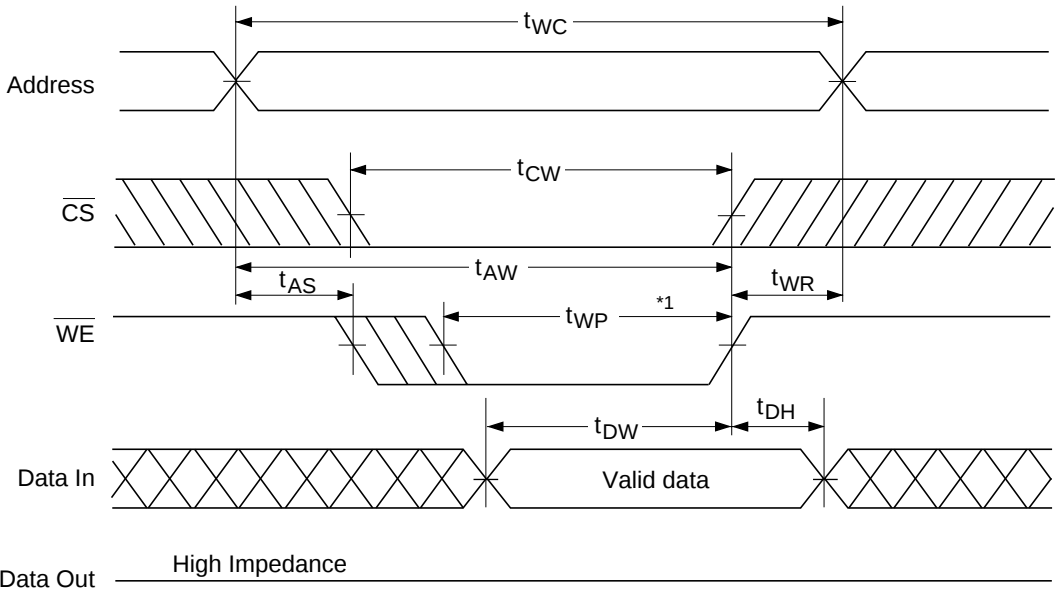
- Note: 1. $\overline{\text{WE}} = V_{\text{IH}}$
2. $\overline{\text{OE}} = V_{\text{IL}}$
3. Address valid prior to or coincident with $\overline{\text{CS}}$ transition low.

Write Cycle

		HM674100H						
		-15		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Write cycle time	t _{WC} ^{*1}	15	—	20	—	25	—	ns
Chip selection to end of write	t _{CW}	12	—	15	—	17	—	ns
Address valid to end of write	t _{AW}	12	—	15	—	17	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	12	—	15	—	17	—	ns
Write recovery time	t _{WR}	3	—	3	—	3	—	ns
Data valid to end of write	t _{DW}	8	—	10	—	15	—	ns
Data hold time	t _{DH}	0	—	0	—	0	—	ns
Write enable to output in high Z	t _{WZ} ^{*2, *3}	0	7	0	8	0	12	ns
Output disable to output in high Z	t _{OHZ} ^{*2, *3}	0	7	0	8	0	10	ns
Output active from end of write	t _{OW} ^{*2, *3}	2	—	2	—	2	—	ns

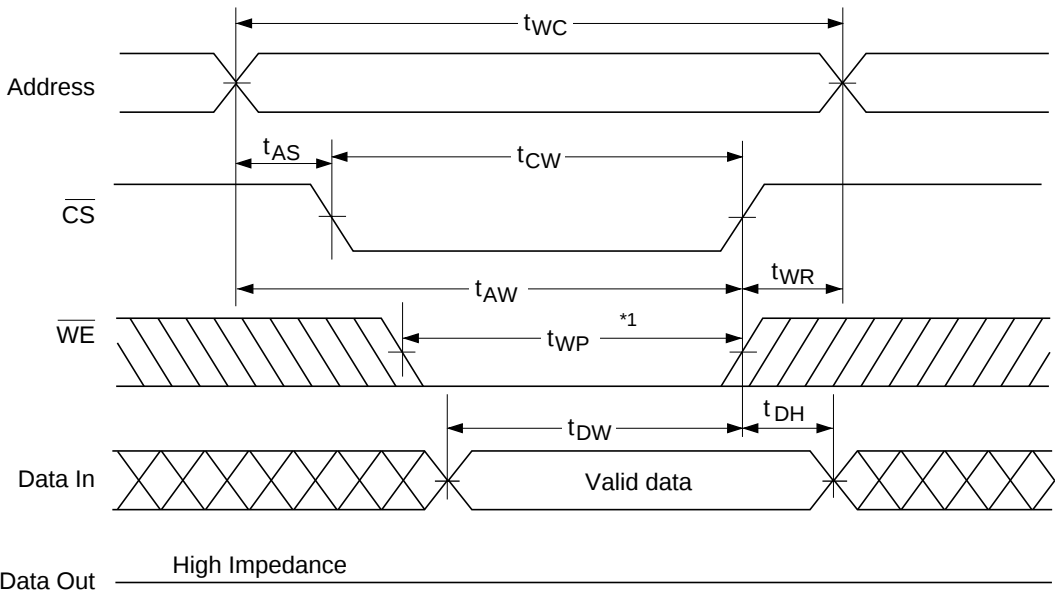
- Notes: 1. All write cycle timings are referred from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

Write Cycle-1 ($\overline{OE} = H$, $\overline{WE}$ Controlled)



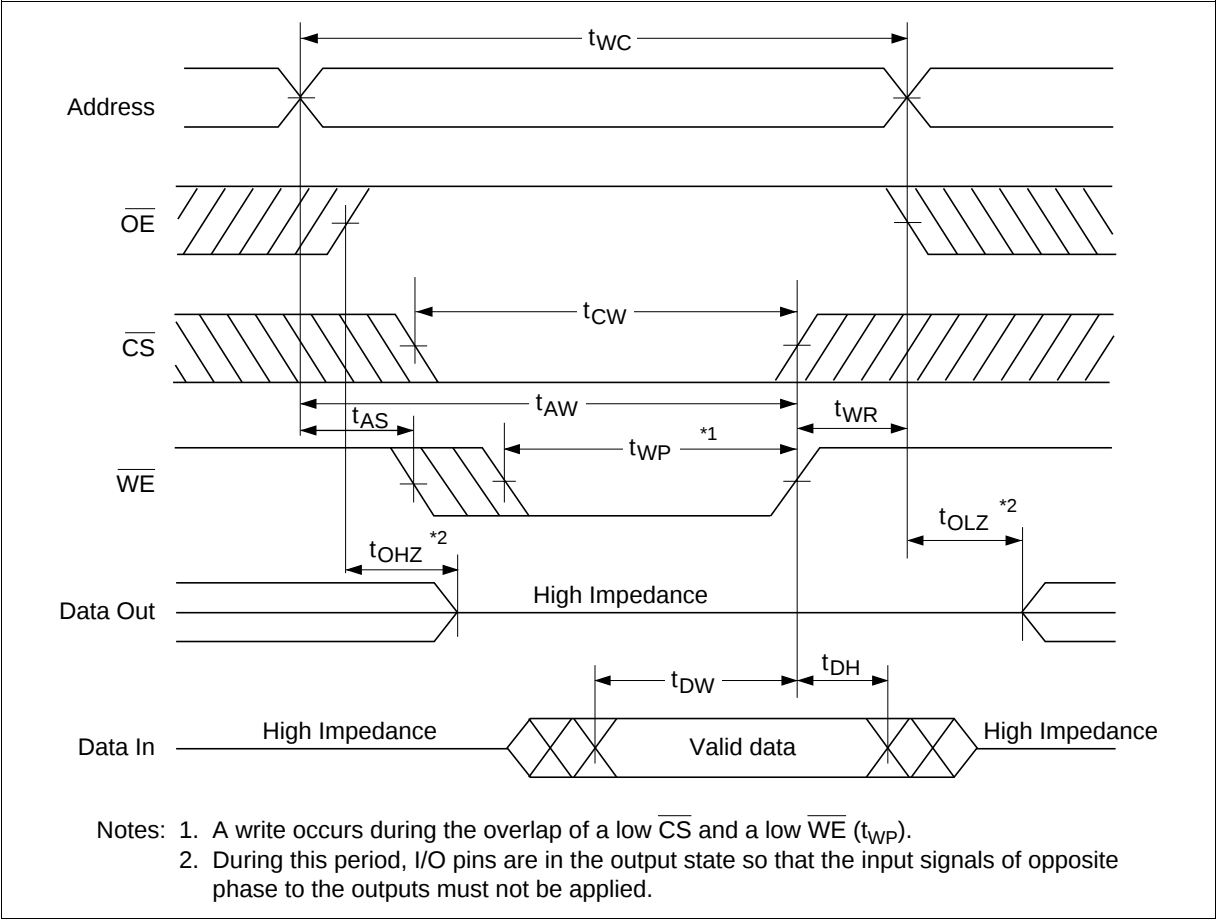
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle-2 ($\overline{OE} = H$, $\overline{CS}$ Controlled)

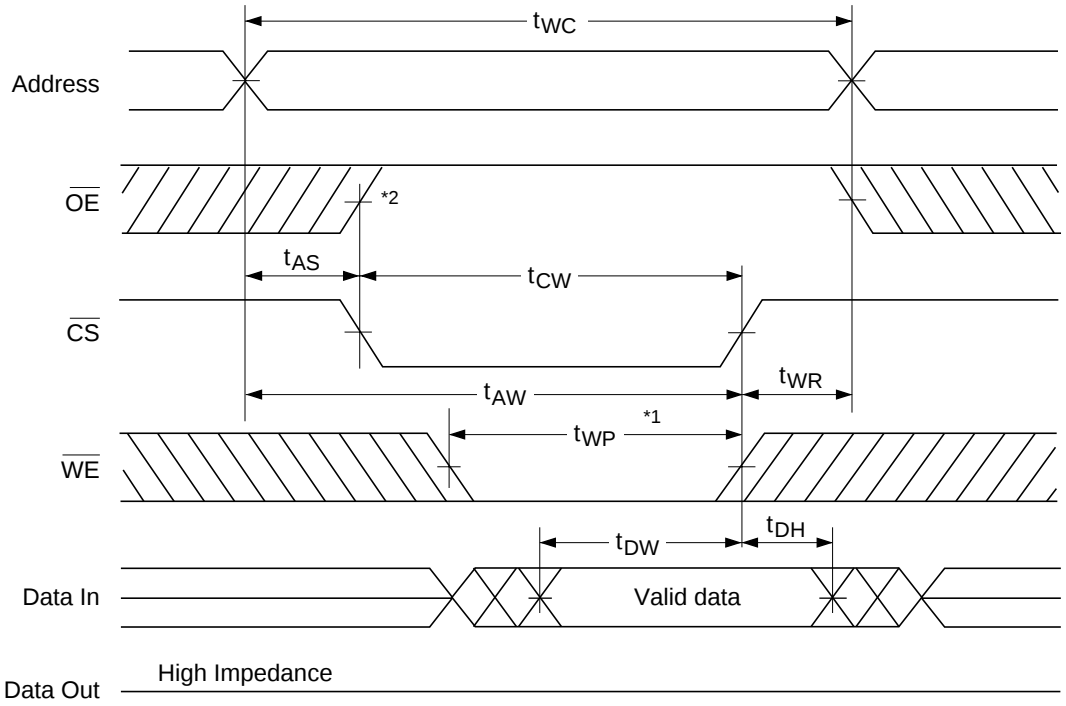


Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle-3 ($\overline{\text{OE}}$ = Clocked, $\overline{\text{WE}}$ Controlled)

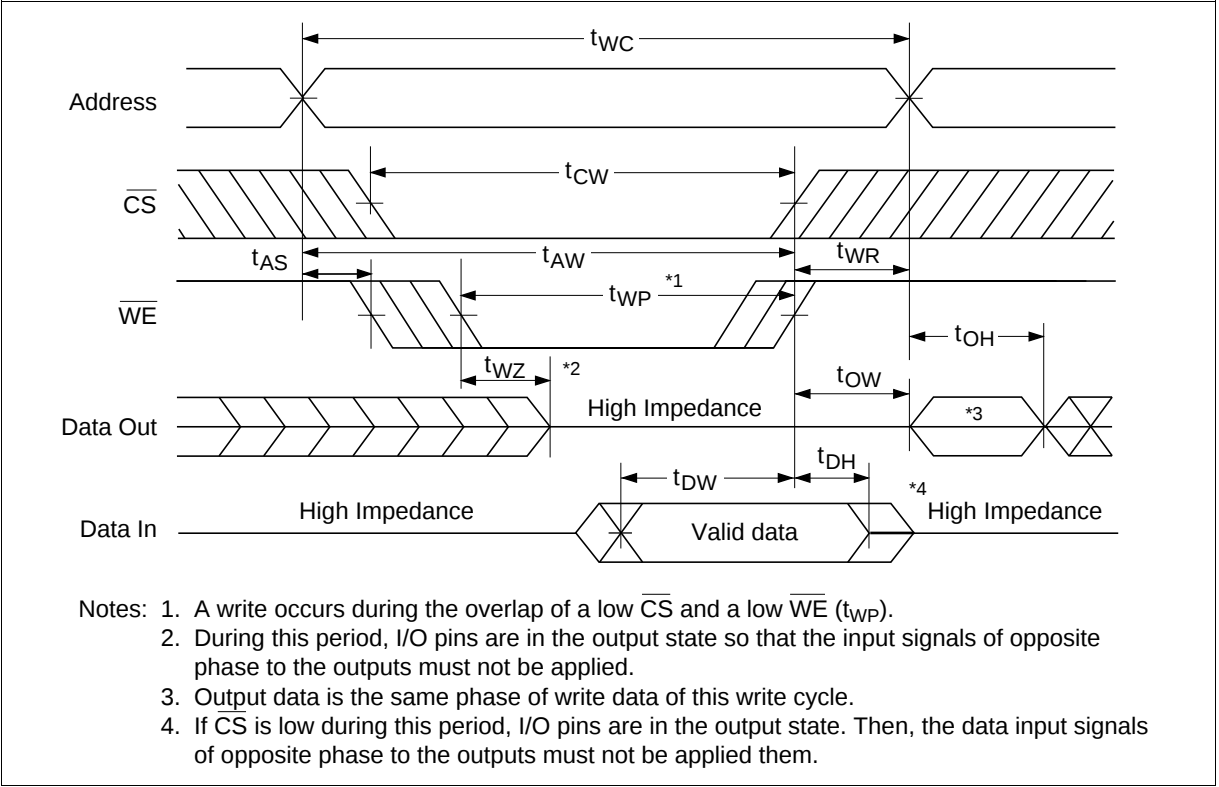


Write Cycle-4 ($\overline{\text{OE}}$ = Clocked, $\overline{\text{CS}}$ Controlled)

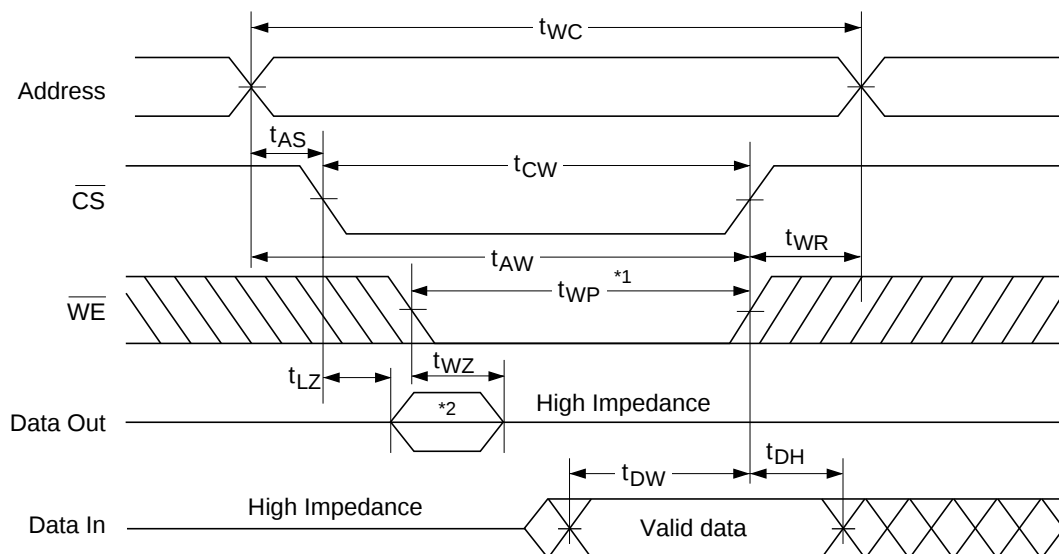


- Notes:
1. A write occurs during the overlap of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$ (t_{WP}).
 2. If $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{OE}}$ high transition or after the $\overline{\text{OE}}$ transition, output remain in a high impedance state.

Write Cycle-5 ($\overline{OE} = L$, $\overline{WE}$ Controlled)



Write Cycle-6 ($\overline{OE} = L$, $\overline{CS}$ Controlled)

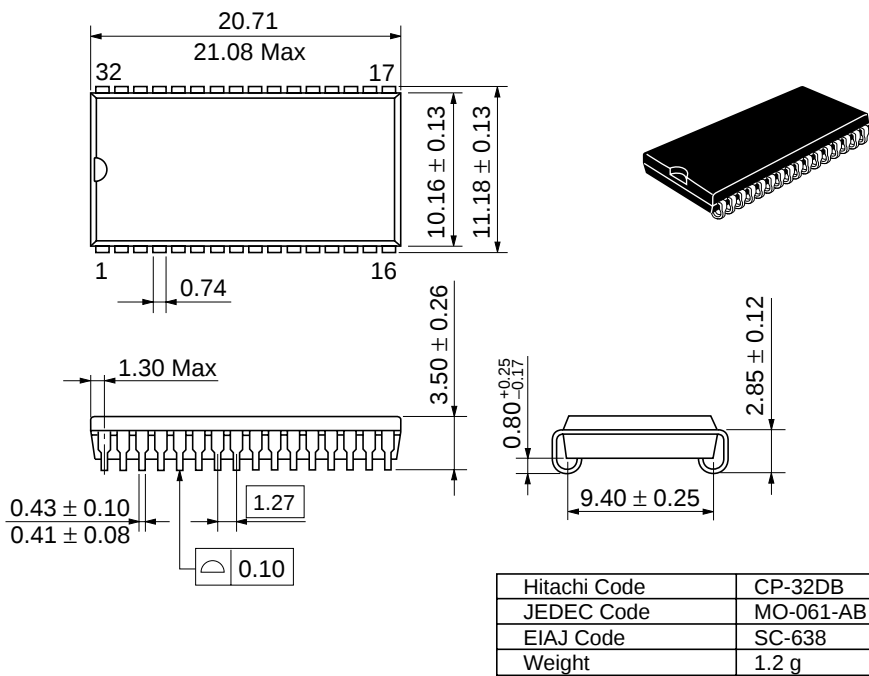


- Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
 2. If $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

Package Dimension

HM674100HJP Series (CP-32DB)

Unit: mm



HM674100HJP -15, -20, -25 400 mil 32 pin plastic SOJ (CP-32DB) — Mechanical