

MOSFET – Power, Single, P-Channel, SOT-223

-60 V, -2.6 A

NTF2955, NVF2955

Features

- Design for low $R_{DS(on)}$
- Withstands High Energy in Avalanche and Commutation Modes
- AEC-Q101 Qualified – NVF2955
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Power Supplies
- PWM Motor Control
- Converters
- Power Management

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	-60	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	-2.6	A
		$T_A = 85^{\circ}\text{C}$		-2.0	
Power Dissipation (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	P_D	2.3	W
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	-1.7	A
		$T_A = 85^{\circ}\text{C}$		-1.3	
Power Dissipation (Note 2)		$T_A = 25^{\circ}\text{C}$	P_D	1.0	W
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$		I_{DM}	-17	A
Operating Junction and Storage Temperature			T_J , T_{STG}	-55 to 175	$^{\circ}\text{C}$
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 25\ \text{V}$, $V_G = 10\ \text{V}$, $I_{PK} = 6.7\ \text{A}$, $L = 10\ \text{mH}$, $R_G = 25\ \Omega$)			EAS	225	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			T_L	260	$^{\circ}\text{C}$

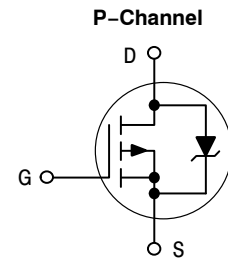
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Tab (Drain) – Steady State (Note 2)	$R_{\theta JC}$	14	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	65	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	150	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1 in. pad size (Cu. area = 1.127 in² [1 oz] including traces)
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu. area = 0.341 in²)

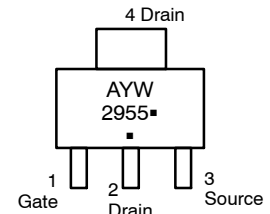
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
-60 V	145 m Ω @ -10 V	-2.6 A



MARKING DIAGRAM AND PIN ASSIGNMENT



SOT-223
CASE 318E
STYLE 3



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTF2955T1G	SOT-223 (Pb-Free)	1000 /Tape & Reel
NVF2955T1G	SOT-223 (Pb-Free)	1000/ Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTF2955, NVF2955

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-60	-	-	V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$		-	66.4	-	mV/°C	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -60\text{ V}$	$T_J = 25^\circ\text{C}$	-	-	-1.0	μA
			$T_J = 125^\circ\text{C}$	-	-	-50	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA	

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -1.0 mA	-2.0	-	-4.0	V
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -0.75 A	-	145	170	mΩ
		V _{GS} = -10 V, I _D = -1.5 A	-	150	180	
		V _{GS} = -10 V, I _D = -2.4 A	-	154	185	
Forward Transconductance	g _{FS}	V _{GS} = -15 V, I _D = -0.75 A	-	1.77		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V	-	492	-	pF
Output Capacitance	C _{OSS}		-	165	-	
Reverse Transfer Capacitance	C _{RSS}		-	50	-	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 30 V, I _D = 1.5 A	-	14.3	-	nC
Threshold Gate Charge	Q _{G(TH)}		-	1.2	-	
Gate-to-Source Charge	Q _{GS}		-	2.3	-	
Gate-to-Drain Charge	Q _{GD}		-	5.2	-	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DD} = 25 V, I _D = 1.5 A, R _G = 9.1 Ω R _L = 25 Ω	-	11	-	ns
Rise Time	t _r		-	7.6	-	
Turn-Off Delay Time	t _{d(OFF)}		-	65	-	
Fall Time	t _f		-	38	-	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 1.5 A	T _J = 25°C	–	–1.10	–1.30	V
			T _J = 125°C	–	–0.9	–	
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 1.5 A	–	36	–	ns	
Charge Time	t _a		–	20	–		
Discharge Time	t _b		–	16	–		
Reverse Recovery Charge	Q _{RR}		–	0.139	–	nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

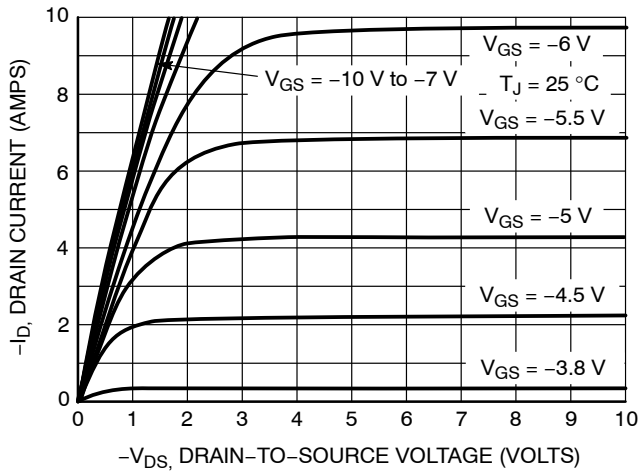


Figure 1. On-Region Characteristics

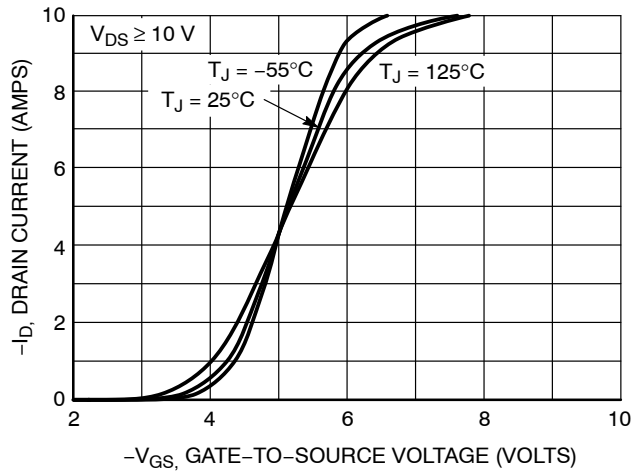


Figure 2. Transfer Characteristics

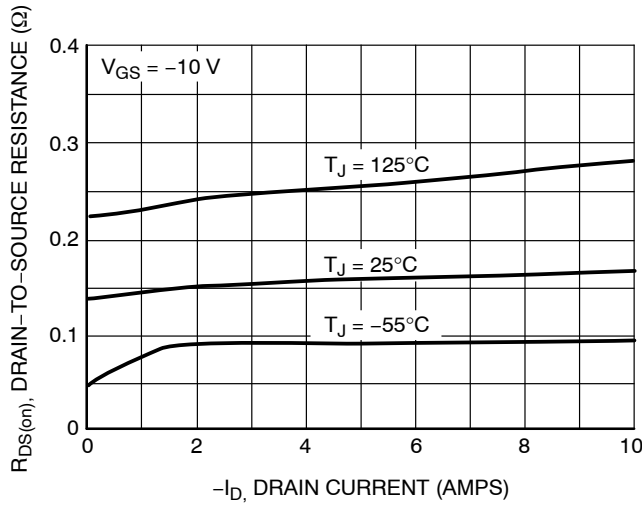


Figure 3. On-Resistance versus Drain Current and Temperature

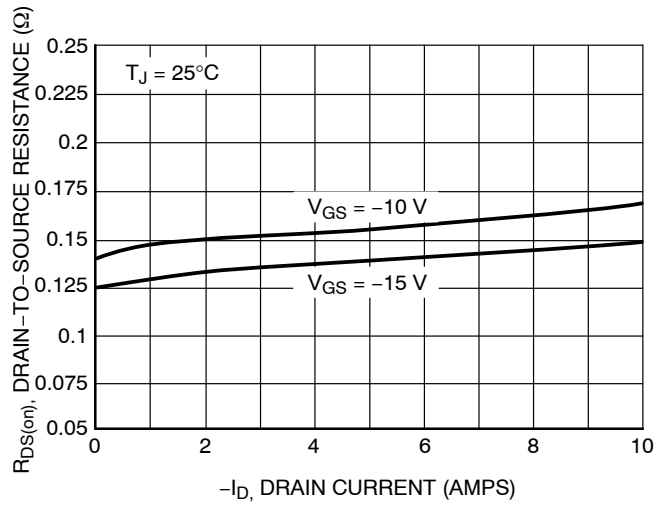


Figure 4. On-Resistance versus Drain Current and Gate Voltage

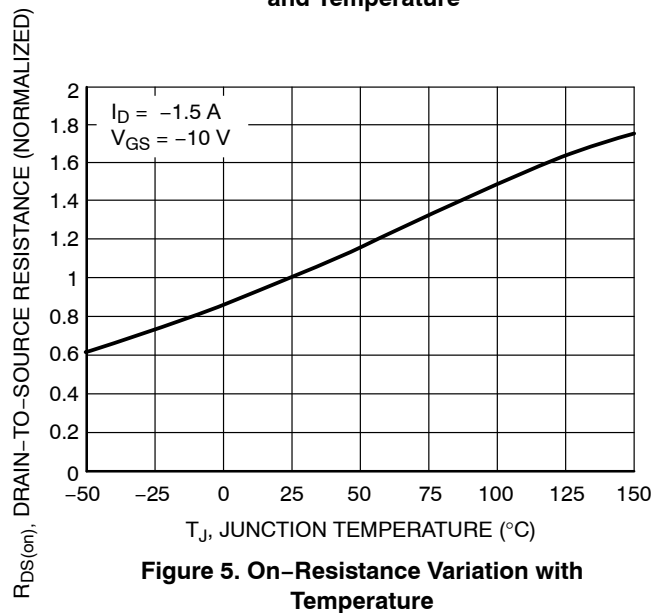


Figure 5. On-Resistance Variation with Temperature

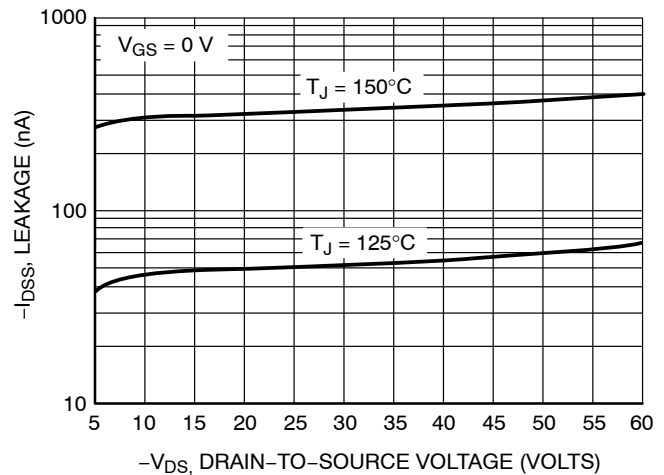
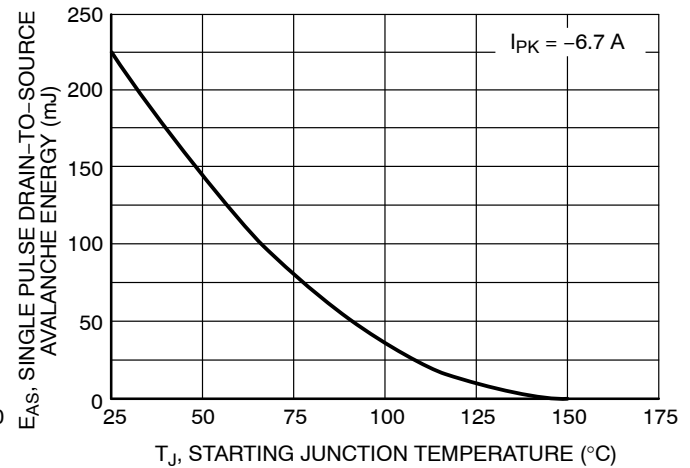
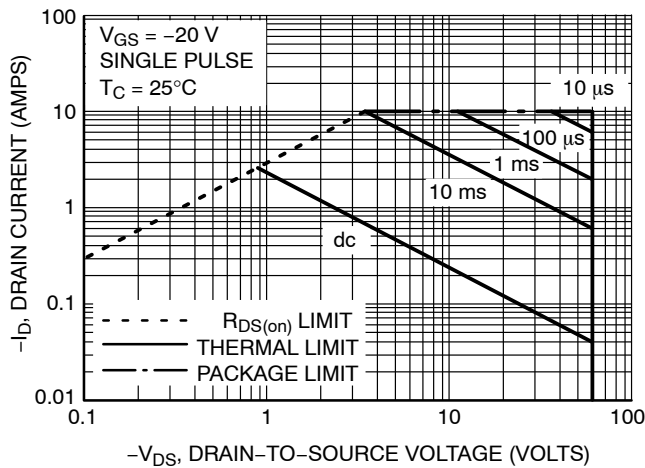
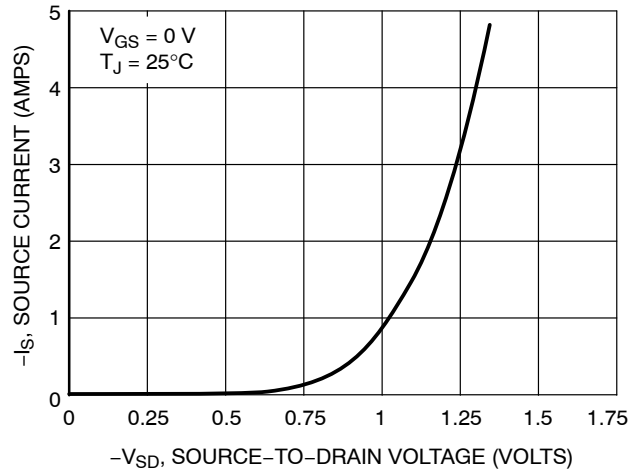
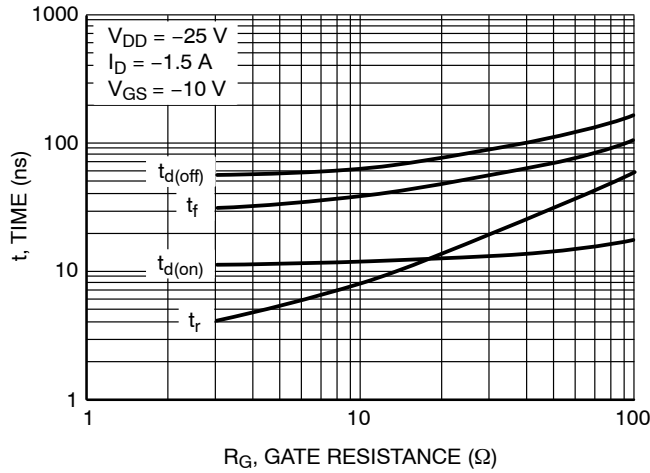
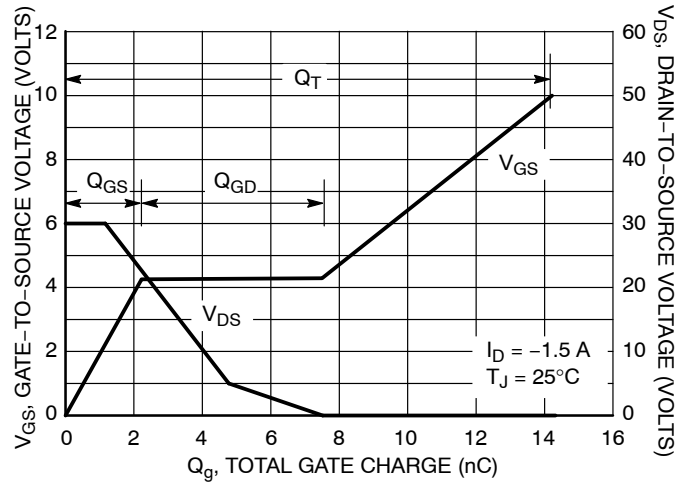
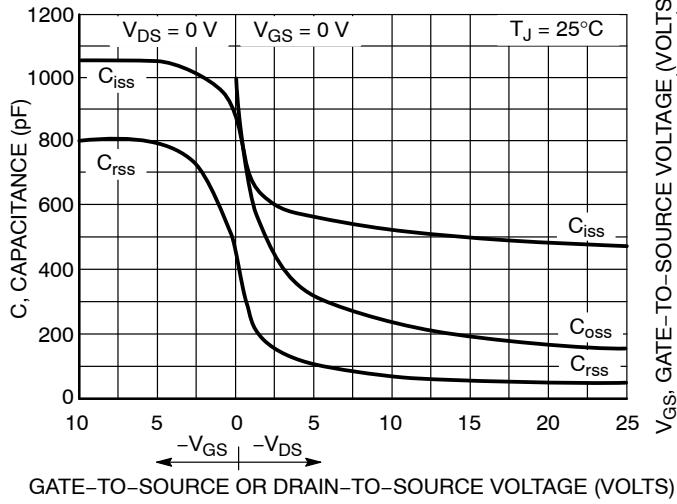


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



NTF2955, NVF2955

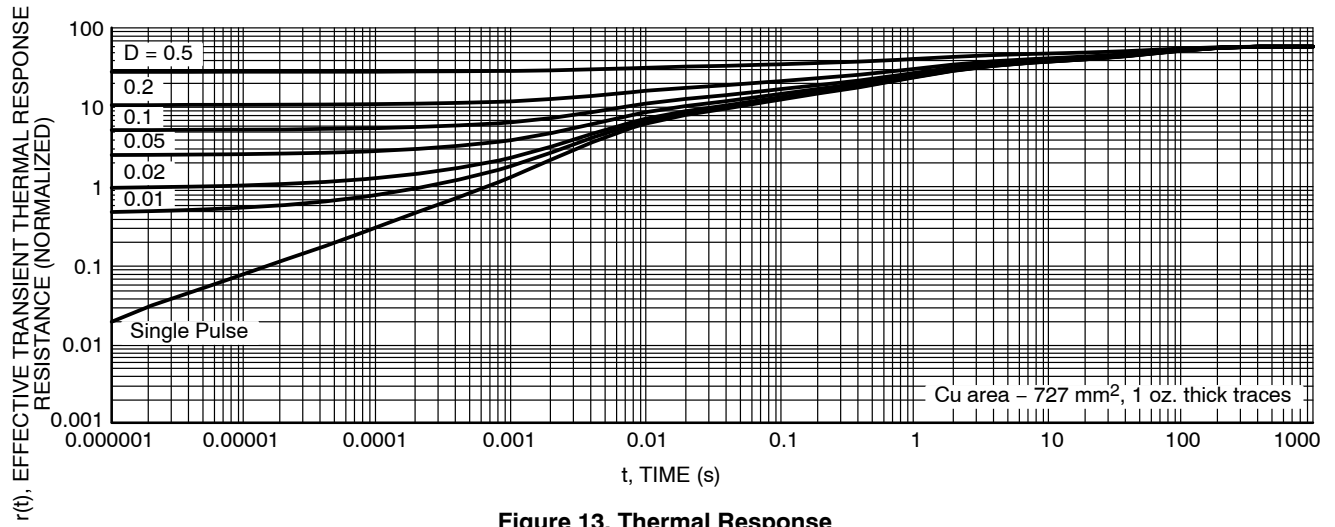


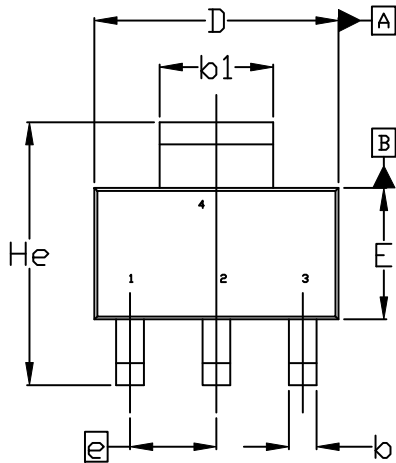
Figure 13. Thermal Response



SCALE 1:1

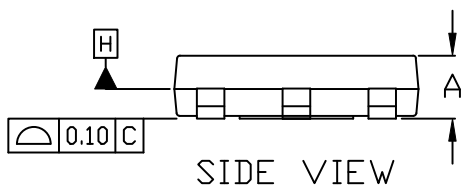
SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

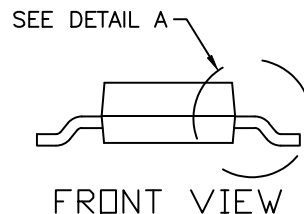


TOP VIEW

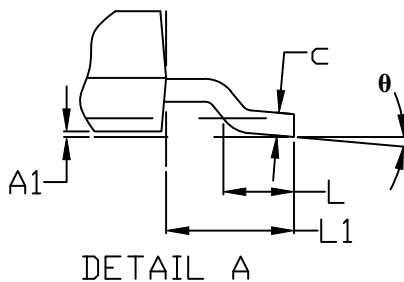
$\oplus 0.10 \text{ (M)} \text{ C A B}$
NOTE 5



SIDE VIEW



FRONT VIEW

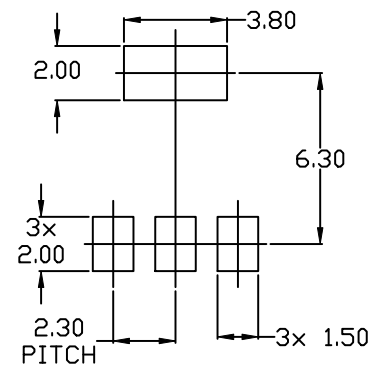


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING
FOOTPRINT

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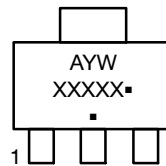
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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***



A = Assembly Location
 Y = Year
 W = Work Week
 XXXXX = Specific Device Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)
 *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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