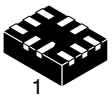
NLAS6234

Audio DPDT Switch with Noise Suppression

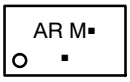
ON Semiconductor®

http://onsemi.com



UQFN10
MU SUFFIX
CASE 488AT

MARKING DIAGRAM



AR = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

Description

The NLAS6234 is a DPDT switch featuring Popless noise suppression circuitry designed to prevent pass through of undesirable transient signals known as pops. Intended for audio systems within portable applications, it provides protection against audible pops that are generated when switching between two different audio sources, such as an amplifier and a CODEC.

The NLAS6234 incorporates two double throw switches controlled by a single select line which allows the system controller to simultaneously switch between two sets of signal lines. The Popless noise suppression circuitry controls the ON and OFF times that define the time interval when switching between the normally open (NO) and normally closed (NC) terminals. This allows any pops to be dissipated within the system before the switch settles into a closed position.

The NLAS6234 operates off of a single supply voltage, V_{CC}, and is available in an ultra−thin UQFN10 package.

Features

- Popless Noise Suppression Circuitry
- OVT up to +4.5 V on Control Pin
- R_{ON} < 0.5 Ω Across BCC Range, Typical
- THD < 0.02 %, Typical
- Off Isolation = −70 dB, Typical
- Crosstalk Attenuation < −70 dB, Typical
- Ultra Small, Thin Package: 1.4 mm x 1.8 mm UQFN10
- This is a Pb−Free Device

Typical Applications

- Cell Phones, PDAs, MP3 and Other Portable Media Players

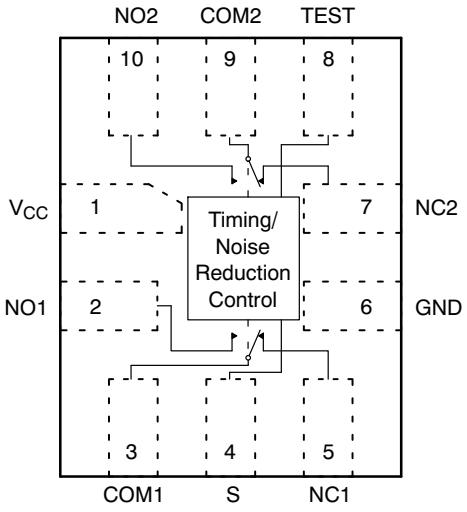


Figure 1. Pin Connections and Logic Diagram (Top View)

NOTE: Pin 8 is for ATE use only, not intended for end customer use.

PIN ASSIGNMENT

PIN	FUNCTION
V_{CC}	Supply Voltage
GND	Ground
S	Control Input Select Line
TEST	ATE Test Pin
NC1, NO1, NC2, NO2	Independent Channels
COM1, COM2	Common Channels

TRUTH TABLE

S	NC1, NC2	NO1, NO2
0	ON	OFF
1	OFF	ON

MAXIMUM RATINGS

Symbol	Pins	Rating	Value	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	−0.5 to +5.5	V
V_{IS}	NOx, NCx, COMx	Analog Signal Voltage	−0.5 to V_{CC} + 0.5	V
V_{IN}	S	Control Input Voltage	−0.5 to +5.5	V
I_{IS_CON}	NOx, NCx, COMx	Analog Signal Continuous Current−Closed Switch	±300	mA
I_{IS_PK}	NOx, NCx, COMx	Analog Signal Continuous Current 10% Duty Cycle	±500	mA
I_{IN}	S	Control Input Current	±20	mA
T_s	T_s	Storage Temperature	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pins	Parameter	Min	Max	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	2.7	4.5	V
V_{IS}	NOx, NCx, COMx	Analog Signal Voltage	GND	V_{CC}	V
V_{IN}	S	Control Input Voltage (OVT Protection)	GND	4.5	V
T_A		Operating Temperature Range	−40	+85	°C
t_r, t_f		Input Rise or Fall Time, S V_{CC} = 3.0 V to 3.6 V	0	10	ns/V

DC ELECTRICAL CHARACTERISTICS

CONTROL INPUT (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
V_{IH}	S	Minimum High−Level Input Voltage, Select Input		2.7 4.2	1.4 2.0	−	−	V
V_{IL}	S	Maximum Low−Level Input Voltage, Select Input		2.7 4.2	−	−	0.7 0.8	V
I_{IN}	S	Control Input Leakage Current	V_{IS} = GND	2.7−4.5	−	±100	±1000	nA

SUPPLY CURRENT AND LEAKAGE (Typical: T = 25°C, V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
I_{CC}	V_{CC}	Quiescent Supply Current	V_{IS} = V_{CC} or GND; I_D = 0 A	2.7 − 4.5	−	<100	1000	nA
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NCx, NOx	OFF State Leakage Current	V_{COM} = 4.5 V V_{NO}, V_{NC} = 1.0 V	2.7 − 4.5	−	±10	±1000	nA
I_{OFF}		Power OFF Leakage Current	V_{IS} = GND	0	−	±10	±1000	nA

ON RESISTANCE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
R_{ON}		On−Resistance	V_{IN} = V_{IL} or V_{IN} = V_{IH} V_{IS} = 0 to V_{CC}; I_{IS} = 100 mA	2.7 4.2	−	0.40 0.35	0.60 0.55	Ω
R_{FLAT}		On−Resistance Flatness	V_{IS} = 0 to V_{CC}; I_{IS} = 100 mA	2.7 4.2	−	0.14 0.15	0.19 0.20	Ω
ΔR_{ON}		On−Resistance Match Between Channels	V_{IS} = 0 to V_{CC}; I_{IS} = 100 mA	2.7 4.2	−	0.15 0.15	0.20 0.20	Ω

AC ELECTRICAL CHARACTERISTICS

TIMING/FREQUENCY (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 35 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	−40°C to +85°C			Unit
					Min	Typ	Max	
t_{ON}	−	Turn−ON Time (Figures 2, 3, 12)		2.7−4.5		11		ns
t_{OFF}	−	Turn−OFF Time (Figures 2, 3, 13)		2.7−4.5		9.0		ns
t_{BBM}	−	Minimum Break Before Make Time (Figure 14)	V_{IS} = 3.0, typ @ V_{CC} = 3.6 V	3.4−4.2		60		ms
BW	−	−3 dB Bandwidth	V_{IS} = 0 dB	2.7−4.5		36		MHz

ISOLATION (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	−40°C to +85°C			Unit
					Min	Typ	Max	
O_{IRR}	NOx	OFF−Isolation	V_{IS} = 1.0 V_{RMS}, f = 100 kHz	2.7−4.5		−70		dB
XTALK	COM 1 to COM 2	Crosstalk	V_{IS} = 1.0 V_{RMS}, f = 100 kHz	2.7−4.5		−98		dB
THD	−	Total Harmonic Distortion	R_L = 600 Ω, V_{COMn} = 2.0 V_{p-p}	3.0		0.02		%

CAPACITANCE (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V_{CC} (V)	−40°C to +85°C			Unit
					Min	Typ	Max	
C_{IN}	S	Select Input Capacitance		0		2.5		pF
C_{OFF}	NOx	OFF−Capacitance	V_{IS} = 3.3 V, S = 0 V	2.7−4.5		72		pF
C_{ON}	COMx to NCx	ON−Capacitance	S = 0 V	2.7−4.5		113		pF

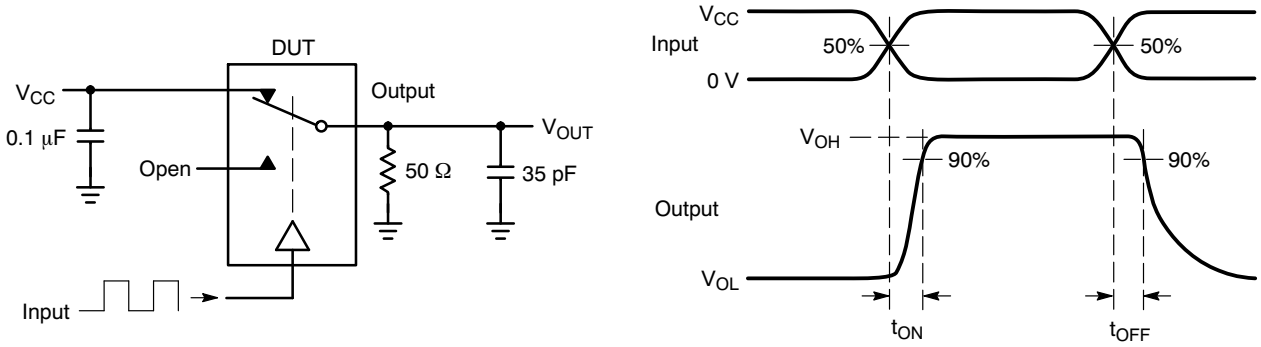


Figure 2. t_{ON} / t_{OFF}, V_{is} = V_{CC}

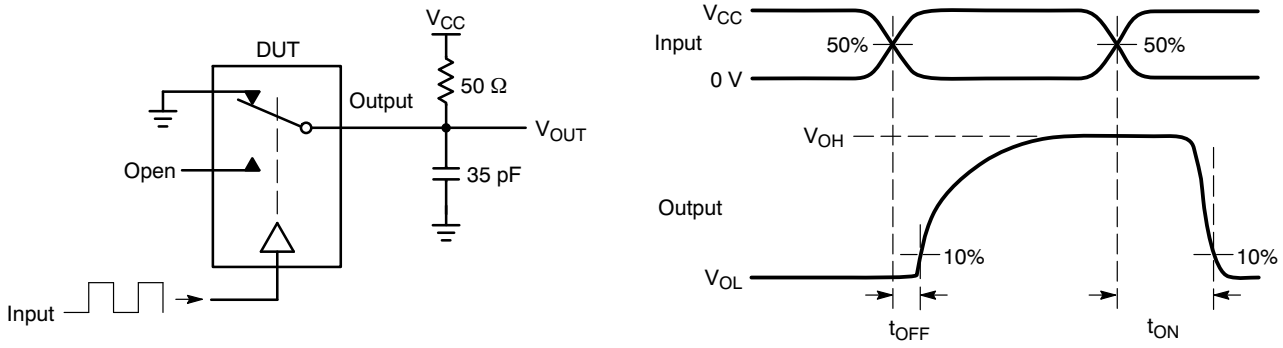
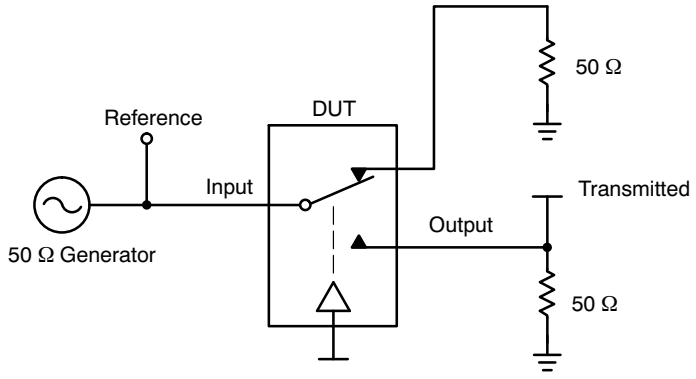


Figure 3. t_{ON} / t_{OFF}, V_{is} = GND



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log } \left(\frac{V_{OUT}}{V_{IN}}\right) \text{for } V_{IN} \text{ at 100 kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log } \left(\frac{V_{OUT}}{V_{IN}}\right) \text{for } V_{IN} \text{ at 100 kHz to 50 MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 4. Off−Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

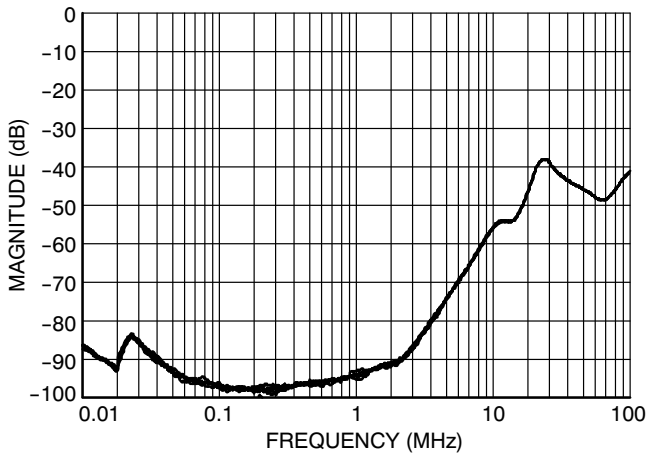


Figure 5. Crosstalk vs. Frequency @ 25°C

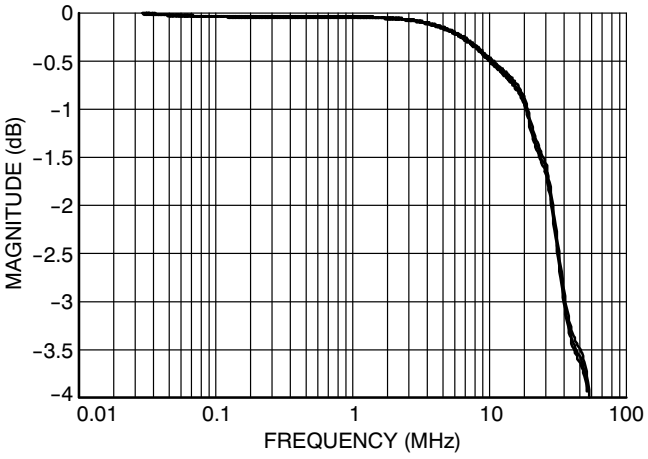


Figure 6. Bandwidth vs. Frequency @ V_{CC} = 3 V

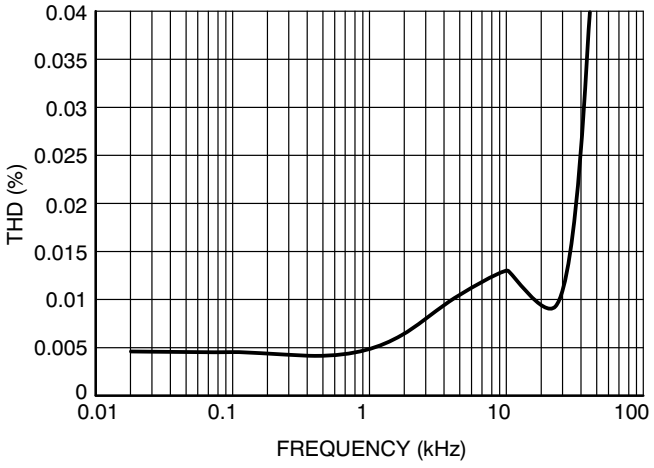


Figure 7. Total Harmonic Distortion @ V_{CC} = 3.0 V

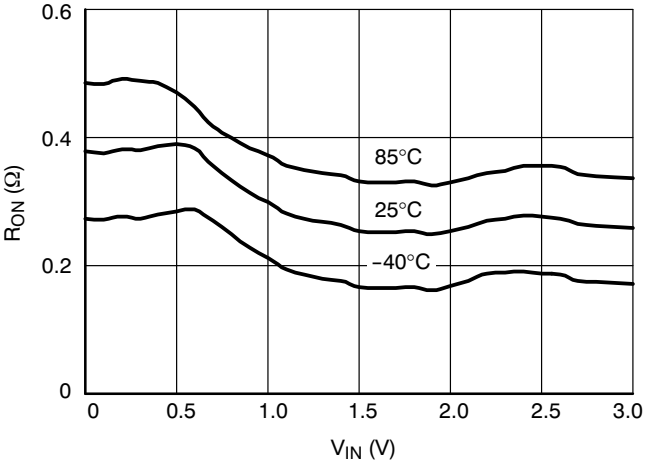


Figure 8. On−Resistance vs. Input Voltage @ V_{CC} = 3.0 V

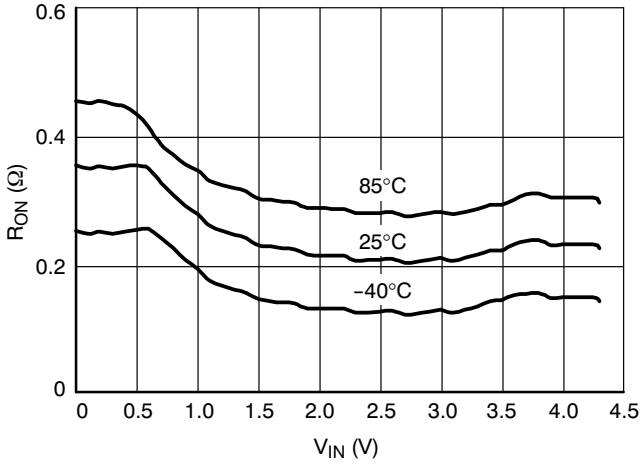


Figure 9. On−Resistance vs. Input Voltage @ V_{CC} = 4.3 V

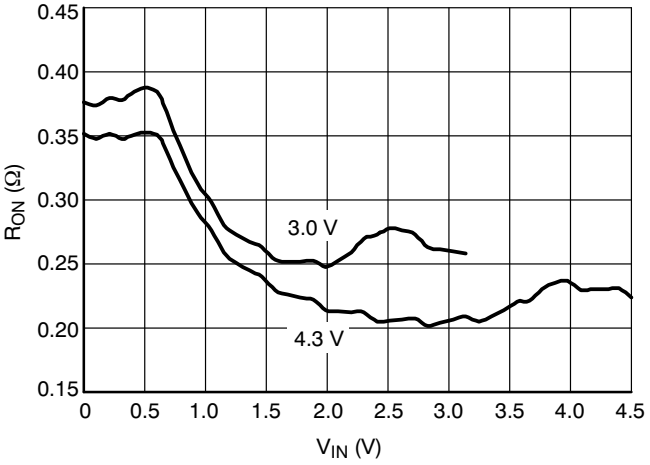


Figure 10. On−Resistance vs. Input Voltage @ 25°C

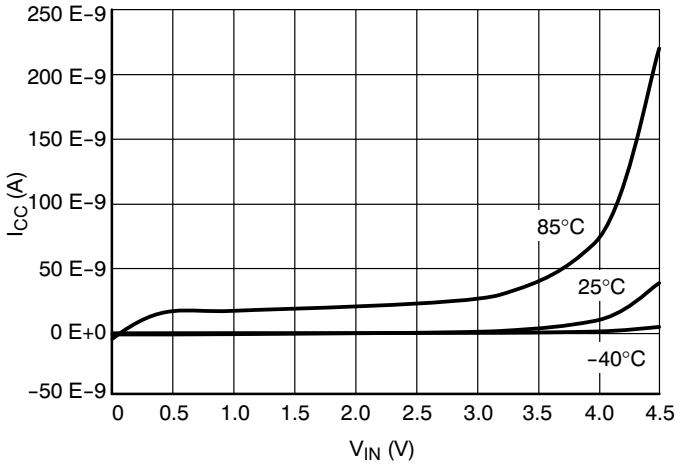


Figure 11. I_{CC} vs V_{CC}

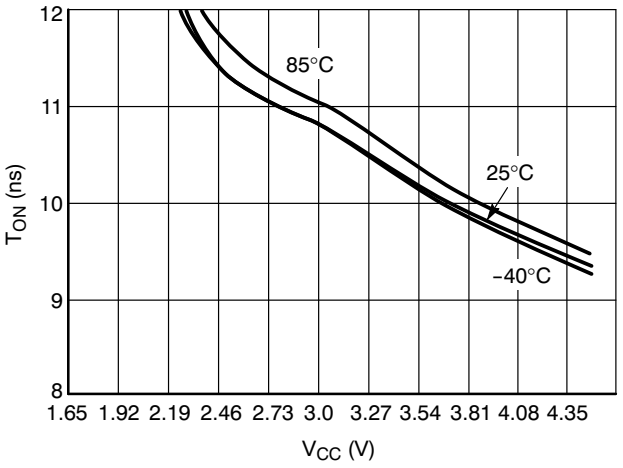


Figure 12. t_{ON} vs V_{CC}

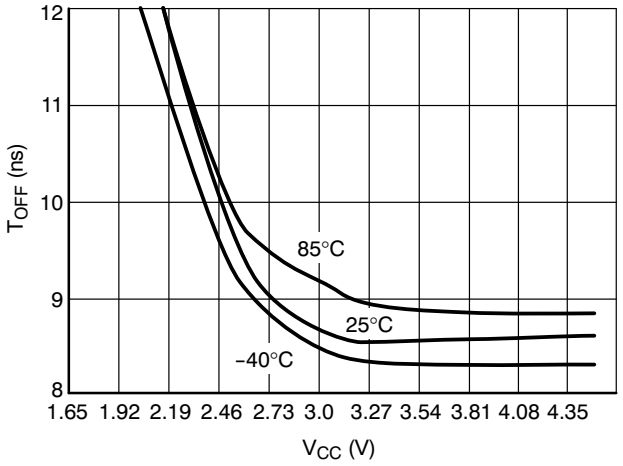


Figure 13. t_{OFF} vs V_{CC}

Popless Implementation on the NLAS6234

Audio sources such as amplifiers or CODECs can generate undesirable, transient voltage spikes when powering up and down. Those voltage spikes can be translated into current surges and ultimately lead to audible pop noises in the speaker if not diverted or suppressed. The NLAS6234 includes popless noise suppression circuitry designed to prevent such undesirable pops from propagating through to the speaker. This feature is realized through a deliberate increase in the Break−Before−Make time, t_{BBM}, and is useful in applications where a switch is used to alternate between two different audio sources.

When the signal from the common pin is removed from one terminal, the switch waits an extended amount of time before connecting to the opposite terminal. The time interval for t_{BBM} is a function of the supply voltage of the switch, V_{CC}. Figure 14 shows the relationship of t_{BBM} for each V_{CC} value within the recommended operating voltage range.

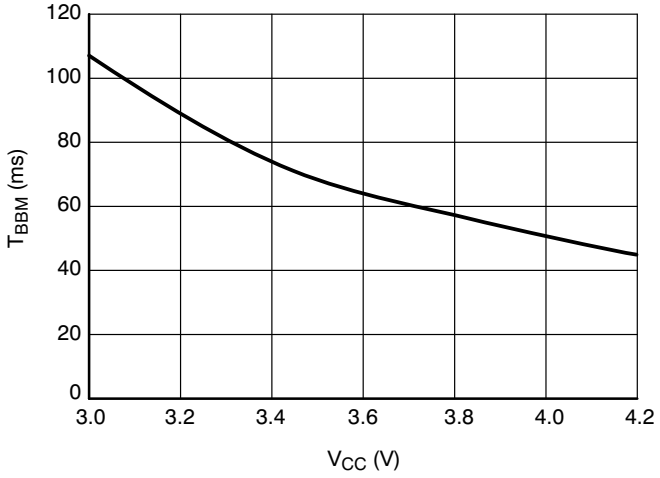


Figure 14. NLAS6234 T_{BBM} vs. V_{CC}

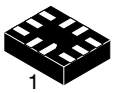
DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NLAS6234MUTBG	UQFN10 (Pb−Free)	3000/Tape & Reel

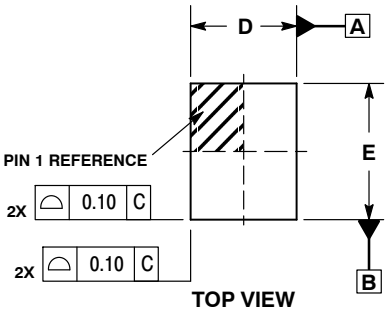
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

UQFN10 1.4x1.8, 0.4P
CASE 488AT
ISSUE A

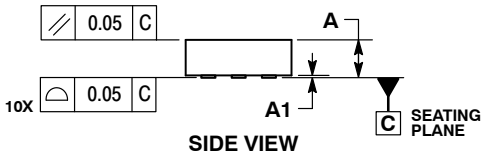
DATE 01 AUG 2007



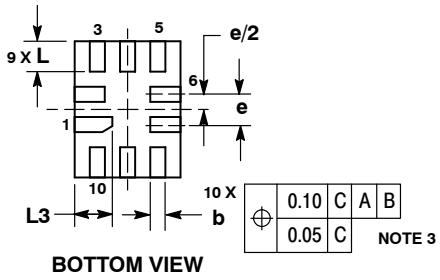
SCALE 5:1



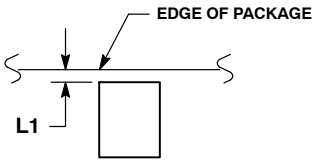
TOP VIEW



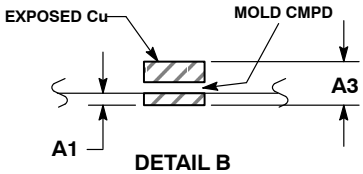
SIDE VIEW



BOTTOM VIEW



DETAIL A
Bottom View
(Optional)

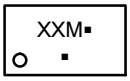


DETAIL B
Side View
(Optional)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L3	0.40	0.60

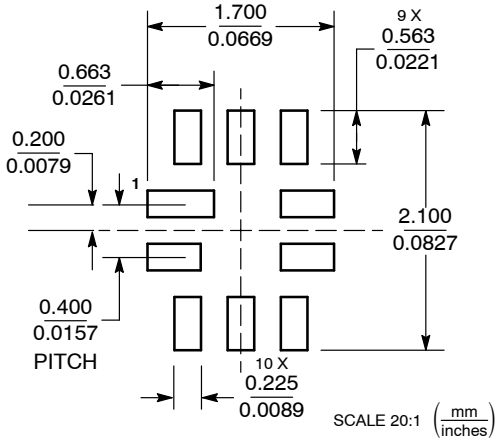
GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

MOUNTING FOOTPRINT



SCALE 20:1 (mm / inches)

DOCUMENT NUMBER:	**98AON22493D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**10 PIN UQFN, 1.4 X 1.8, 0.4P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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