

MMJT9435

Preferred Device

Bipolar Power Transistors

PNP Silicon

Features

- Pb-Free Packages are Available
- Collector -Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 30 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain –
 $h_{FE} = 125 \text{ (Min) @ } I_C = 0.8 \text{ Adc}$
 $= 90 \text{ (Min) @ } I_C = 3.0 \text{ Adc}$
- Low Collector -Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.275 \text{ Vdc (Max) @ } I_C = 1.2 \text{ Adc}$
 $= 0.55 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- SOT-223 Surface Mount Packaging
- Epoxy Meets UL 94, V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B; > 8000 V
Machine Model, C; > 400 V



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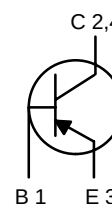
<http://onsemi.com>

POWER BJT

$I_C = 3.0 \text{ AMPERES}$

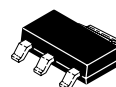
$BV_{CEO} = 30 \text{ VOLTS}$

$V_{CE(sat)} = 0.275 \text{ VOLTS}$

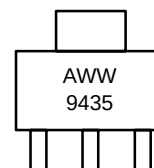


Schematic

MARKING DIAGRAM

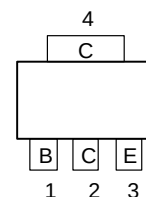


**SOT-223
CASE 318E
STYLE 1**



9435 = Specific Device Code
A = Assembly Location
WW = Work Week

PIN ASSIGNMENT



Top View Pinout

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

MMJT9435

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CEO}	30	Vdc
Collector–Base Voltage	V _{CB}	45	Vdc
Emitter–Base Voltage	V _{EB}	6.0	Vdc
Base Current – Continuous	I _B	1.0	Adc
Collector Current – Continuous – Peak	I _C	3.0 5.0	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C Total P _D @ T _A = 25°C mounted on 1" sq. (645 sq. mm) Collector pad on FR-4 bd material Total P _D @ T _A = 25°C mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 bd material	P _D	3.0 24 1.56 0.72	W mW/°C W
Operating and Storage Junction Temperature Range	T _J , T _{stg}	–55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to–Case – Junction-to–Ambient on 1" sq. (645 sq. mm) Collector pad on FR-4 bd material – Junction-to–Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 bd material	R _{θJC} R _{θJA} R _{θJA}	42 80 174	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	260	°C

ORDERING INFORMATION

Device	Package	Shipping†
MMJT9435T1	SOT-223	1000 / Tape & Reel
MMJT9435T1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
MMJT9435T3	SOT-223	4000 / Tape & Reel
MMJT9435T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MMJT9435

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 10 \text{ mAdc}$, $I_B = 0 \text{ Adc}$)	$V_{CEO(sus)}$	30	–	–	Vdc
Emitter-Base Voltage ($I_E = 50 \mu\text{Adc}$, $I_C = 0 \text{ Adc}$)	V_{EBO}	6.0	–	–	Vdc
Collector Cutoff Current ($V_{CE} = 25 \text{ Vdc}$, $R_{BE} = 200 \Omega$) ($V_{CE} = 25 \text{ Vdc}$, $R_{BE} = 200 \Omega$, $T_J = 125^\circ\text{C}$)	I_{CER}	– –	– –	20 200	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$)	I_{EBO}	–	–	10	μAdc

ON CHARACTERISTICS (Note 1)

Collector-Emitter Saturation Voltage ($I_C = 0.8 \text{ Adc}$, $I_B = 20 \text{ mAdc}$) ($I_C = 1.2 \text{ Adc}$, $I_B = 20 \text{ mAdc}$) ($I_C = 3.0 \text{ Adc}$, $I_B = 0.3 \text{ Adc}$)	$V_{CE(sat)}$	– – –	0.155 – –	0.210 0.275 0.550	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0 \text{ Adc}$, $I_B = 0.3 \text{ Adc}$)	$V_{BE(sat)}$	–	–	1.25	Vdc
Base-Emitter On Voltage ($I_C = 1.2 \text{ Adc}$, $V_{CE} = 4.0 \text{ Vdc}$)	$V_{BE(on)}$	–	–	1.10	Vdc
DC Current Gain ($I_C = 0.8 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 1.2 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 3.0 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$)	h_{FE}	125 110 90	220 – –	– – –	–

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0 \text{ Adc}$, $f = 1.0 \text{ MHz}$)	C_{ob}	–	100	150	pF
Input Capacitance ($V_{EB} = 8.0 \text{ Vdc}$)	C_{ib}	–	135	–	pF
Current-Gain – Bandwidth Product (Note 2) ($I_C = 500 \text{ mA}$, $V_{CE} = 10 \text{ V}$, $f_{test} = 1.0 \text{ MHz}$)	f_T	–	110	–	MHz

1. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
2. $f_T = |h_{FE}| \cdot f_{test}$

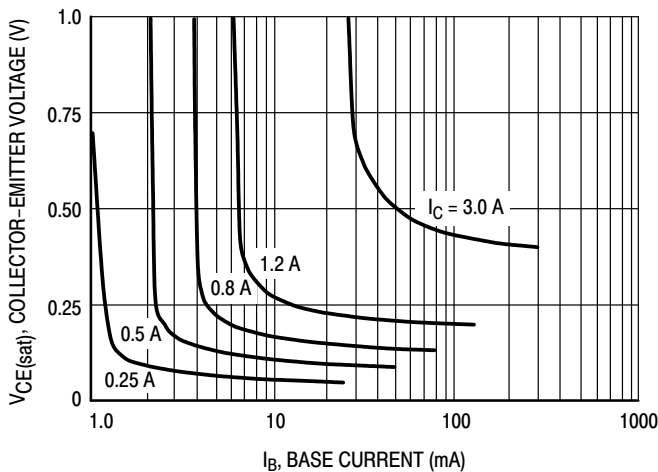


Figure 1. Collector Saturation Region

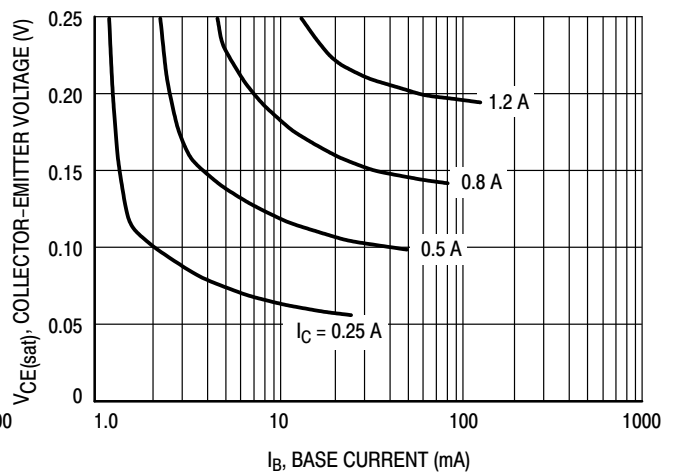


Figure 2. Collector Saturation Region

MMJT9435

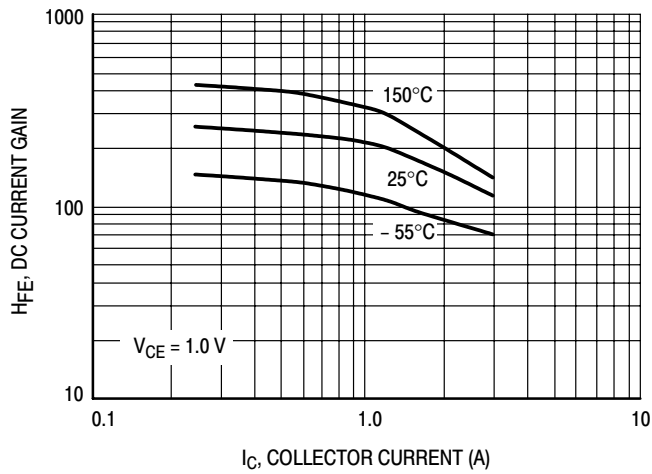


Figure 3. DC Current Gain

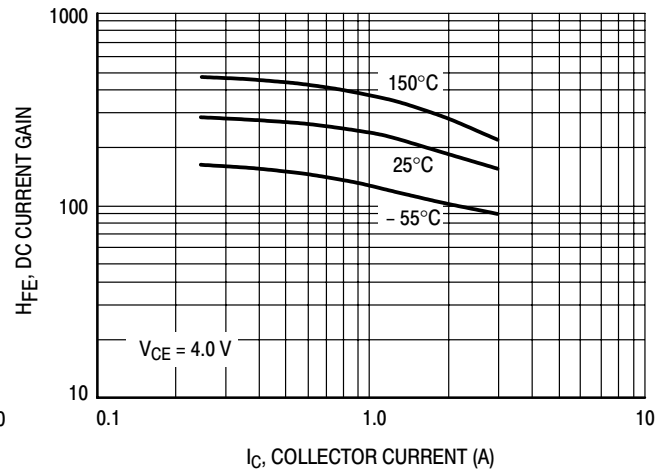


Figure 4. DC Current Gain

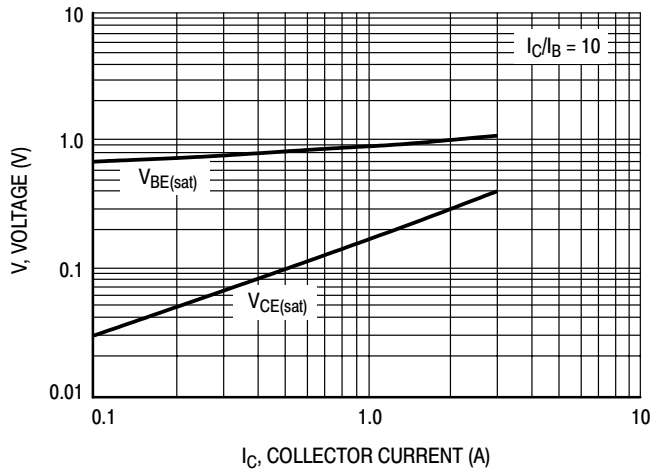


Figure 5. "On" Voltages

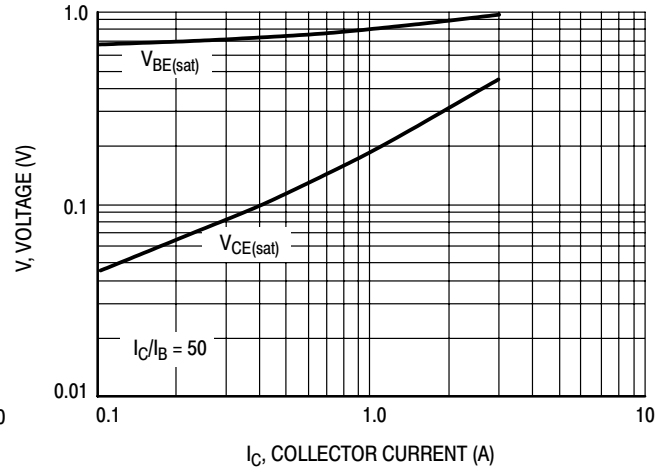


Figure 6. "On" Voltages

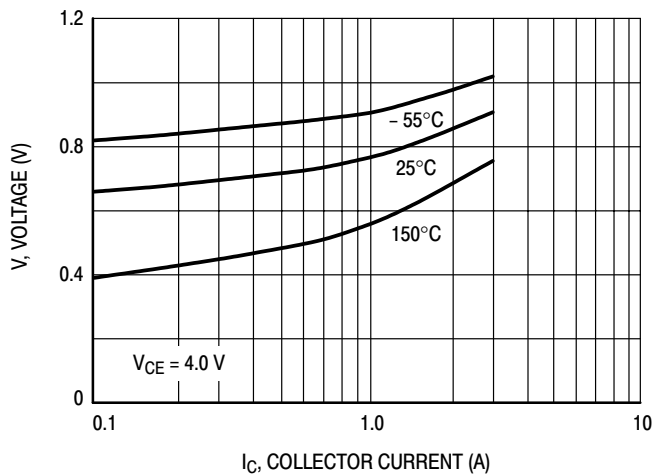


Figure 7. $V_{BE(on)}$ Voltage

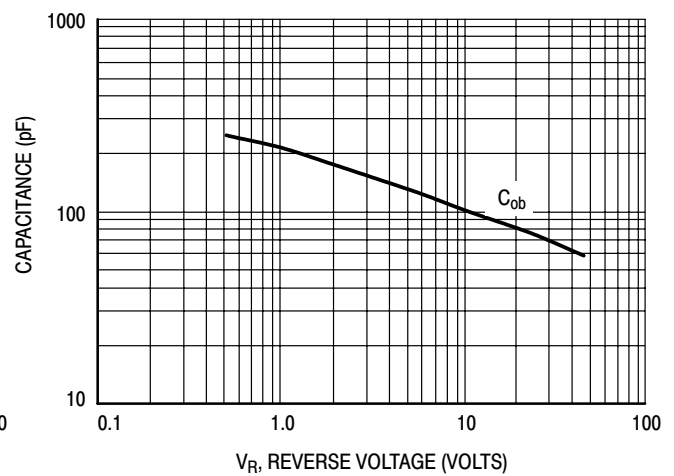


Figure 8. Output Capacitance

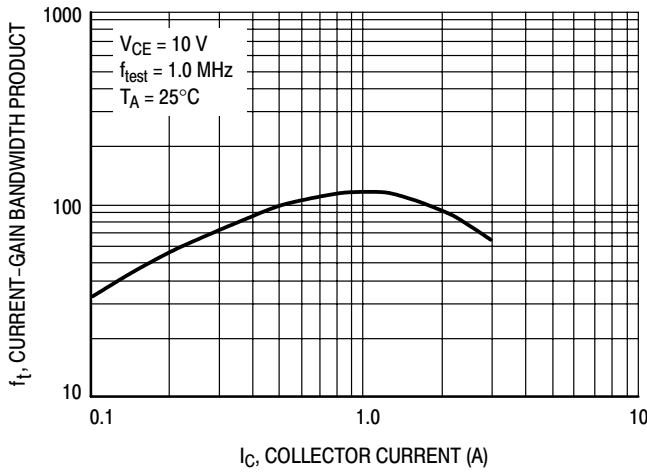


Figure 9. Current-Gain Bandwidth Product

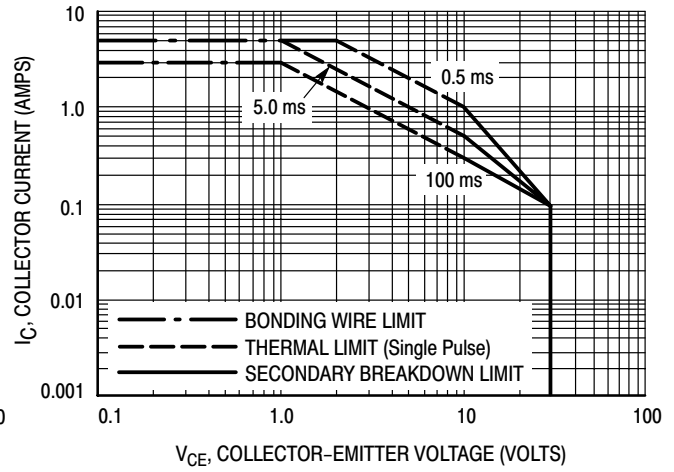


Figure 10. Active Region Safe Operating Area

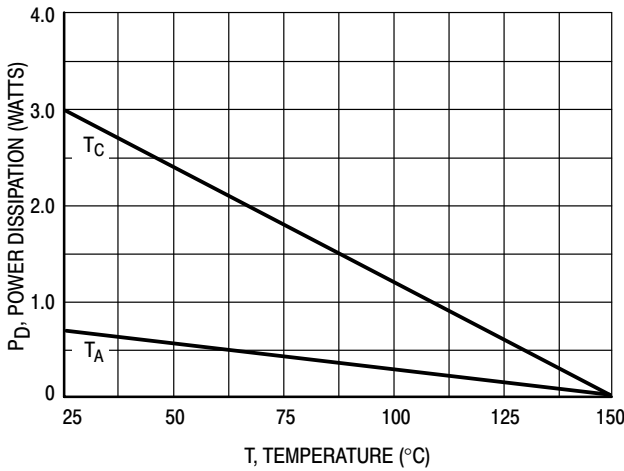


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

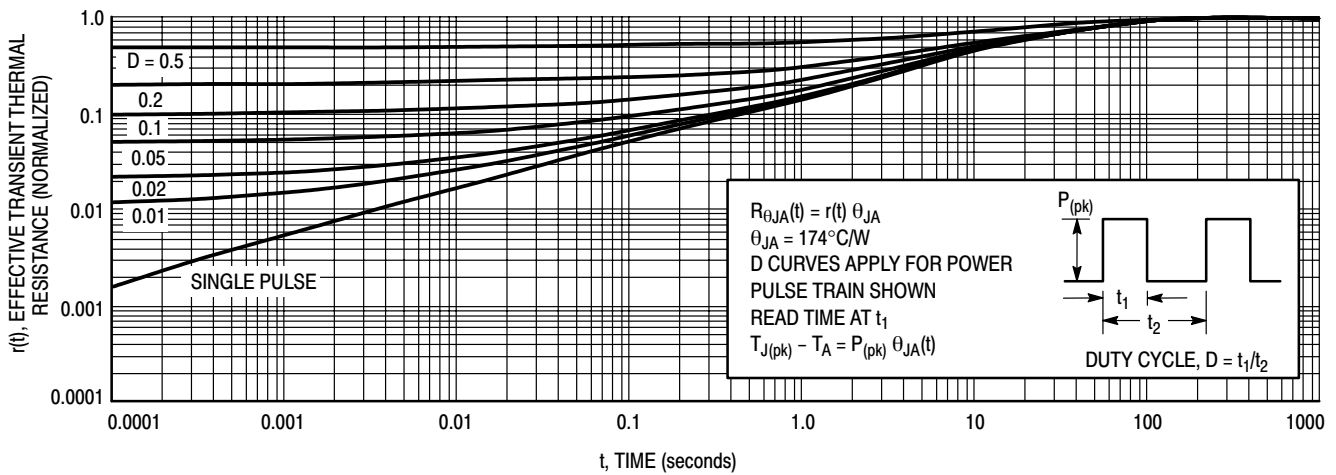


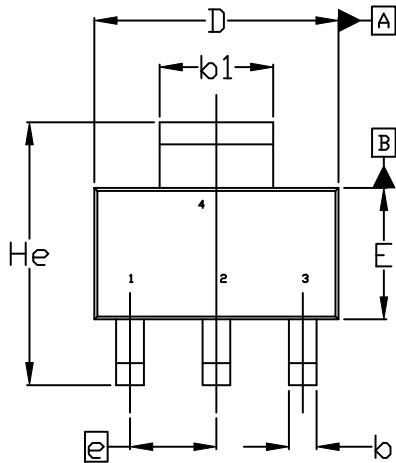
Figure 12. Thermal Response



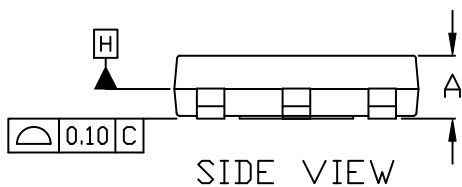
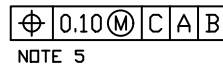
SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

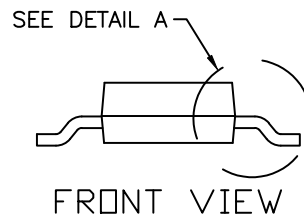
DATE 02 OCT 2018



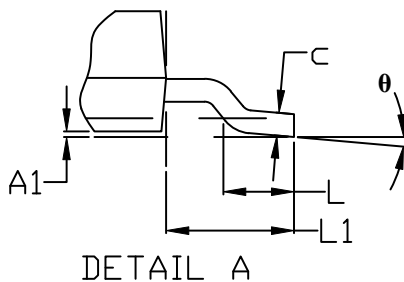
TOP VIEW



SIDE VIEW



FRONT VIEW

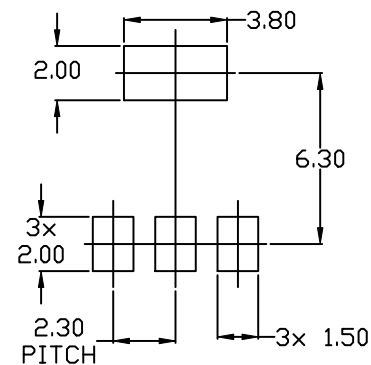


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°


RECOMMENDED MOUNTING
FOOTPRINT

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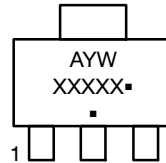
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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***



A = Assembly Location
 Y = Year
 W = Work Week
 XXXXX = Specific Device Code
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)
 *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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