Chapter 1. Introduction

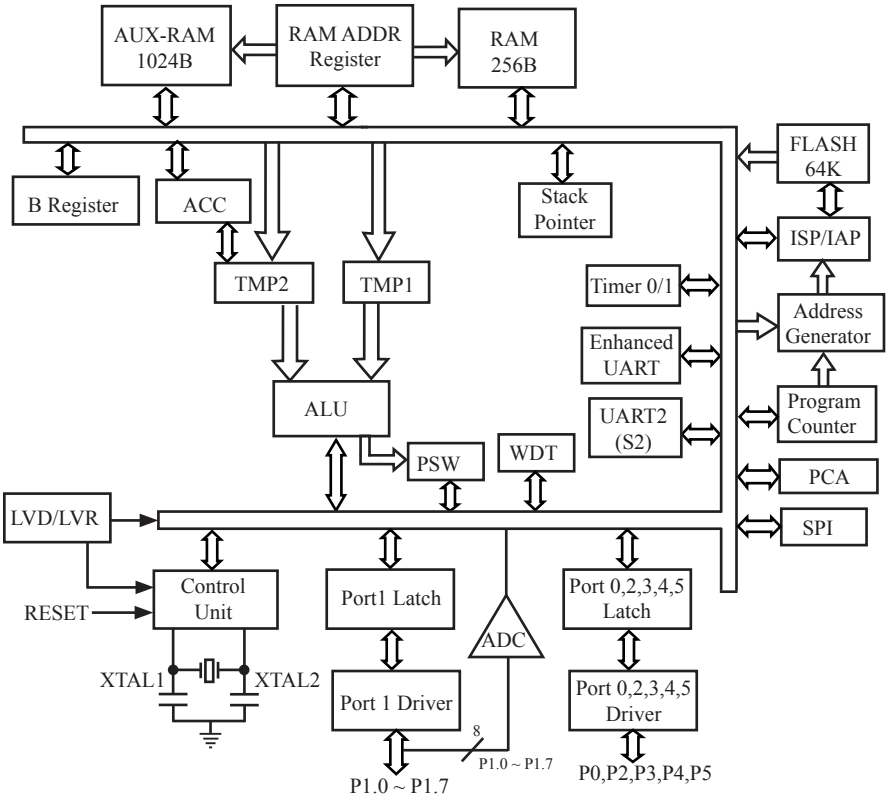
STC12C5A60S2 is a single-chip microcontroller based on a high performance 1T architecture 80C51 CPU, which is produced by STC MCU Limited. With the enhanced kernel, STC12C5A60S2 executes instructions in 1~6 clock cycles (about 6~7 times the rate of a standard 8051 device), and has a fully compatible instruction set with industrial-standard 80C51 series microcontroller. In-System-Programming (ISP) and In-Application-Programming (IAP) support the users to upgrade the program and data in system. ISP allows the user to download new code without removing the microcontroller from the actual end product; IAP means that the device can write non-valatile data in Flash memory while the application program is running. The STC12C5A60S2 retains all features of the standard 80C51. In addition, the STC12C5A60S2 has two extra I/O ports (P4 and P5), a 10-sources, 4-priority-level interrupt structure, 10-bit ADC, two UARTs, on-chip crystal oscillator, a 2-channel PCA and PWM, SPI, a one-time enabled Watchdog Timer.

1.1 Features

- Enhanced 80C51 Central Processing Unit ,1T per machine cycle, faster 6~7 times than the rate of a standard 8051.
- Operating voltage range: 5.5V ~ 3.5V or 2.2V ~ 3.6V (STC12LE5A60S2).
- Operating frequency range: 0- 35MHz, is equivalent to standard 8051:0~420MHz
- On-chip 8/16/20/32/40/48/52/56/60/62K FLASH program memory with flexible ISP/IAP capability
- On-chip 1280 byte RAM: 256 byte scratch-pad RAM and 1024 bytes of auxiliary RAM
- Be capable of addressing up to 64K byte of external RAM
- Dual Data Pointer (DPTR) to speed up data movement
- Code protection for flash memory access
- Excellent noise immunity, very low power consumption
- four 16-bit timer/counter, be compatible with Timer0/Timer1 of standard 8051, 2-channel PCA can be available as two timers.
- 10 vector-address, 4 level priority interrupt capability
- One enhanced UART with hardware address-recognition and frame-error detection function
- Secondary UART with self baud-rate generator
- One 15 bits Watch-Dog-Timer with 8-bit pre-scaler (one-time-enabled)
- SPI Master/Slave communication interface
- Two channel Programmable Counter Array (PCA)
- 10-bit, 8-channel Analog-to-Digital Converter (ADC)
- Simple internal RC oscillator and external crystal clock
- Power control: idle mode(all interrupt can wake up IDLE mode) , power-down mode(external interrupt can wake up Power-Down mode) and slow down mode
- Power down mode can be woken-up by PCA_pin, RXD_pin, T0/T1 pin and external interrupts (INT0, INT1)
- 44/40/36 programmable I/O ports are available
- Programmable clock output Function. T0 output the clock on P3.4,T1 output the clock on P3.5,BRT output the clock on P1.0
- External low-voltage detector function(P4.6, the EA pin at the pin location of standard 8051)
- Five package type : LQFP-44, LQFP-48 ,PDIP-40, PLCC-44,QFN-40

1.2 Block diagram

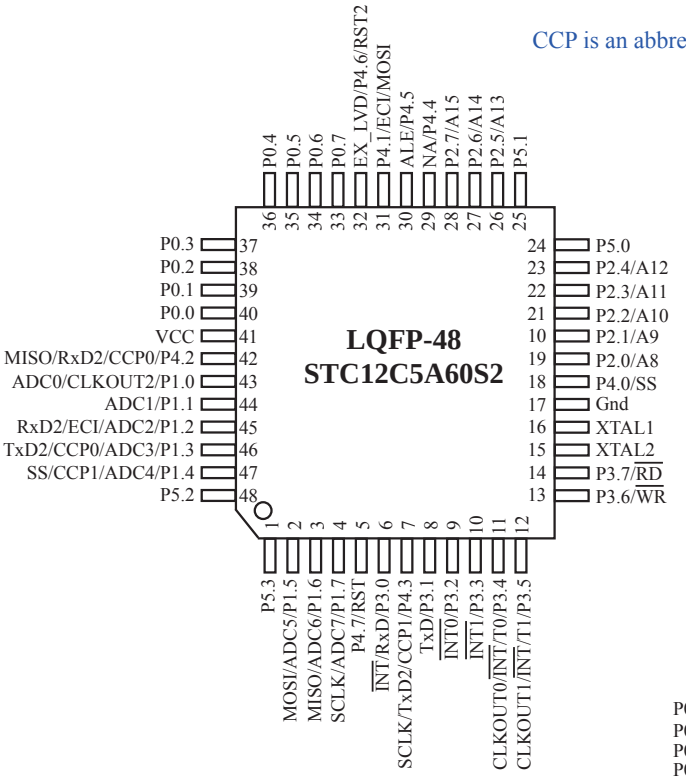
The CPU kernel of STC12C5A60S2 is fully compatible to the standard 8051 microcontroller, maintains all instruction mnemonics and binary compatibility. With some great architecture enhancements, STC12C5A60S2 executes the fastest instructions per clock cycle. Improvement of individual programs depends on the actual instructions used.

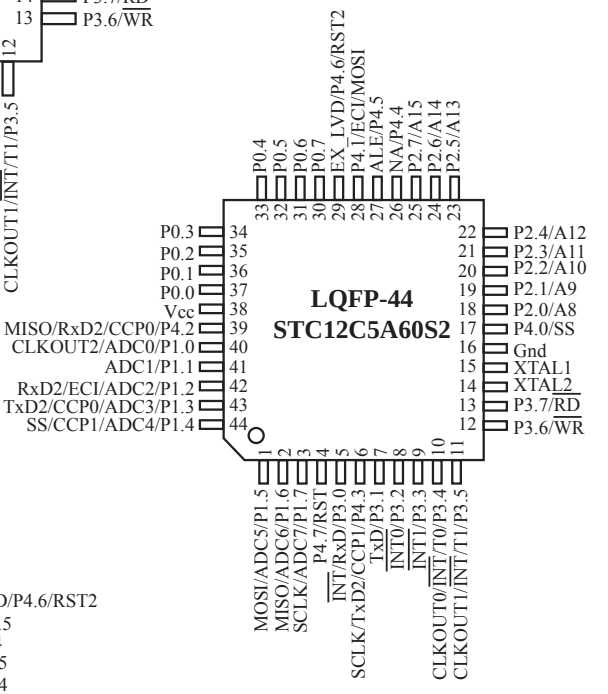


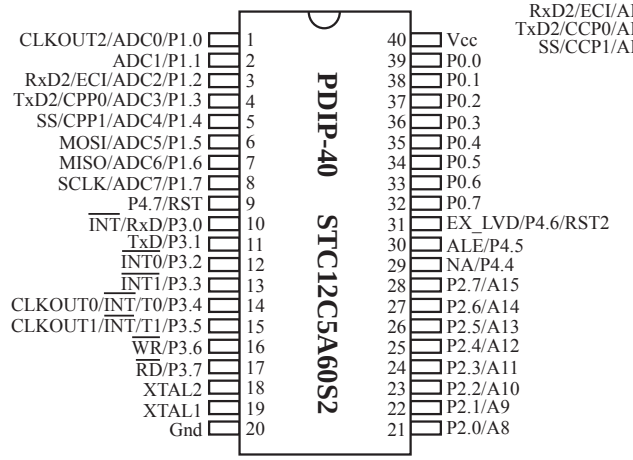
STC12C5A60S2 Block Diagram

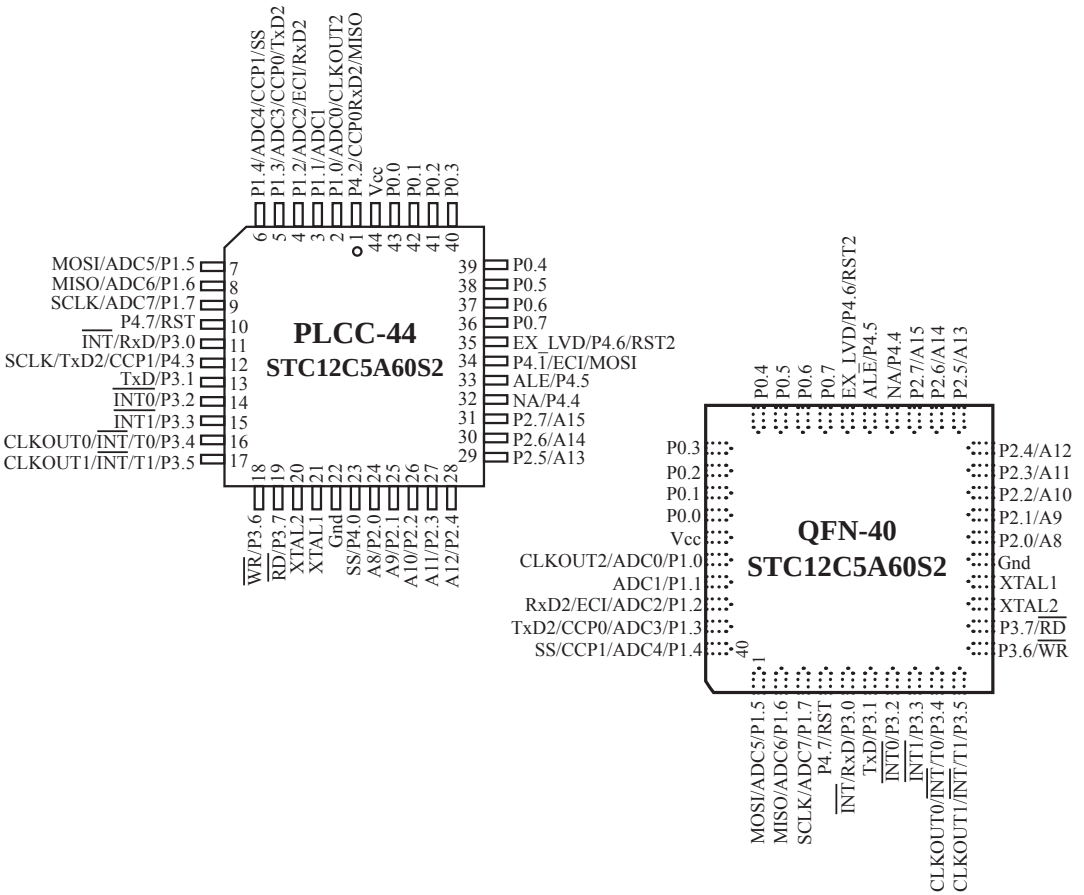
1.3 Pin Configurations

CCP is an abbreviation of Capture, Compare and PWM









Register P4SW is used to set the secondary function of NA/P4.4, ALE/P4.5 and EX_LVD/P4.6

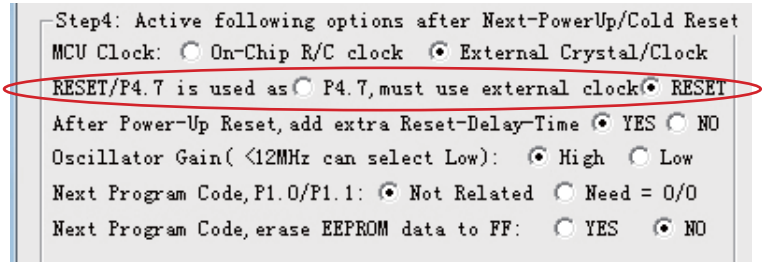
Mnemonic	Add	Name	7	6	5	4	3	2	1	0	Reset Value
P4SW	BBH	Port-4 switch		LVD_P4.6	ALE_P4.5	NA_P4.4					x000,xxxx

NA/P4.4: 0, P4SW.4=0 when MCU is reset. NA/P4.4 is weak pull-up and no any function.
1, when P4SW.4 is set to 1, NA/P4.4 is as an I/O port (P4.4)

ALE/P4.5: 0, P4SW.5=0 when MCU is reset. ALE/P4.5 is as ALE signal which is used to access external data memory .
1, when P4SW.5 is set to 1, ALE/P4.4 is used as an I/O port (P4.5)

LVD/P4.6: 0, P4SW.6=0 when MCU is reset. EX_LVD/P4.6 is as External Low-Voltage Detection function
1, when P4SW.6 is set to 1, EX_LVD/P4.6 is used as an I/O port (P4.6)

In STC-ISP writter/programmer, users can select what RST/P4.7 is used as. the pin RST/P4.7 is as reset function acquiescently, see the following figure.



Register AUXR1 is used to select whether PCA/PWM/SPI/UART2 function is on P1 port or P4 port

Mnemonic	Add	Name	7	6	5	4	3	2	1	0	Reset Value
AUXR1	A2H	Auxiliary register 1	-	PCA_P4	SPI_P4	S2_P4	GF2	ADRJ	-	DPS	x000,00x0

PCA _P4
- 0 : Default. The PCA function is on P1[4:2]
- 1 : The PCA function on P1[4:2] is switched to P4[3:1].
  ECI is switched from P1.2 to P4.1
  PCA0/PWM0 is switched from P1.3 to P4.2
  PCA1/PWM1 is switched from P1.4 to P4.3

SPI_P4
- 0 : Default. The SPI function is on P1[7:4]
- 1 : The SPI function on P1[7:4] is switched to P4[3:0].
  SCLK is switched from P1.7 to P4.3
  MOSI is switched from P1.6 to P4.2
  MISO is switched from P1.5 to P4.1
  SS is switched from P1.4 to P4.0

S2_P4
- 0 : Default. the UART2(S2) function is on P1[3:2]
- 1 : The UART2(S2) function on P1[3:2] is switched to P4[3:2].
  TxD2 is switched from P1.3 to P4.3
  RxD2 is switched from P1.2 to P4.2

GF2 : General Flag. It can be used by software.

ADRJ
- 0 : The 10-bit conversion result of ADC is arranged as {ADC_RES[7:0], ADC_RESL[1:0]}.
- 1 : The 10-bit conversion result is right-justified, {ADC_RES[1:0], ADC_RESL[7:0]}.

DPS
- 0 : Default. DPTR0 is selected as Data pointer.
- 1 : The secondary DPTR is switched to use.

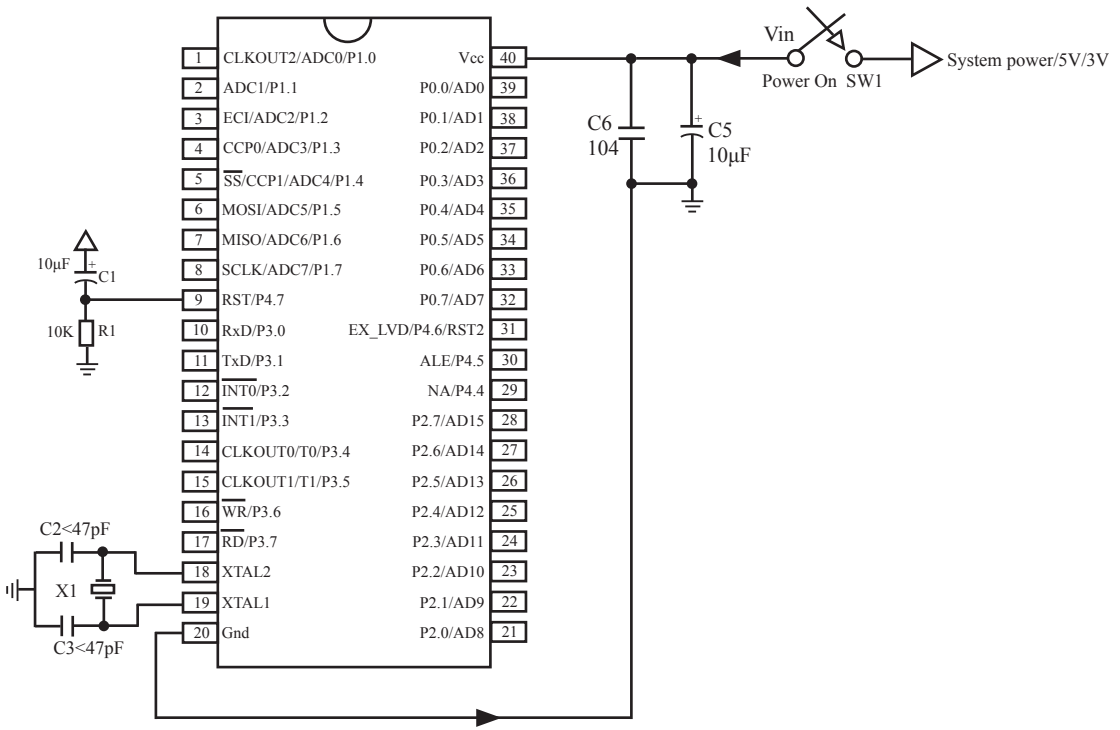
1.4 STC12C5A60S2 series Selection Table

Type 1T 8051 MCU	Operating Voltage (V)	Flash (Byte)	SRAM (B)	TIMER	UART	DPTR	EEPROM (B)	16-bit PCA/ 8-bit PWM D/A	A/D	WDT	External real-time low voltage interrupt	External Reset threshold voltage can be configured	External interrupts which can wake up power down mode	Package of 40-pin (36 I/O ports)	Package of 44-pin (40 I/O ports)	Package of 48-pin (44 I/O ports)
STC12C5A60S2 series Selection Table																
STC12C5A08S2	5.5~3.5	8K	1280	4	2-3	2	53K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A16S2	5.5~3.5	16K	1280	4	2-3	2	45K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A32S2	5.5~3.5	32K	1280	4	2-3	2	29K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A40S2	5.5~3.5	40K	1280	4	2-3	2	21K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A48S2	5.5~3.5	48K	1280	4	2-3	2	13K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A52S2	5.5~3.5	52K	1280	4	2-3	2	9K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A56S2	5.5~3.5	56K	1280	4	2-3	2	5K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A60S2	5.5~3.5	60K	1280	4	2-3	2	1K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
IAP12C5A62S2	5.5~3.5	62K	1280	4	2-3	2	IAP	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A60S2 series Selection Table																
STC12LE5A08S2	3.6~2.1	8K	1280	4	2-3	2	53K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A16S2	3.6~2.1	16K	1280	4	2-3	2	45K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A32S2	3.6~2.1	32K	1280	4	2-3	2	29K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A40S2	3.6~2.1	40K	1280	4	2-3	2	21K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A48S2	3.6~2.1	48K	1280	4	2-3	2	13K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A52S2	3.6~2.1	52K	1280	4	2-3	2	9K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A56S2	3.6~2.1	56K	1280	4	2-3	2	5K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A60S2	3.6~2.1	60K	1280	4	2-3	2	1K	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
IAP12LE5A62S2	3.6~2.1	62K	1280	4	2-3	2	IAP	2	10	Y	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48

Type 1T 8051 MCU	Operating voltage (V)	Flash (Byte)	SRAM (B)	TIMER	UART	DPTR	16-bit PCA/ 8-bit PWM D/A	A/D	WDT	EEPROM (B)	External real-time low voltage interrupt	External Reset threshold voltage can be configured	External interrupts which can wake up power down mode	Package of 40-pin (36 I/O ports)	Package of 44-pin (40 I/O ports)	Package of 48-pin (44 I/O ports)
STC12C5A60AD series Selection Table																
STC12C5A08AD	5.5~3.5	8K	1280	4	1	2	2	10	Y	53K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A16AD	5.5~3.5	16K	1280	4	1	2	2	10	Y	45K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A32AD	5.5~3.5	32K	1280	4	1	2	2	10	Y	29K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A40AD	5.5~3.5	40K	1280	4	1	2	2	10	Y	21K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A48AD	5.5~3.5	48K	1280	4	1	2	2	10	Y	13K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A52AD	5.5~3.5	52K	1280	4	1	2	2	10	Y	9K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A56AD	5.5~3.5	56K	1280	4	1	2	2	10	Y	5K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12C5A60AD	5.5~3.5	60K	1280	4	1	2	2	10	Y	1K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
IAP12C5A62AD	5.5~3.5	62K	1280	4	1	2	2	10	Y	IAP	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A60AD series Selection Table																
STC12LE5A08AD	3.6~2.1	8K	1280	4	1	2	2	10	Y	53K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A16AD	3.6~2.1	16K	1280	4	1	2	2	10	Y	45K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A32AD	3.6~2.1	32K	1280	4	1	2	2	10	Y	29K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A40AD	3.6~2.1	40K	1280	4	1	2	2	10	Y	21K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A48AD	3.6~2.1	48K	1280	4	1	2	2	10	Y	13K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A52AD	3.6~2.1	52K	1280	4	1	2	2	10	Y	9K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A56AD	3.6~2.1	56K	1280	4	1	2	2	10	Y	5K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
STC12LE5A60AD	3.6~2.1	60K	1280	4	1	2	2	10	Y	1K	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48
IAP12LE5A62AD	3.6~2.1	62K	1280	4	1	2	2	10	Y	IAP	Y	Y	7	PDIP40	LQFP/ PLCC	LQFP48

Type 1T 8051 MCU	Operating voltage (V)	Flash (Byte)	SRAM (B)	TIMER	UART	DPTR	16-bit PCA/ 8-bit PWM D/A	A/D	WDT	EEPROM (B)	External real-time low voltage interrupt	External Reset threshold voltage can be configured	External interrupts which can wake up power down mode	Package of 40-pin (36 I/O ports)	Package of 44-pin (40 I/O ports)	Package of 48-pin (44 I/O ports)
STC12C5A60PWM series Selection Table																
STC12C5A08PWM	5.5~3.5	8K	1280	4	1	2	2	N	Y	53K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12C5A16PWM	5.5~3.5	16K	1280	4	1	2	2	N	Y	45K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12C5A32PWM	5.5~3.5	32K	1280	4	1	2	2	N	Y	29K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12C5A40PWM	5.5~3.5	40K	1280	4	1	2	2	N	Y	21K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12C5A48PWM	5.5~3.5	48K	1280	4	1	2	2	N	Y	13K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12C5A52PWM	5.5~3.5	52K	1280	4	1	2	2	N	Y	9K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12C5A56PWM	5.5~3.5	56K	1280	4	1	2	2	N	Y	5K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12C5A60PWM	5.5~3.5	60K	1280	4	1	2	2	N	Y	1K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
IAP12C5A62PWM	5.5~3.5	62K	1280	4	1	2	2	N	Y	IAP	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12LE5A60PWM series Selection Table																
STC12LE5A08PWM	3.6~2.1	8K	1280	4	1	2	2	N	Y	53K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12LE5A16PWM	3.6~2.1	16K	1280	4	1	2	2	N	Y	45K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12LE5A32PWM	3.6~2.1	32K	1280	4	1	2	2	N	Y	29K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12LE5A40PWM	3.6~2.1	40K	1280	4	1	2	2	N	Y	21K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12LE5A48PWM	3.6~2.1	48K	1280	4	1	2	2	N	Y	13K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12LE5A52PWM	3.6~2.1	52K	1280	4	1	2	2	N	Y	9K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12LE5A56PWM	3.6~2.1	56K	1280	4	1	2	2	N	Y	5K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
STC12LE5A60PWM	3.6~2.1	60K	1280	4	1	2	2	N	Y	1K	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48
IAP12LE5A62PWM	3.6~2.1	62K	1280	4	1	2	2	N	Y	IAP	Y	Y	7	PDIP	LQFP/ PLCC	LQFP48

1.5 STC12C5A60S2 series Minimum Application System



About reset circuit:

When the clock frequency is lower than 12MHz, it is suggested not to use C1 and R1 replaced by 1K resistor connect to ground when the clock frequencies is higher than 12MHz, it is recommended to use the second reset function pin

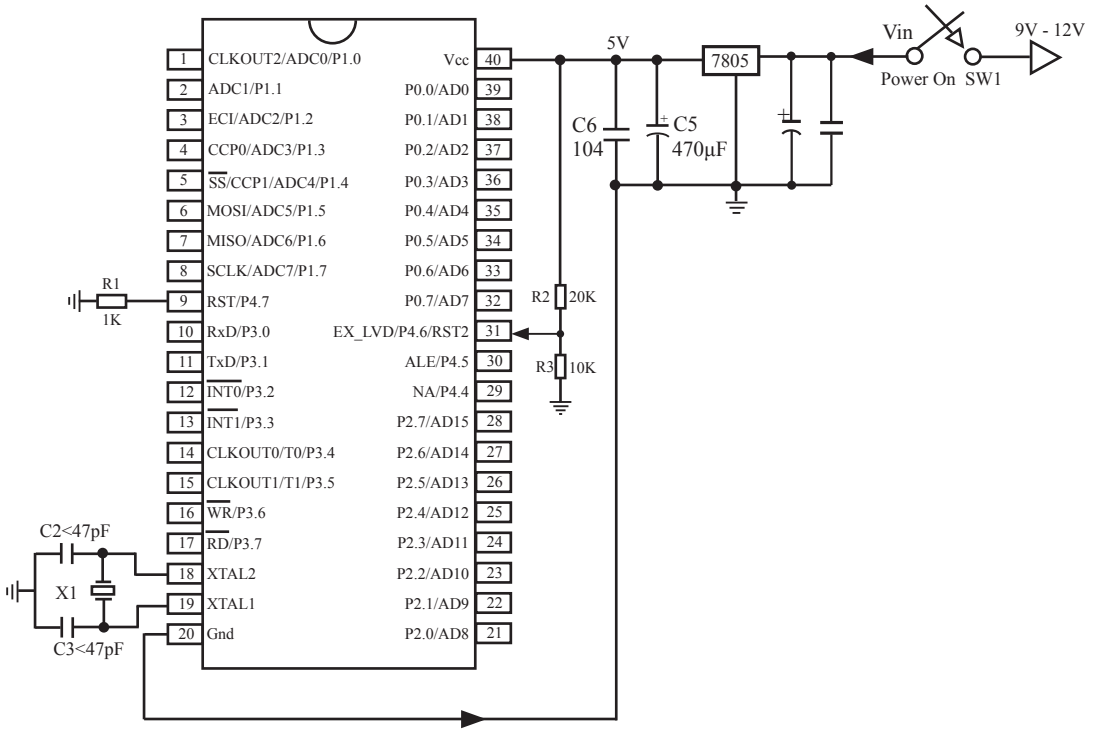
(STC12C5A60S2 series on RST2/EX_LVD/P4.6 pin
STC12C5201AD series on RST2/EX_LVD/P1.2 pin)

About crystals circuit:

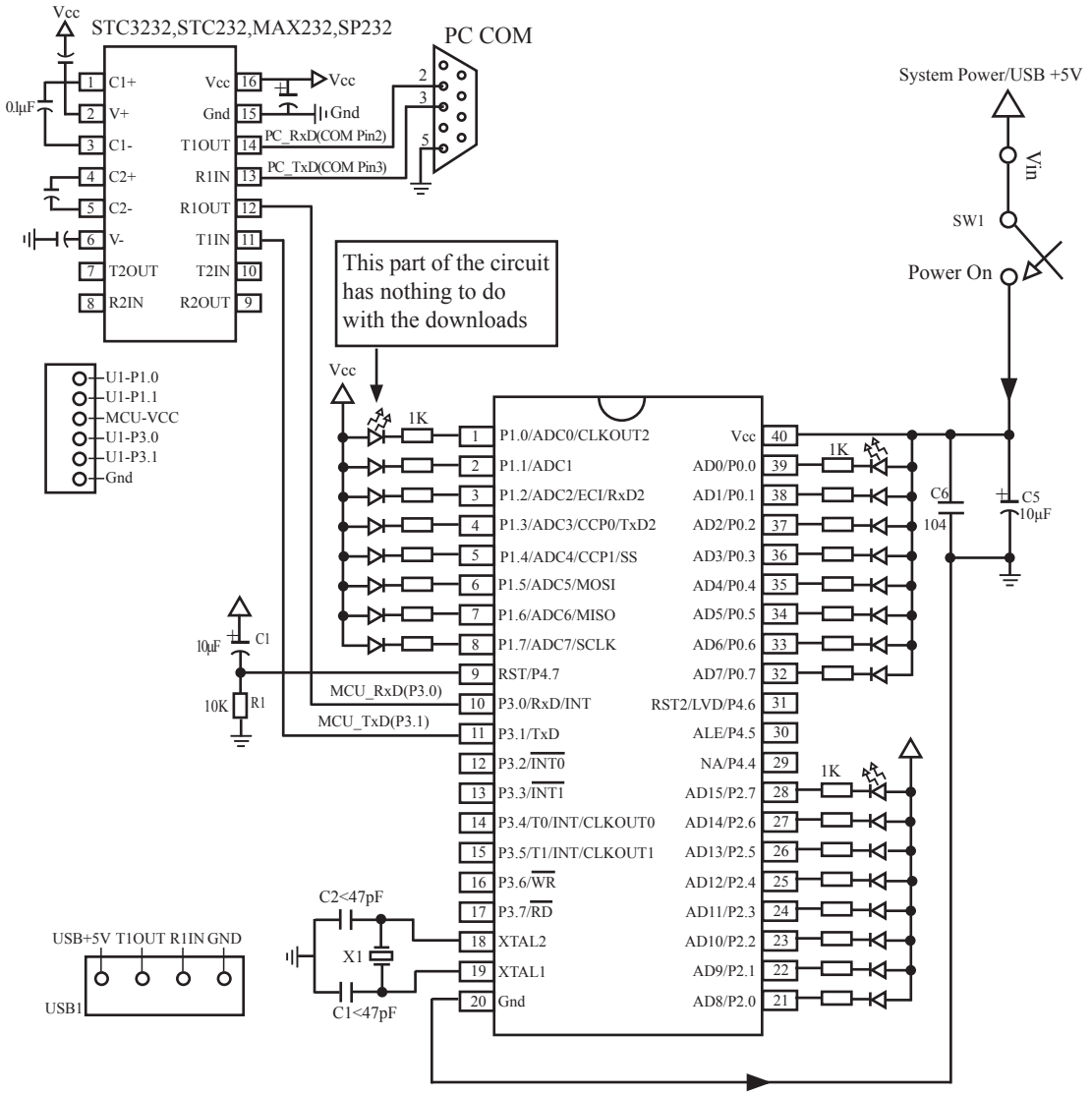
If External clock frequency is higher than 33MHz, it is recommendedto directly use external active crystals.

If using internal R/C oscillator clock (At the room temperature circumstance, the clock frequency of 5V MCU is 11MHz ~ 17MHz, 3V MCU's is 8MHz ~ 12MHz), XTAL1 and XTAL2 pin should be floated. If external clock frequency is in 27MHz above, we suggest to use the crystal that its nominal frequency is the fundamental frequency or directly use external active crystals which clock are input from XTAL1 pin and XTAL2 pin must be floated. But three partials crystals don't be used. Otherwise as parameter improper collocation, it is possible to vibrate in the fundamental frequency, and then the actual frequency is only 1/3 of nominal frequency.

when the clock frequencies is higher than 12MHz, it is recommended to use the second reset function pin. C1 can be removed and R1 replaced by 1K resistor connect to ground. So the minimum application system is shown below



1.6 STC12C5A60S2 series Application Circuit for ISP



Notes:

Traditional 8051's ALE pin regardless of whether access to external data bus, will have a clock frequency output. The signals is a source of interference to the system. For this reason,STC MCU new added a Enable/ Disable ALE signal output switch, thus reduced MCU internal to external electromagnetic emissions, improve system stability and reliability. If needs the signal as other peripheral device's clock source, you can get clock source from CLKOUT0/P3.4, CLKOUT1/P3.5, CLKOUT2/P1.0 or XTAL2 clock output. (Recommended a 200ohm series resistor to the XTAL2 pin)

Users in their target system, such as the P3.0/P3.1 through the RS-232 level shifter connected to the computer after the conversion of ordinary RS-232 serial port to connect the system programming / upgrading client software. If the user panel recommended no RS-232 level converter, should lead to a socket, with Gnd/P3.1/P3.0/Vcc four signal lines, so that the user system can be programmed directly. Of course, if the six signal lines can lead to Gnd/P3.1/P3.0/Vcc/P1.1/P1.0 as well, because you can download the program by P1.0/P1.1 ISP ban. If you can Gnd/P3.1/P3.0/Vcc/P1.1/P1.0/Reset seven signal lines leads to better, so you can easily use "offline download board (no computer)" .

ISP programming on the Theory and Application Guide to see "STC12C5201AD Series MCU Development / Programming Tools Help"section. In addition, we have standardized programming download tool, the user can then program into the goal in the above systems, you can borrow on top of it RS-232 level shifter connected to the computer to download the program used to do. Programming a chip roughly be a few seconds, faster than the ordinary universal programmer much faster, there is no need to buy expensive third-party programmer?.

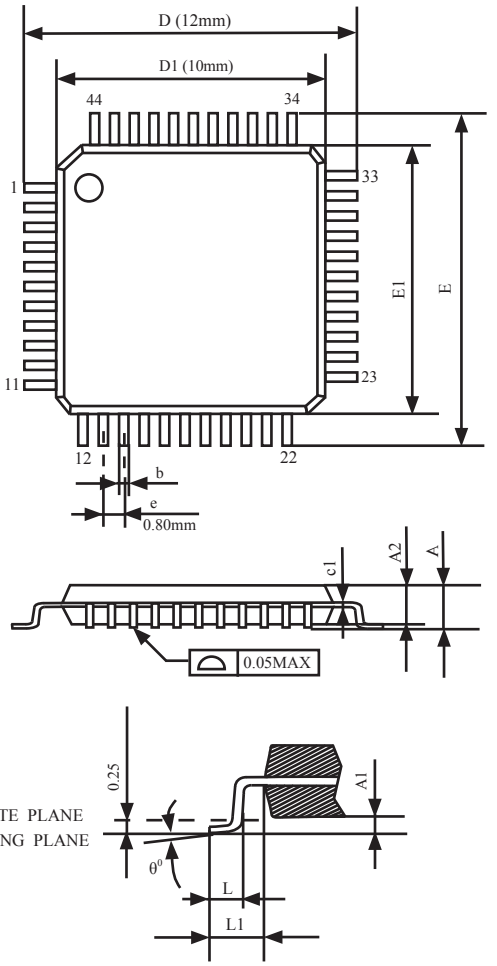
PC STC-ISP software downloaded from the website

1.7 Pin Descriptions

MNEMONIC	LQFP44	LQFP48	PDIP40	PLCC44	QFN40	DESCRIPTION
P0.0 ~ P0.7	37-30	40 ~33	39-32	43~36	34~27	**Port0** : Port0 is an 8-bit bi-directional I/O port with pull-up resistance. Except being as GPIO, Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory.
P1.0/ADC0/CLKOUT2	40	43	1	2	36	**Port1** : General-purposed I/O with weak pull-up resistance inside. When 1s are written into Port1, the strong output driving CMOS only turn-on two period and then the weak pull-up resistance keep the port high. **ADCn**: Analog to Digital Converter Input
P1.1/ADC1	41	44	2	3	37	
P1.2/ADC2/ECI/RxD2	42	45	3	4	38	
P1.3/ADC3/CCP0/TxD2	43	46	4	5	39	
P1.4/ADC4/CCP1/SS	44	47	5	6	40	
P1.5/ADC5/MOSI	1	2	6	7	1	
P1.6/ADC6/MISO	2	3	7	8	2	
P1.7/ADC7/SCLK	3	4	8	9	3	
P2.0 ~ P2.7	18-25	19-23	21-28	24~31	16~23	**Port2** : Port2 is an 8-bit bi-directional I/O port with pull-up resistance. Except being as GPIO, Port2 emits the high-order address byte during accessing to external program and data memory.
		26-28				
P3.0/RXD	5	6	10	11	5	**Port3** : General-purposed I/O with weak pull-up resistance inside. When 1s are written into Port3, the strong output driving CMOS only turn-on two period and then the weak pull-up resistance keep the port high. Port3 also serves the functions of various special features of STC12C5A60S2.
P3.1/TXD	7	8	11	13	6	
P3.2/INT0	8	9	12	14	7	
P3.3/INT1	9	10	13	15	8	
P3.4/T0/INT/CLKOUT0	10	11	14	16	9	
P3.5/T1/INT/CLKOUT1	11	12	15	17	10	
P3.6/WR	12	13	16	18	11	
P3.7/RD	13	14	17	19	12	
P4.0/SS	17	18		23		**Port4** : Port4 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44. **ALE**: Address Latch Enable. It is used for external data memory cycles (MOVX) **EX_LVD**: External Low Voltage Reset Detector
P4.1/ECI/MOSI	28	31		34		
P4.2/CCP0/MISO	39	42		1		
P4.3/CCP1/SCLK	6	7		12		
P4.4/NA	26	29	29	32	24	
P4.5/ALE	27	30	30	33	25	
P4.6/EX_LVD/RST2	29	32	31	35	26	
P4.7/RST	4	5	9	10	4	
RST	4	5	9	10	4	**RESET**: A high on this pin for at least two machine cycles will reset the device.
P5.0		24				**Port5**: Port5 are extended I/O ports such like Port1. It can be available only on LQFP48.
P5.1		25				
P5.2		48				
P5.3		1				
XTAL1	15	16	19	21	14	**Crystal1**: Input to the inverting oscillator amplifier. Receives the external oscillator signal when an external oscillator is used.
XTAL2	14	15	18	20	13	**Crystal2**: Output from the inverting amplifier. This pin should be floated when an external oscillator is used.
VCC	38	41	40	44	35	**Power**
Gnd	16	17	20	22	15	**Ground**

1.8 Package Dimension Drawings

LQFP-44 OUTLINE PACKAGE

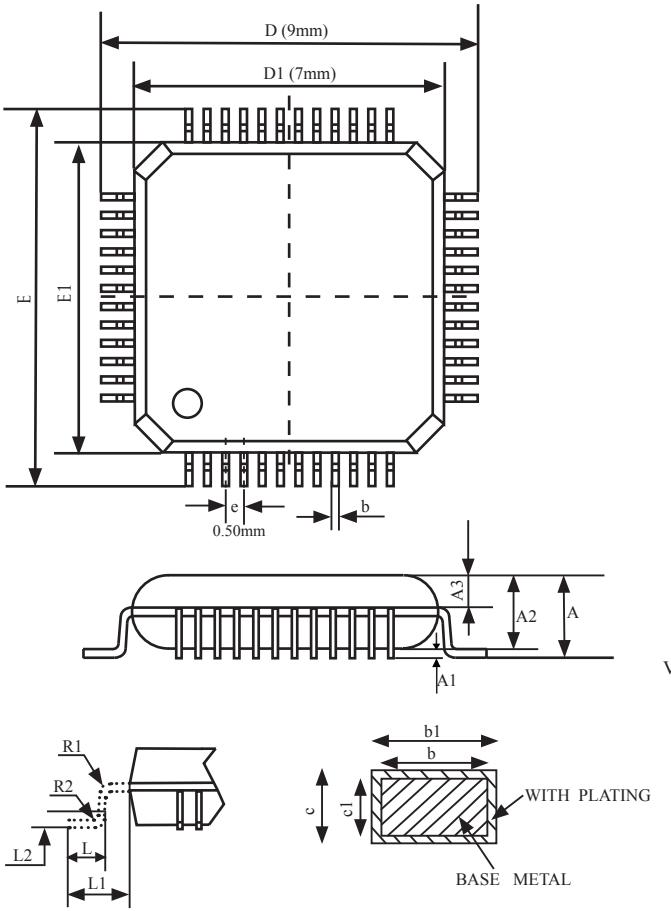


VARIATIONS (ALL DIMENSIONS SHOWN IN MM

SYMBOLS	MIN.	NOM	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
c1	0.09	-	0.16
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
e		0.80	
b(w/o plating)	0.25	0.30	0.35
L	0.45	0.60	0.75
L1		1.00REF	
θ^0	0^0	3.5^0	7^0

NOTES:
1.JEDEC OUTLINE:MS-026 BSB
2.DIMENSIONS D1 AND E1 D0 NOT INCLUDE MOLD PROTRUSION. ALLOWBLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWBLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUN b DIMNSION BY MORE THAN 0.08mm.

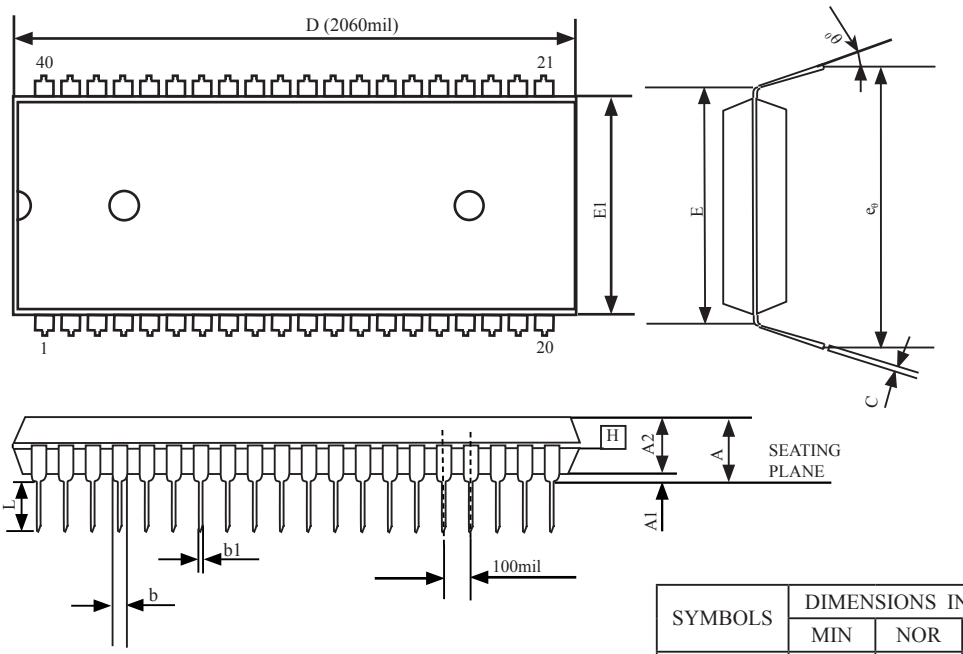
LQFP-48 OUTLINE PACKAGE



SYMBOL	MIN	NOM	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.50	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25	
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-

VARIATIONS (ALL DIMENSIONS SHOWN IN MM

PDIP-40 OUTLINE PACKAGE

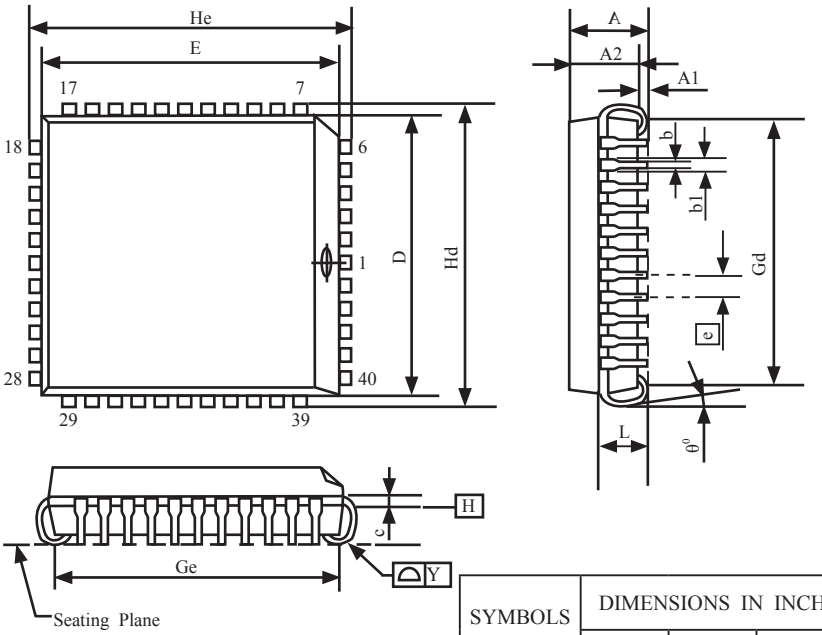


SYMBOLS	DIMENSIONS IN INCH		
	MIN	NOR	MAX
A	-	-	0.190
A1	0.015	-	0.020
A2	0.15	0.155	0.160
C	0.008	-	0.015
D	2.025	2.060	2.070
E	0.600 BSC		
E1	0.540	0.545	0.550
L	0.120	0.130	0.140
b1	0.015	-	0.021
b	0.045	-	0.067
e_0	0.630	0.650	0.690
0	0	7	15

UNIT: INCH 1 inch = 1000mil

NOTE:
1.JEDEC OUTLINE :MS-011 AC

PLCC-44 OUTLINE PACKAGE



SYMBOLS	DIMENSIONS IN INCH			DIMENSIONS IN MILLMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.165	-	0.180	4.191	-	4.572
A1	0.020	-	-	0.508	-	-
A2	0.147	-	0.158	3.734	-	4.013
b1	0.026	0.028	0.032	0.660	0.711	0.813
b	0.013	0.017	0.021	0.330	0.432	0.533
c	0.007	0.010	0.0013	0.178	0.254	0.330
D	0.650	0.653	0.656	16.510	16.586	16.662
E	0.650	0.653	0.656	16.510	16.586	16.662
e	0.050BSC			1.270BSC		
Gd	0.590	0.610	0.630	14.986	15.494	16.002
Ge	0.590	0.610	0.630	14.986	15.494	16.002
Hd	0.685	0.690	0.695	17.399	17.526	17.653
He	0.685	0.690	0.695	17.399	17.526	17.653
L	0.100	-	0.112	2.540	-	2.845
Y	-	-	0.004	-	-	0.102

1 inch = 1000 mil

NOTE:

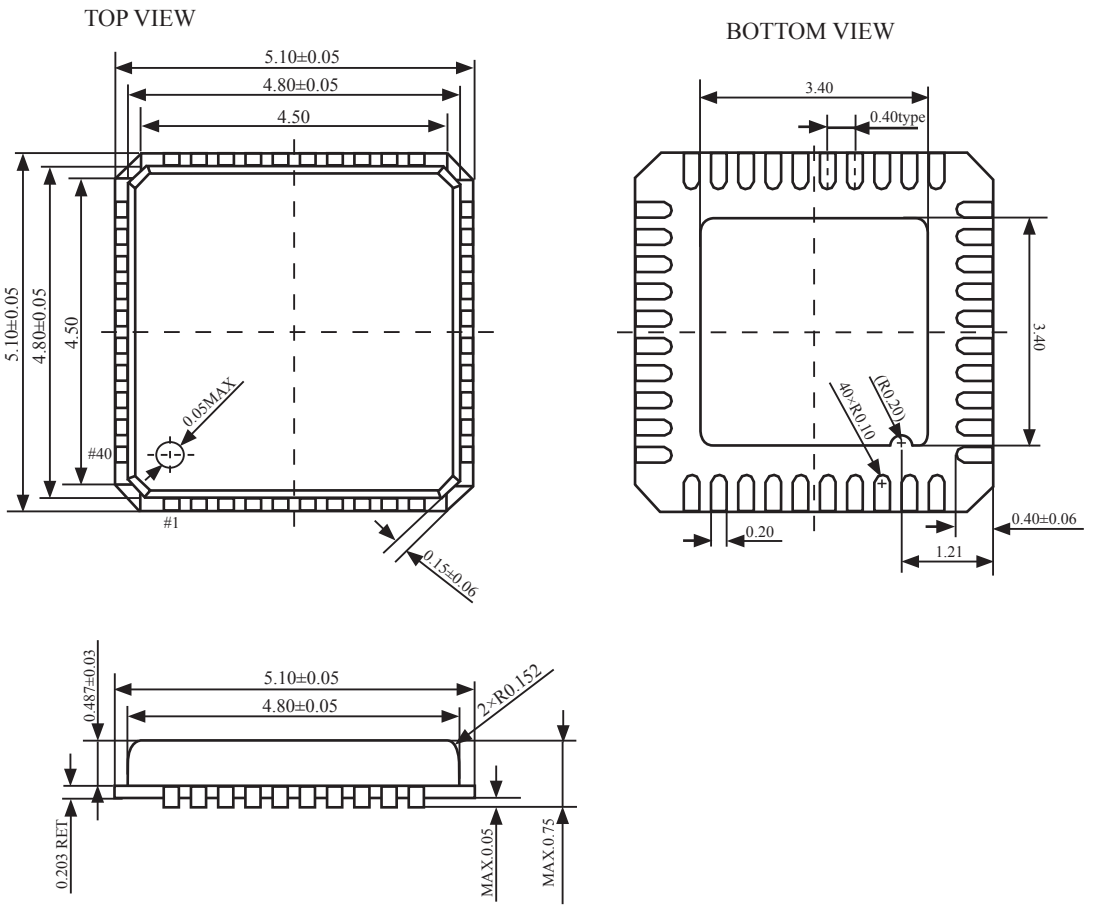
1.JEDEC OUTLINE :M0-047 AC

2.DATUM PLANE H IS LACATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS E AND D D0 NOT INCLUDE MODE PROTRUSION. ALLOWABLE PROTRUSION IS 10 MIL PRE SIDE.DIMENSIONS E AND D D0 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION.

QFN-40 OUTLINE PACKAGE



1.9 STC12C5A60S2 series MCU naming rules